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Novel Design of Four-Bit Reversible Numerical Comparator

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Abstract— In this paper, a new four bit reversible comparator circuit has been designed and was found that the proposed design is better in terms of no. of garbage outputs, no. of reversible logic gates used and no. of constants inputs than previous design. Reversible Logic Technology is becoming a very popular technology in the field of Nano-electronics, Low Power Chip Design, and Quantum Circuits etc. The comparator design has been modeled and verified using VHDL and Active-HDL 7.1 Version.

Keywords- Reversible Logic Gate; Quantum Cost; Garbage Output; Constant Input; Comparator.

I. INTRODUCTION

A comparator is a circuit that takes two numbers as input in binary form and determines whether one number is less than, greater than or equal to the other number. Comparator circuits are very important and commonly used for computing systems like Analog to Digital and Digital to Analog Convertors, Error Detectors, Microprocessors, Microcontrollers, and Communications Systems etc. In conventional circuits, the comparison is carrying out irreversibly i.e. once output bits are generated the input bits are lost forever, but this is not in the case of reversible logic circuits. In recent years, reversible logic circuits are used at large level in low power VLSI design. The conventional logic gates like AND, OR, EXOR, NAND etc. are not reversible as they are all multiple input-single output gates. Input states are lost because there are less number of outputs than inputs, i.e. output contain less information than input. This loss of information leads to the loss of energy in the form of heat. According to R. Landauer [1], circuit design based on irreversible logic operations produces $kT\ln 2$ joules of energy, where k is Boltzmann's Constant, T is the absolute temperature ($300K$).

According to C.H. Bennet [2], a circuit designed using reversible logic gates consume zero power and no heat is dissipated. In reversible logic gates there are equal number of inputs and outputs. A reversible gate only moves the states around and no information is lost i.e. no energy is lost and heat dissipation is zero.

II. REVERSIBLE LOGIC CIRCUIT OPTIMIZATION PARAMETERS

Reversible logic circuits are designed using reversible logic gates. Reversible logic gates have equal number of inputs and outputs. Reversible logic gate has distinct output for each distinct input. In reversible logic gates the input states are uniquely determined from the output states. A reversible logic gate is balanced, i.e. the outputs are 1s for exactly half of the inputs. Optimization parameters are very important for designing an optimized reversible logic circuit and determine the complexity and performance of the circuit. The optimization parameters are as follows:

- Reversible Gates: The number of reversible gates used to realize the function and should be as minimum as possible so as to reduce delay, quantum cost and area.

- Quantum Cost: This refers to the cost of the circuit in terms of reversible gates used and should be minimum to reduce the circuit cost.

- Garbage Output: This refers to the no. of outputs which are not used and therefore it should be as small as possible.

- Constant Input: This refers to the no. of inputs to be maintained constant at either logic 0 or logic 1 and should be minimum.

- Delay: The delay is the propagation delay of the critical path where, critical path is the path to the output

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which has the maximum delay and so it should be minimum.

- Fan-out: Fan-out is not allowed in reversible logic circuits.

III. REVERSIBLE LOGIC GATES USED IN PROPOSED ARCHITECTURE

In proposed architecture design following reversible logic gates is used:

- STG Gate (as AND gate),
- STAG Gate (as a full adder),
- Feynman Gate (as a copying gate) and
- NOT Gate (as an inverter).

A. STG gate

STG gate is a three input-three output reversible logic gate as shown in Fig. 1(a) with its truth table in Table1. From truth table, it is clear that the input pattern corresponding to a specific output pattern can be uniquely determined and hence maintaining a one-to-one mapping between the input vector and the output vector. The STG gate is used as two input AND gate. For using STG gate as two input AND gate put C=0, then last third output terminal give the required AND operation as shown in Fig. 1(b).

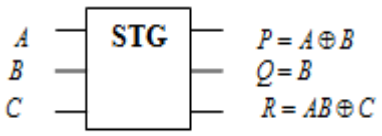

Fig. 1(a): Reversible STG gate

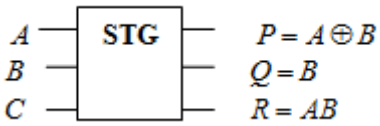

Fig. 1(b): STG gate as AND gate

TABLE I
TRUTH TABLE OF STG GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	1	0

B. STAG Gate

STAG gate is a four input-four output reversible logic gate as shown in Fig. 2(a) with its truth table in Table 2. From truth table, it is clear that the input pattern corresponding to a specific output pattern can be uniquely determined and hence maintaining a one-to-one mapping between the input vector and the output vector. The STAG gate is used as Full Adder. For using STAG gate as Full Adder put D=0, then first output terminal give the Sum output and last output terminal give the required Carry output as shown in Fig. 2(b).

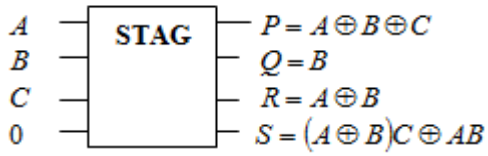

Fig. 2(a): Reversible STAG gate

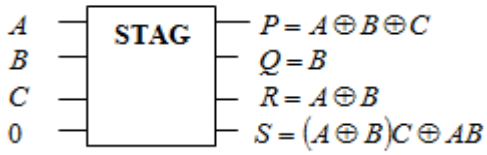

Fig.2(b): STAG gate as Full Adder

TABLE II
TRUTH TABLE OF STAG GATE

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	1	0	0	0
0	0	1	1	1	0	0	1
0	1	0	0	1	1	1	0
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	1
1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	1
1	1	0	1	0	1	0	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0

C. Feynman Gate

Feynman gate is also known as controlled-not gate shown in Fig. 3(a). It implements the logic functions: $P = A$ and $Q = A \oplus B$. Since the fan-out in the reversible circuit is 1, this gate is often used as a copying gate to duplicate the required output. Fig.3 (b) shows the Feynman gate as a copying gate. If B=0 then $P = A$ and $Q = A$.

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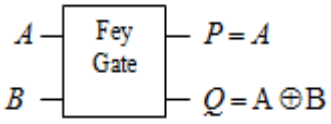

Fig. 3(a): Feynman gate

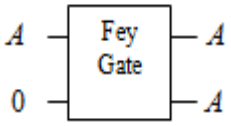

Fig. 3(b): Feynman gate as a copying gate

TABLE III
TRUTH TABLE OF FEYNMAN GATE

INPUT		OUTPUT	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

D. NOT Gate

NOT gate is the only conventional logic gate which is also reversible logic gate. It is used as an inverter to invert the applied input. It is a one input-one output reversible logic gate as shown in Fig. 4 and implements the logic function: $P = \overline{A}$.

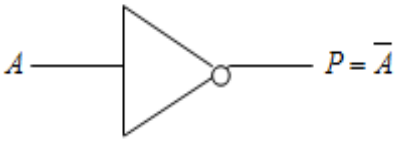

Fig. 4: NOT Gate

IV. 4-BIT COMPARATOR DESIGN

The generalized equation for a comparator circuit that compares two 4-bit binary numbers A and B is given below:

- When A is equal to B, the output signal $F_{A=B}$ goes high, and $F_{A=B} = E_3E_2E_1E_0$
  Where $E_i = (A_iB_i) + (\overline{A_iB_i})$ for $i = 0,1,2,3.$

- When A is greater than B, the output signal $F_{A>B}$ goes high and
  $F_{A>B} = G_3 + E_3G_2 + E_3E_2G_1 + E_3E_2E_1G_0$
  Where $G_i = A_i\overline{B_i}$ for $i = 0,1,2,3.$

- When A is smaller than B, the output signal $F_{A<B}$ goes high and
  $F_{A<B} = S_3 + E_3S_2 + E_3E_2S_1 + E_3E_2E_1S_0$
  Where $S_i = \overline{A_i}B_i$ for $i = 0,1,2,3.$

For designing of 4-bit comparator circuit above equations has to be implemented and for this reason STG Gate as AND gate, STAG Gate as Full Adder, Feynman gate as Copying gate and NOT gates are used.

A. 4-BIT COMPARATOR DESIGN: MATHAMATICAL PROOF

Proposed Four Bit Reversible Comparator Architecture Contains:

- Four STAG gates as a full adder,
- Four STG gates as reversible AND gate,
- Two Feynman gates as a copying gate and
- Ten NOT gates as an inverter.

The final architecture of four bit reversible comparator is shown in Figure 6. It can compare the value of two binary numbers A and B, where $A = (A_3, A_2, A_1, A_0)$ and $B = (B_3, B_2, B_1, B_0)$ and generate the comparison result in the form of three output signals F_1, F_2, F_3. When $A < B$, F_1 output signal goes high i.e. $F_1 = F_{A<B} = 1.$ When $A > B$, F_3 output signal goes high i.e. $F_3 = F_{A>B} = 1.$ When $A = B$, F_2 output signal goes high i.e. $F_2 = F_{A=B} = 1.$
From simulation result as shown in Figure 5 it is proved that

- A is smaller than B: F_1 output signal is high.
When we apply Inputs as $A_3A_2A_1A_0 = 0000$, $B_3B_2B_1B_0 = 1111$ and get Outputs as $F_1F_2F_3 = 100.$

- A is equal to B: F_2 output signal is high.
When apply Inputs as $A_3A_2A_1A_0 = 1111$ and $B_3B_2B_1B_0 = 1111$ we get Outputs as $F_1F_2F_3 = 010.$

- A is greater than B: F_3 output signal is high.
When apply Inputs as $A_3A_2A_1A_0 = 1111$ and $B_3B_2B_1B_0 = 0000$ we get Outputs as $F_1F_2F_3 = 001.$

B. 4-Bit COMPARATOR DESIGN: VHDL SIMULATION

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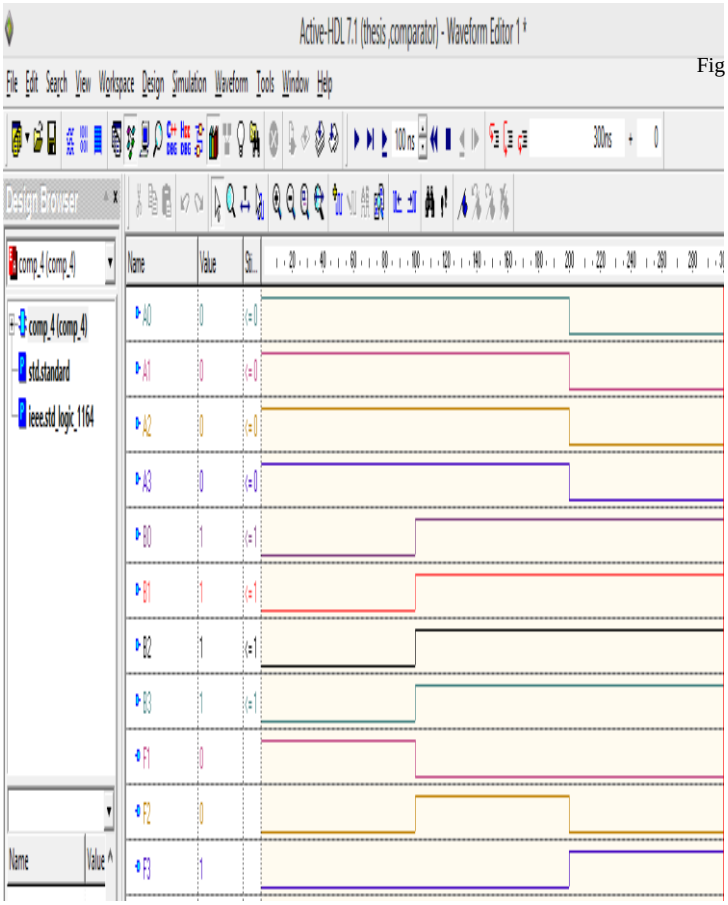

Fig 5. Simulation result of proposed architecture design of 4-bit reversible comparator circuit

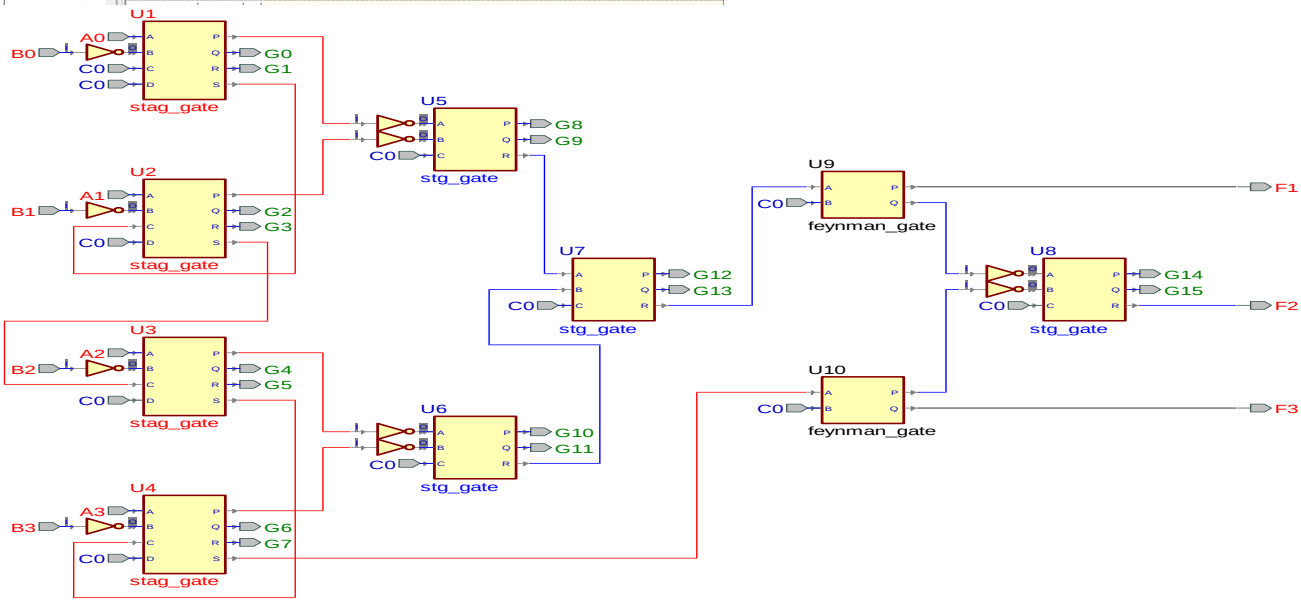

Fig 6. Proposed Architecture Design of 4- bit Reversible Comparator Circuit

V. COMPARISON BETWEEN PROPOSED AND EXISTING 4-BIT COMPARATOR CIRCUITS

The comparison result is shown in Table IV. From table it has been clear that proposed architecture design is much better and optimized in terms of no. of gates, no. of garbage outputs and no. of constants inputs.

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TABLE IV
COMPARISON TABLE BETWEEN PROPOSED AND EXISTING COMPARATOR CIRCUITS

Parameters	*No. of gates*	*No. of GO's*	*No. of CI's*
Proposed circuit	10	16	11
Existing Circuit [11]	25	23	17
Improvement in %	60	43.75	35.29

VI. CONCLUSION

From the above discussions it has been proved that the proposed architecture design of comparator circuit is much better than its predecessor in terms of no. of gates, no. of garbage outputs and no. of constant inputs. This architecture design can be used in various low power arithmetical and logical operations.

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