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Analysed Modulation Doped Fieled Effect Transister (MODFET) and Metal Oxide Semiconductor Modulation Doped Fieled Effect Transister ((MOS-MODFET)) using compound material silicon Germanium (SiGe)

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Abstract: In this paper SiGe material incorporated to design Modulation Doped Fieled Effect Transister (MODFET) and analysed theoretically. The SiGe is a compound semiconductor material and impurity material is P-type. The Gate length of MOS-MODFET is fabricated 0.1µm. The SiGe/Si Heterojunction grown by ultrahigh vacuum chemical vapor deposition technique. The performance of modulation-doped field effect transistor is a new approached to design FET with heterojunction field effect transistor (HBT). The performance of MOS-MODFET is also a good approached to design device as CMOS with the HBT. The characteristics shown is improved the speed and power consumption with BJT and MOSFET.

Keywords: Modulation doping , MODFET, MOS-MODFET, and Characteristics

I. INTRODUCTION

CMOS digital circuits represent low-power consumption and the possibility of dynamic memories. Silicon Bipolar Junction Transistors (BJTs) are used about 20% of all integrated circuits, mostly high-speed and analog applications. The trend of increasing switching speeds and communication rates demands further improvement of the performance of BJT. In addition, at the present considerable number of BiCMOS circuits, which combine the high-current drive capability of BJTs with the low-power CMOS demonstrate new application for bipolar transistors [1]. The SiGe Heterojunction Bipolar Transistor (HBT) is one device that can meet these demands. Doped with III-V element in SiGe devices offer superior performance over silicon made device due to better material parameters as mobility and carrier velocity. The band-gap of SiGe is in beneath Si and Ge and the application of quantum effects have yielded new devices as, the modulation doped field effect transistor (MODFET). It has low noise.

II. MODULATION DOPING $Si_{1-x}Ge_x$ STRAINED LAYER

Heteroepitaxy of Si/Ge_xSi_{1-x}offers exciting possibilitis for integrated field-effect transistor (FET) structures [2]. In addition to such application, system also offers a unique opportunity to determine the effects of misfit strain on the transport properties of indirect gap semiconductor heterointerfaces and strained layer superlatices since the lattice mismatch between Si and Ge is ~4%. Recent progress in silicon molecular beam epitaxy (Si MBE) coupled with a quantitative determine of growth parameters pertinent to the pseudomorphic growth of Ge_xSi_{1-x}/Si strained layers has made it possible to achieve the first two-dimensional hole gas at a Si/$Ge_{0.2}Si_{0.8}$ heterointerface.

III. MODFET STRUCTURE

The SiGe/Si heterostructure layer is grown by ultra high vacuum chemical deposition (UHV-CVD) on an n^- Si substrate. The layer sequence started with linearly step-graded $Si_{(1-x)}Ge_x$ buffer layer relaxed to the lattice constant of $Si_{0.7}Ge_{0..3}$. A 1µm-thick $Si_{0.7}Ge_{0..3}$ buffer layer is followed by the modulation-doped structure which consisted a 4-nm B-doped $Si_{0.7}Ge_{0..3}$ supply layer at a doping density Of $2x10^{18}$ cm, a 3-nm undoped $Si_{0.7}$ $Ge_{0.3}$ spacer, and a 4.5 nm-thick $Si_{(1-x)}Ge_x$ channel graded from 0.8 to 0.7, and a 10 nm

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$Si_{0.7}$ $Ge_{0.3}$ cap layer. The layer exhibited a 2-D hole-gas mobility shown in figure1.

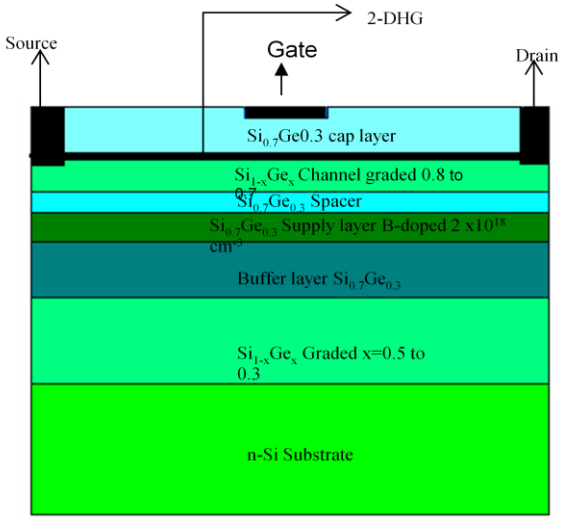

Figure1: Modulation Doped Field Effect Transistor (MODFET)

Ids-Vds Characteristics of Modulation Doped Field Effect Transistor (MODFET):

Current–voltage characteristics of modulation doped field effect transistor may be found based on the charge control model, using the channel approximation concept, the surface carrier concentration in the channel is given by[3].

$$n_s = \frac{\varepsilon}{q(d+\Delta d)}[V_g - V_{off} - V(x)] \quad (1)$$

Where, x is the space along the channel length and V(x) is the channel potential equation.
The current through the channel is defined by

$$I_{ds} = qn_s v(F)W \quad (2)$$

The I_{ds} is the drain-to-source current, electron velocity $v(F)$, which is the function of the electric field F in the channel. Here W is the gate width. Using the gradual channel approximation. The electric field in the channel is parallel to the heterointerface (it is directed from drain to the source) and neglect the diffusion current.
The electron velocity is simply proportional to the electric field:

$$v = \mu F \quad (3)$$

Where, μ is the effective field mobility.

By the Shockley model equation describing the current-voltage characteristics of the MODFET at low drain to source voltage Vds [4]:

$$I_{ds} = \frac{\varepsilon \mu W}{(d+\Delta d)L}[(V_g - V_{off})V_{ds} - V_{ds}^{\ 2}/2] \quad (4)$$

Where d= d_d +d_i
d_d = Thickness of the doped (B, SiGe) beneath the gate
d_i = Thickness of the undoped SiGe beneath the gate
In this expression one thing is noted down that Vg, and V_{off} is negative because the device is 2-Dimentional Hole Gas.

$$I_{ds} = \frac{\varepsilon \mu W}{(d+\Delta d)L}[-(V_g - V_{off})V_{ds} - V_{ds}^{\ 2}/2] \quad (5)$$

The current is in ampere, and it is dependent to the length of gate and drain to source, so the dimension should be in account with length also. i.e. $\frac{I_{ds}}{DS}$ Where DS, is the distance between drain to source.

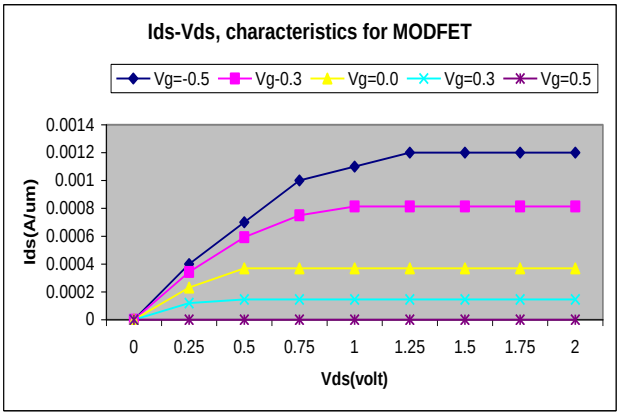

Figure2: Ids – Vds characteristics for different gate voltages

The figure2 is current – voltage characteristics for different gate voltages. Here gate voltages varied from -0.5 to +0.5v. When voltage at drain terminal i.e. Vds is applied then two

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dimensional hole gas is accelerated by this voltage and current will flow because of lattice free charges are there so that it starts to flow a minimum voltage of Vds at negative gate voltage. In the figure it is clear that when gate is raised from negative value to positive values then graph is shifted to lower as shown in the figure2.

IV. MOS-MODFET STRUCTURE

The processing of MOS-MODFET's started with the deposition of a 20-nm-thick SiO_2 film using the JVD method [5]. To density the film, the sample received a post-deposition annealing at 300 ^{0}C in nitrogen ambient for 30 min. 240-nm-thick electron beam-evaporated SiO_2 film. The ohmic metallization of 30-nm-thick Pt was evaporated and lifted-off after the oxide in the ohmic area was removed by wet chemical etching. The gates length is 0.1µm with a trilayers resist system using electron beam lithography. Finally, the contact pads were defined by deposition of Ti/Pt/Au. The distance between source-drain is 4µm while the gate width of this device is 1µm.The device structure of MOS-MODFET's is shown in Figure3.

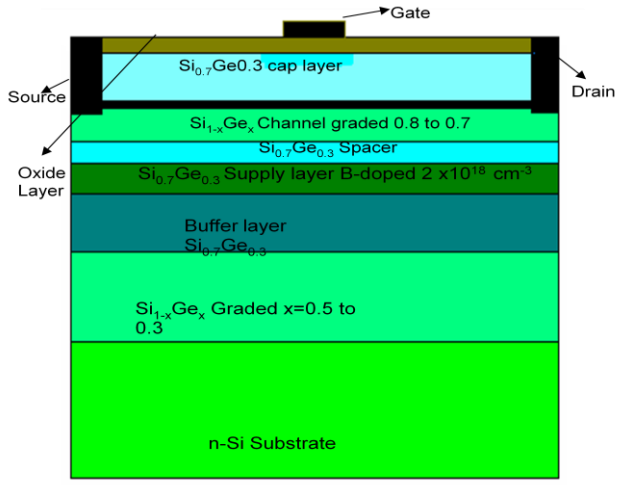

Figure3: Metal Oxide Semiconductor Modulation Doped Field Effect Transistor (MOS-ODFET)

Ids-Vds Characteristics of Metal Oxide Semiconductor Modulation Doped Field Effect Transistor (MOS-MODFET):

In the MOS-MODFET there is the slight change in the Height of the gate to channel distance. In MODFET the distance of the height is as '$d_d + d_i + \Delta d$.' But the MOS-MODFET the effected distance is counted as from addition of cap layer thickness i.e. 'cap layer thickness + $d_d + d_i + \Delta d$.'

And formula is same as equation (5)

$$I_{ds} = \frac{\varepsilon \mu W}{(d' + \Delta d)L}[(V_g - V_{off})V_{ds} - V_{ds}^{\ 2}/2] \quad (6)$$

Where d'=thickness of cap layer+ $d_d + d_i$

In this expression one thing is noted down that Vg, and V_{off} is negative because the device is 2-Dimentional Hole Gas. So, the expression now slightly changes as:

$$I_{ds} = \frac{\varepsilon \mu W}{(d' + \Delta d)L}[-(V_g - V_{off})V_{ds} - V_{ds}^{\ 2}/2] \quad (7)$$

The current is in ampere, but the current is dependent to the length of gate and drain to source, so the dimension should be in account with length also. i.e. $\frac{I_{ds}}{DS}$ Where DS, Is the distance between drain to source.

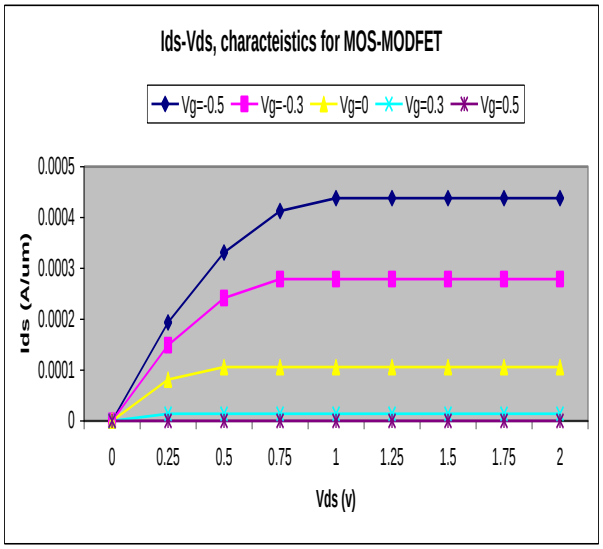

Figure4: Ids – Vds characteristics for different gate voltages

The figure4 shown above is current – voltage characteristics for different gate voltages.The gate is isolated by oxide so the device is known as MOS-MODFET (metal oxide semiconductor MODFET) Here gate voltages varied from -0.5 to +0.5v. When voltage at drain terminal i.e. Vds is applied then two dimensional hole gas is accelerated by this voltage and this carriers are controlled by the insulated gate and current will start to flow because of lattice free charges

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are there so that it starts to flow a minimum voltage at negative gate voltages current is higher than high gate voltages as shown in the figure4.

Parameters Values Used:
Oxide thickness = 20 nm
Thickness of $Si_{0.7}Ge_{0.3}$ cap layer = 10 nm
Thickness of $Si_{1-x}Ge_x$ Channel graded 0.8 to 0.7 = 4.5 nm
Thickness of $Si_{0.7}Ge_{0.3}$ Spacer = 3 nm
Thickness of $Si_{0.7}Ge_{0.3}$ Supply layer B-doped 2 $x10^{18}$ cm^{-3} = 4 nm
Thickness of Buffer layer $Si_{0.7}Ge_{0.3}$ = 100 nm
Thickness of Si $_{1-x}Ge_x$ Graded from x=0.5 to 0.3 = n-Si Substrate
ε_{SiGe} = 1.17 x 10^{10} F/m, [6]
μ(for hole) = 815 cm^2/v-s
Width of gate (W) =1um
Gate length (L) = 1um
Φ_b = 0.9 ev
ΔE_c = 0.15 ev
d_d = 4 nm
d_i = 3 nm
ΔE_{F0} = 0.025 ev
Δd = 9 nm

V. CONCLUSION

The MODFET and MOS-MODFET is novel devices in which channel are obtained by modulation doping as 2-DEG (Two dimensional electron gas) or 2-DHG(two dimensional hole gas). This channel is free from lattice scattering problems. The formation of oxide layer on to MODFET surface so, that there is a way to find CMOS devices. This device has better performance as Radio frequency range so its application in the wireless communication is very important as comparison to other device in case of performance and cost effective.

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BIOGRAPHY

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