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A Robust Power Downgrading Technique using Sparse Modulo 2^n+1 Adder

S.Surabhi[1], M.Jagadeeswari[2]

PG Scholar, Department of VLSI Design, Sri Ramakrishna Engineering College, Coimbatore, India[1]

Professor and Head, Department of VLSI Design, Sri Ramakrishna Engineering College, Coimbatore, India [2]

Abstract – A promising direction for dramatically suppressing the power utilised by a circuit is reducing the dynamic power which dominates total power dissipation. An architecture that reduces the power by separating the target design into two parts; MSP & LSP and it switches off the MSP whenever it does not affect the computation result to reduce the power consumption is proposed in the paper. It also introduces an advanced glitch-diminishing technique to remove the unwanted switching power by asserting the data signals after data transient period. The LSP section employs a sparse modulo adder constructed with a gray operator that do not require extra logic gates which reduces the carry computational complexity and minimizes the area for an enhanced quick output. MSP is a collection of an ordinary adder, latches, detection logic unit and a sign extension. The experimental data reveal that the proposed technique offer a higher operation speed with minimum power consumption of 0.173W.

Index terms - Low power design, modulo arithmetic, glitches, dynamic power, data transient period.

I. INTRODUCTION

Low power and small area are mandatory requirements for designing electrical devices used in day to day life. This paper can drastically minimise the power dissipation of combinational VLSI designs for multimedia/DSP applications. The data of the multimedia/DSP computations, such as transform coding and texture coding in any systems, tend to fluctuate within a small range of bit width because of the temporal and spatial redundancies existing in video signals. Thus, the corresponding hardware design still needs to provide the maximum data bit width to acquire data accuracy. There are many techniques that have been developed for reducing the power consumption of VLSI designs, including voltage scaling, switched-capacitance reduction, clock gating, power-down techniques, threshold-voltage controlling, multiple supply voltages, and dynamic voltage frequency scaling[1]-[5]. Among these techniques the most relevant technique for marking down the power consumption is by lowering the dynamic power that dominates total power dissipation which is achieved by the proposed power downgrading technique. From the viewpoint of logic design, the adders in the design are divided into two parts, i.e., the *Most Significant Part* (MSP) and the *Least Significant Part* (LSP), and the input data of the MSP circuits are latched whenever they do not influence the computation results. The MSP employs Detection-logic and Sign Extension (SE) blocks in the proposed RPDT (Robust Power Downgrading Technique) to determine the effective ranges of the operands and compensate for the sign signals of the MSP, respectively.

Even if the concept is similar to partially guarded computation (PGC), efficiently implementing the technique and manifesting its effects on power saving in real circuits remains challenging.

Modulo $2^n + 1$ adders that minimises the carry computation complexity are employed in the LSP to enhance the efficiency of the entire circuitry. The resulting RBDT adders can be achieved in smaller area and subjected power consumption compared to all existing works, while maintaining a high operation speed. The diminished-1 representation of binary numbers was introduced to speed up the modulo $2^n + 1$ arithmetic operations. For large word lengths, the design of sparse parallel prefix adders is chosen, since the wiring and area of the architectural design are significantly reduced without sacrificing delay. The design of sparse adders relies on the use of a sparse parallel-prefix carry computation unit and carry-select (CS) blocks. Only the carries at the boundaries of the carry-select blocks are computed, saving considerable amount of area in the carry-computation unit. A 24-bit RPDT adder is divided into MSP and LSP between the 15^{th} and 16^{th} bits.

The adder operation is kept unchanged because most of the spurious signals existed in the data flowing out of the first and the second stages have been filtered out by the RPDT. The most effective way to increase the speed of an adder is to reduce the delay in producing carries between each bit of the calculation .To reduce the number of calculation steps for the carry calculation and thus the addition evaluation, architectures has been applied mostly where sparse tree has taken the role of increasing the speed to calculate carry and RPDT to remove unwanted calculations and sort out the spurious signals.

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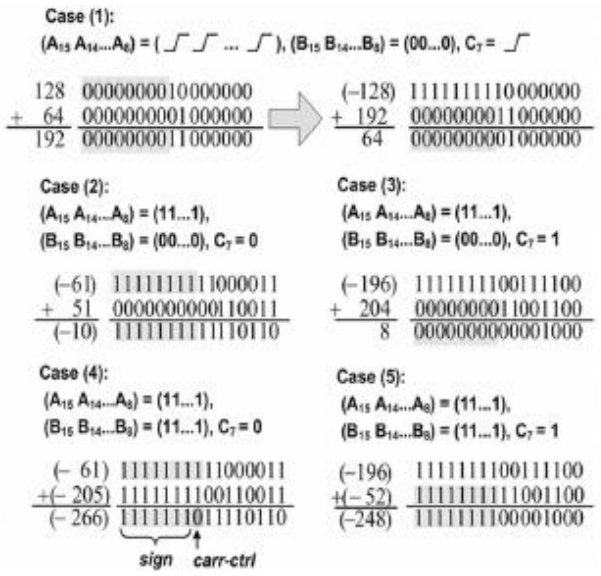

Fig. 1. Spurious transitions in the DSP computations.

II. MATERIALS AND METHODS

A. *Related Work*

Various techniques employed for reducing the power consumptions of VLSI designs are voltage scaling, switched-capacitance reduction, clock gating, power-down techniques, threshold-voltage controlling, multiple supply voltages, and dynamic voltage frequency scaling as said in [1]-[4]. The existing works that reduce the dynamic power consumption by minimizing the switched capacitance include the designs in [5]–[10]. The design in [5] proposes a concept called partially guarded computation (PGC), which divides the arithmetic units, e.g., adders and multipliers, into two parts and turns off the unused part to minimize the power consumption. The design in [6] proposes a 32-bit 2's complement adder equipping a two-stage (master and slave stages) flip-flop at each of the two inputs, a dynamic-range determination (DRD) unit and a sign-extension (SE) unit, which tends to reduce the power dissipation of conventional adders for multimedia applications. Additionally, the design in [7] presents a multiplier using the DRD unit to select the input operand with a smaller effective dynamic range to yield the Booth codes. However, the DRD unit induces additional delay and area overheads. The design in [8] incorporates a technique for glitching power minimization by replacing some existing gates with functionally equivalent ones that can be frozen by asserting a control signal. This technique can be applied to replace layout-level descriptions and guarantees predictable results. The design in [9] introduces a double-switch circuit-block switch scheme capable of reducing power dissipation during downtime by shortening the settling time after reactivation. The impediments of the scheme are the necessity for two independent virtual power rails and the requirement for two additional transistors for switching each cell. At last,

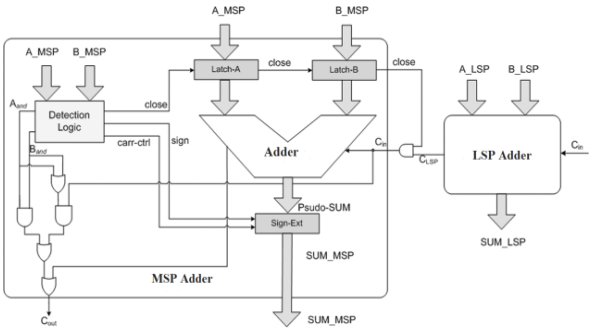

Fig. 2 : Low power adder design adopting proposed RPDT

the design in [10] presents a DCT core exploiting an adaptive bandwidth approach and a method which trades off power consumption and arithmetic precision.

B. *Theoretical Analysis*

To illustrate the reason of those spurious signal transitions, five cases of 16-bit additions as shown in Fig. 1 is explored. The cases of exchanging the operands A and B in additions lead to the same spurious transitions with those shown in Fig. 1. Thus, there is probably no other case beyond these five based on this construction. The first case shows a transient state in which spurious transitions of carry signals generates in the MSP, although the final result of the MSP is the same. At the same time, the second and third cases describe situations involving one negative operand adding another positive operand without and with carry-in from the LSP, respectively. Meanwhile, the fourth and fifth cases demonstrate the addition of two negative operands without and with carry-in from the LSP, respectively. In those cases, the outputs of MSP are predictable; therefore, the computations in MSP are unnecessary and can be avoided. Eliminating those spurious computations not only can save the power consumption inside the adder in the current stage but also can decrease the glitching noises which cause power wastage inside the arithmetic circuits in the next stage.

From the analysis of Fig. 1, the RPDT as shown in Fig. 2 is proposed that separates the adder into two parts and then latches the input data of the MSP whenever they do not affect the computation results. The RPDT can be expanded to be a fine-grain scheme in which the adder is divided into more than two parts. However, the hardware constructional complexity of the augmented circuits such as the detection-logic unit, the data latches, and the SE unit expands dramatically. Based on an adder example, we actually find that the power expense caused by the augmented circuits is larger than the power reduction in a tri partitioned scheme. This is the reason we propose a bi-partitioned RPDT scheme in this paper When the bits in A_{MSP} and/or in B_{MSP} are all ones, the value of A_{and} and/or that of $B_{and,}$ respectively,

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changes to one, while when the bits in A_{MSP} and/or in B_{MSP} are all zeros, the value of and/or that of , respectively, turn into one. Being one of the three outputs of the detection-logic unit,as shown in Fig. 3, *close* denotes whether the MSP circuits can be neglected or not. When the two input operands can be classified into one of the five cases shown in Fig. 1, the value of *close* becomes zero, which indicates that the MSP circuits can be closed to save power dissipation. This design architecture aims to close the MSP circuits by feeding zero inputs into them, which may freeze the switching activities in the MSP circuits to avoid dynamic power consumption. On comparison with the use of transmission gates to latch the inputs, this architectural design can prevent the voltage-drop problems caused by the floating-connected points after the MSP circuits are closed for a relatively long span of time.

The LSP employs a sparse modulo adder shown in Fig. 5 that utilises minimum area and reduced complexity for carry computation as it contributes more for power suppression. This is based on a sparse approach which is enabled by the introduction of the inverted circular idempotency property of the parallel-prefix carry operator and its regularity and area efficiency are further enhanced by the introduction of a new prefix operator, known as gray operator, Fig 6,which requires one extra gate, but does not require extra logic levels. The logic level implementation of the basic cells employed in building the sparse modulo adder is shown in Fig 7. It reduces the area consumed and produces a faster result since the operation is based on a sparse approach.

C. *Modulo 2^n +1 Addition*

Modulo 2^n +1 adders can be designed as a special case of general modulo m adders.

$$S^+ = (A^\star + B^\star) \bmod (2^n + 1)$$
$$= \begin{cases} (A^\star + B^\star + 1) \bmod 2^n, & A^\star + B^\star < 2^n, \\ (A^\star + B^\star) \bmod 2^n, & A^\star + B^\star \geq 2^n. \end{cases}$$

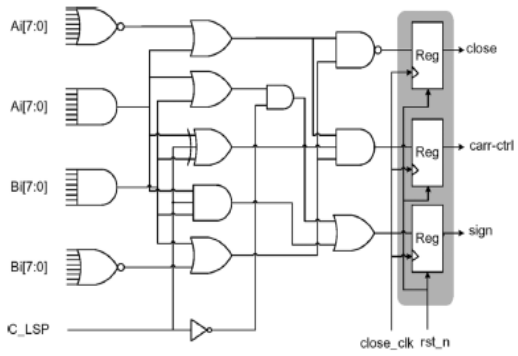

Fig.3 :Detection-logic unit

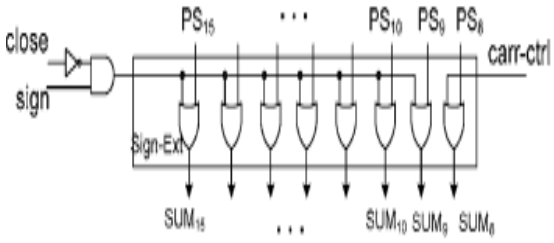

Fig. 4. Sign Extension Unit Using OR gates.

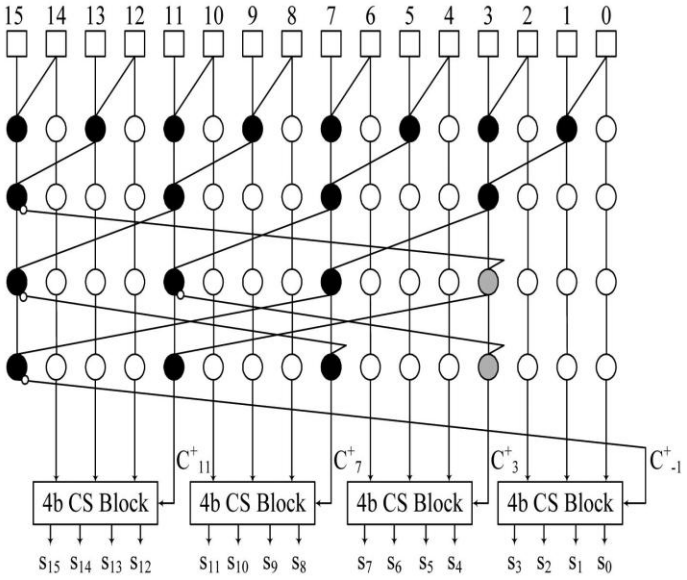

Fig. 5. Sparse-4 modulo 2^{16}+1 diminished-1 Adder used in the LSP of the RPDT

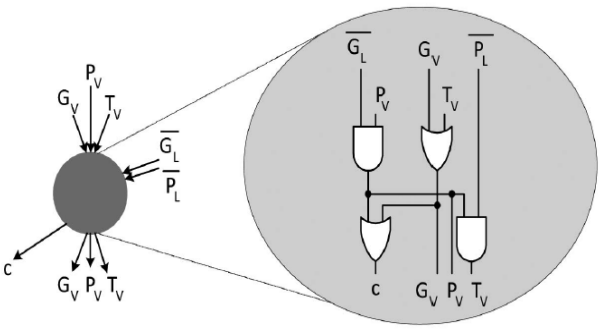

Fig. 6. Notation and implementation of a gray prefix operator

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where A and B are inputs, n represents the bit length of the inputs and A*(B*) represents the diminished-1 representation of A(B).

TABLE I : PERFORMANCE ANALYSIS OF RPDT USING CONVENTIONAL ADDER AND SPARSE MODULO ADDER IN LSP.

Architecture	Delay (ns)	Memory usage (kilobytes)	Peak memory usage	Power(W)	4 input LUTS
RPDT employing conventional adders in MSP and LSP	29.787	194940	269	0.196	118
RPDT employing sparse modulo adder in LSP	21.540	109452	267	0.173	73

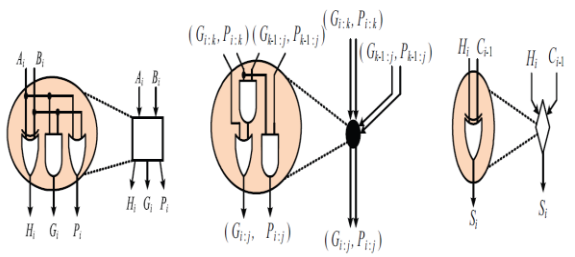

Fig. 7. The logic-level implementation of the basic cells used in parallel-prefix adder.

The diminished-1 representation of binary numbers was introduced to speed up the modulo $2^n + 1$ arithmetic operations. Modulo 2n+1 channel handles n+*1* bit input where as modulo 2n-1 and *2*n type can handle only *n* bit input operands. So, the implementation of modulo 2^n+1 channel is more complicated than 2^n-1 or 2^n type channel. To remove this problem, we use Diminished-one arithmetic. In this approach a number *A*Є (0, 2^n +1) is represented as A−1 = A−1 , while zero is handled separately. Since only *n* bits are required for the representation of any number *A*Є (0, 2^n +1) the diminished-1 representation can lead to implementations with delay and area approaching that of modulo 2^n −1, 2^n.

The parallel prefix adder employs the 3-stage structure. The preprocessing stage computes the carry-generate bits, G_i the carry-propagate bits P_i, and the half-sum bits H_i, for every i,0 ≤ i ≤ n-1, according to

$Gi = Ai .Bi \quad Pi = Ai + Bi \quad Hi = Ai \quad Bi;\oplus$

where .,+ and $\oplus$ denote logical AND, OR, and exclusive- OR, respectively. The second stage of the adder, eventually called the carry computation unit, computes the carry signals Ci, for 0 ≤i ≤ n -1 using vthe carry generate and carry propagate bits G_i and P_i .The third stage computes the sum bits according to

$$Si = Hi \quad C_{i-1} \oplus$$

The betterment is in the carry generation stage which is the most intensive one.

Idempotency Property

$$(G_{i:0}, P_{i:0}) \circ \overline{(G_{n-1:i+1}, P_{n-1:i+1}) \circ (G_{i:0}, P_{i:0})} = (G_{i:0}, P_{i:0}) \circ \overline{(G_{n-1:i+1}, P_{n-1:i+1})}$$

D. OPERATION OF THE RPDT

1) *When the detection-logic unit switches off the MSP:* At this moment, the outputs of the MSP are directly compensated by the SE unit; therefore, the time saved from skipping the computations in the MSP circuits shall cancel out the delay caused by the detection-logic unit.

2) *When the detection-logic unit switches on the MSP:* The MSP circuits must wait for the notification of the detection-logic unit to turn on the data latches to let the data in. Hence, the delay caused by the detection-logic unit will contribute to the delay of the whole combinational circuitry, i.e., the 16-bit adder/subtractor in this design example.

3) *When the detection-logic unit remains its decision:* No matter whether the last decision is turning on or turning off the MSP, the delay of the detection logic is negligible because the path of the combinational circuitry (i.e., the 16-bit adder/subtractor in this design example) remains the same.

III. EXPERIMENTAL RESULTS

The experimental results obtained from Xilinx 12.3i with VHDL coding with SPARTAN 3E XC3S1600E

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fixed as target device indicate that the proposed architecture heavily outperforms the earlier solutions in implementation thus reducing area from 118 LUTs to 73 LUTs while offering a high execution rate in a comparatively less time of 21.540ns. Table I show the area and timing analysis of the proposed architecture with the existing one and it is clear that the proposed architecture consumes less hardware due to the elimination of double operators and less wiring complexity.

IV. CONCLUSION

The low power technique called RPDT decreases the switching or dynamic power which contributes a significant portion of the whole power dissipation in integrated circuits. The obtained data reveal that the proposed power downgrading technique offer a higher operation speed consuming less power than those of [5]. Employing adders of [11], [12] consumes more power that can be reduced by using the proposed sparse modulo adder. Table I compares the performance of the proposed power downgrading technique using a low power, high speed sparse modulo adder and a conventional adder and its seen that it reduces the memory usage, power and area utilized for operation.

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