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FPGA Implementation of FIR based Decimation Filter Structure for WiMAX Application

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Abstract: This paper presents the implementation of two stage FIR (Finite Impulse Response) decimation filter using system generator and it is compared with single stage implementation of FIR filter for WiMAX Application. FIR filter with decimation factor M is subdivided into two decimation factors M_1 and M_2. The two different FIR filters are designed with different coefficient values and different sampling rate and cascaded instead of single stage FIR filter. The prototype is designed with MATLAB Simulink model and it is converted to VHDL code using Xilinx system generator. Prototype is implemented in Virtex V- FPGA kit and simulation results and device utilization reports are generated and tabulated. The result shows that the two stage FIR filter utilizes less LUT's and consumes less power than the single stage FIR filter. This low power implementation of two stage FIR filter may be used as a decimation filter in WiMAX application.

Keywords: Decimation, FIR – Finite Impulse Response Filter, SRC- Sampling Rate Conversion, DDC – Digital Down Converter, FPGA – Field Programmable Gate Array

I. INTRODUCTION

WiMAX is a wireless data communication technology, based on IEEE 802.16 standard providing high speed data over a wide range. The WiMAX stands for World Wide Interoperability for Microwave Access and it is a technology for point to multipoint wireless networking. WiMAX technology expected to meet the needs of a large variety of users from those in developed nations wanting to install a new high speed data network very cheaply without the cost and time required to install a wide network, to those in rural areas needing fast access where wired solutions may not be viable because of distance and cost involved. Additionally it is being used for mobile applications, providing high speed data to users on the move.

Table 1: WiMAX Specifications and Filter Design Parameters

Frequency range (GHz)	10-66
Channel Spacing (MHz)	20
Symbol rate / Chip Rate	16.704 Symbols/sec
Over sampling ratio(OSR)	8
Input sampling frequency F_s (MHz)	133.632
Pass band Edge (MHz)	8
Stop band Edge (MHz)	10
Pass band ripple (MHz)	0.5
Stop band attenuation (dB)	39

In this paper the designing of the decimation filter for WiMAX standard as per the specifications mentioned in the table 1 is presented. The sampling rate reduction is required for WiMAX is 8, which is realized with two stage realization techniques. It improves the passband and stopband attenuation effectively and reduces the complexity, device utilization and power consumption as compared to single stage realization. Hence this paper presents the implementation of single stage FIR filter and two stage FIR filter for decimation process.

In recent years, with the rapid development of VLSI (Very Large Scale Integration) technologies, FPGA (Field Programmable Gate Array) has been widely applied in the field of digital signal processing, because of its reprogrammability, reconfigureability, low cost, high logic density and high reliability. Sample rate conversion (SRC) is the process of changing sampling rate of data stream from a specific sampling rate to another sampling rate. With the conversion of communication and software market SRC is a necessary component in many of today's applications, like CD, Audio players, Multitask Digital audio workstations, Tape recorders, computer communication, etc.

In most of these applications, very high quality sample rate converter is required. Most high quality SRCs currently available in the market employ a digital filter that provides the required quality by upsampling the data to a very high sampling rate followed by down sampling to the required output sampling rate. The digital filters

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used in the SRC are the strong options for removing noise, shaping spectrum and minimizing Inter Symbol Interference (ISI) in communication system. The FIR filter is one which has narrow passband and more stopband attenuation.

In 1973, McClellan, et al., [1] have developed a computer program to design an optimum FIR linear phase digital filter. The program has options for designing standard filters as low-pass, high-pass, band-pass and band-stop filters. The program is also used to design filters with arbitrary frequency specifications which are provided by users. This program is written in FORTRAN. Bellanger, et al., G [2] have designed a polyphase network structure. It permits the use of recursive devices for efficient sample-rate alteration. The comparison with conventional filters shows that with the same active memory, a reduction of computation rate approaching a factor of 2 can be achieved when the alteration factor increases.

Saramäki, T [3] has discussed a linear phase characteristics of a FIR filter for interpolation and decimation. Characteristics of the new filters like zero positions, coefficient of sensitivity and output noise variance due to round off errors are compared with conventional FIR designs. It was proved that cascading multistage new decimators and interpolators will provide narrow-band filters requiring considerably fewer multiplications per output sample with equivalent elliptic design. Ramstad. T.E and Saramäki [4] have presented about the filter system which is capable of implementing virtually any practical low-pass and high-pass filter which uses 50-60 multiplications per sample. The method works with multirate techniques and complementary filters.
Gustafsson, et al., [5] have implemented the polyphase decomposed FIR filters using MCM techniques which uses a number of constant multiplications using minimum number of adders and subtracters. For interpolations, direct form subfilters lead to fewer registers as the shared structure of subfilters. But in a transposed direct form subfilters the registers cannot be shared. For decimation filters the opposite holds for direct form and transposed direct form subfilters. Finally implementation results for area, speed, and power for different realizations are compared. In [6] a polyphase multistage FIR filter with memory saving structure has been studied. The structures are implemented with help of Xilinx system generator.

Suvarna Joshi and Bharati Ainapure, [7] implemented basic FIR filter structure with the help of FPGA platform. The MATLAB FDA Tool has been used to determine the filter coefficients and 4th order 32 bit filters has been prototyped. The design has been prototyped on XC3S500-4FG320 in Spartan-3E platform using ISE 9.1/10.1 Xilinx platforms. Kristin Scholfield and Tom Chen, [8] presented low power design of a decimator for a sigma-delta ADC for biomedical applications in commercial 0.18µm CMOS process. Two features help make the design low power: use of bit-serial architecture and use of an ultra-low supply voltage of 0.9V in a 0.18µm CMOS design. Muhammad Ali Siddiqi Nabeel Samad and Faheem Sheikh [9], paper presents a practical implementation of multistage sample rate conversion in multistandard software radios. This implementation is done on Xilinx Virtex-II Pro FPGA board.

The paper is organized as follows. The section II describe the basic FIR filter structure, section III describe two stage FIR filter structure, section IV describe the FPGA design for FIR filter structure, section V describe simulation and synthesis results and section VI describe conclusion.

II. FIR FILTER STRUCTURE

The non-recursive nature of FIR filter [7] offers the opportunity to create implementation schemes which significantly improve the overall efficiency of the decimator. Consider the factor M-decimator of which uses a FIR antialiasing filter with the impulse response h[n]. The time domain relation for the filter are expressed by the convolution sum,

$$v[n] = \sum_{k=0}^{N-1} h[k]\, x[n-k] \qquad (1)$$

Where N is the order of the filter.

The decimated signal y[m] is obtained after applying down sampling which is given by,

$$y[m] = \sum_{k=0}^{N-1} h[k]\, x[nM-k] \qquad (2)$$

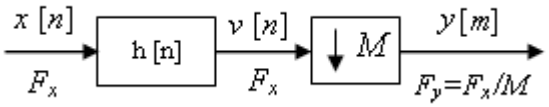

Fig. 1 Factor of M-decimator with FIR filter

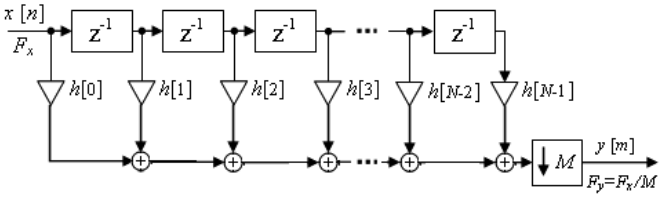

Fig. 2 Direct Implementation of factor-of-M decimator

III. TWO STAGE FIR FILTER STRUCTURE

To decrease the multiplication rate of the sampling rate in the FIR filter structure, the decimation factor M is sub divided into M_1 and M_2 and implemented using two stages

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FIR filter structure with different co-efficient values and sampling rates. The first FIR filter decimation factor is M_1, and the second filter decimation filter is M_2 to form two stage. Fig. 3 and 4 shows the two stages and single stage implementation for the decimation factors respectively.

Two stage implementation for $M = M_1 * M_2$

Efficiency of $H_1(z)$ is given

$$Rm\_dec\_H_1 = N_1 * F_{y1} = N_1 * F_x / M_1 \quad (3)$$

$$Rm\_dec\_H_2 = N_2 * F_{y2} \quad (4)$$

The total multiplication rate of two stage decimation is

$$Rm\_dec = Rm\_dec\_H_1 + Rm\_dec\_H_2$$

$$Rm\_dec = N_1 * F_{y1} + N_2 * F_{y2} \quad (5)$$

Where,

N_1 is order of the First Stage FIR Filter

N_2 is order of the Second Stage FIR Filter

$Rm\_dec\_H_1$ is Multiplication rate of First Stage

$Rm\_dec\_H_2$ is Multiplication rate of Second Stage

Rm_dec is the Total Multiplication rate of FIR Filter

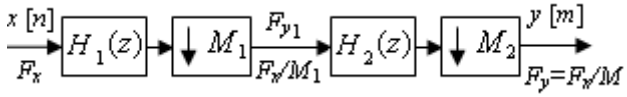

Fig. 3 Two stage implementation for $M = M_1 * M_2$

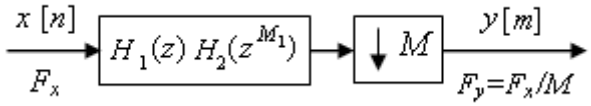

Fig. 4 Single stage equivalent for M

IV. FPGA DESIGN FOR FIR FILTER

The recent advancement in the VLSI technology particularly in FPGA as made possible, the realization of advanced Digital Signal Processing algorithm in high frequency domain. With this development a single chip solution is possible for complex DSP based applications like, ADC, Decimation and Interpolation in the communication system. Digital implementation couples with signal processing algorithms greatly enhance the system performance, reduced the cost and increase the reliability of the system. Low power DSP systems are implemented by changing the sampling clock for each subsystem depending on the real requirements. The sampling rate change results in aliasing; this necessitates the use of filters to overcome it.

The initial model was designed and tested in Simulink, a software package from The Mathworks for modeling, simulating and implementing the dynamic systems. The figure 6 and 7 shows the Simulink model of the single stage and two stage FIR Filter structures respectively for the decimation factors M=6 and M=8.

This Simulink model is used as the reference model for synthesis of the design in FPGA. To implement t the module on FPGA, the Xilinx System Generator is used, which provide a Simulink blockset that is converted to VHDL for synthesis and implementation. This VHDL generation flow is shown in fig. 5

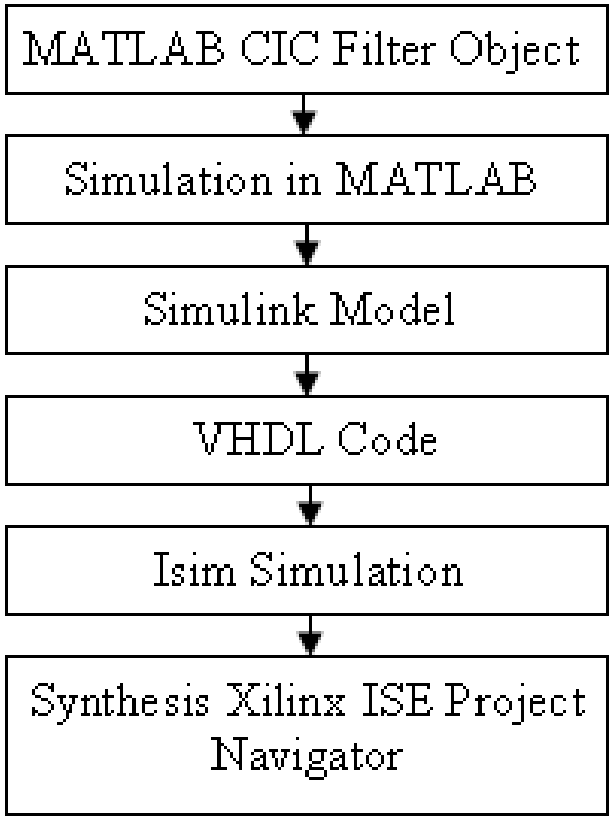

Fig. 5 FPGA Synthesis Flow

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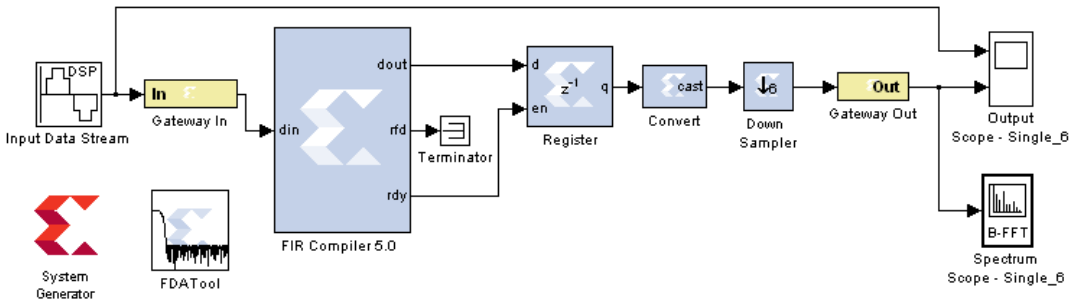
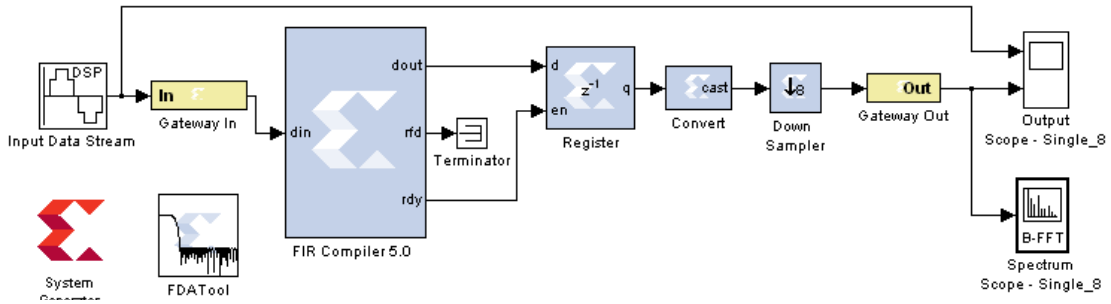
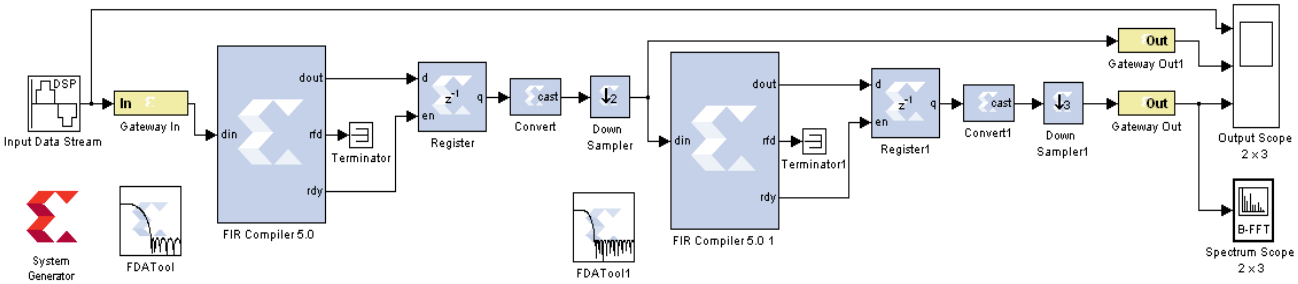


(a) Realization of single stage FIR Filter Structure for M=6

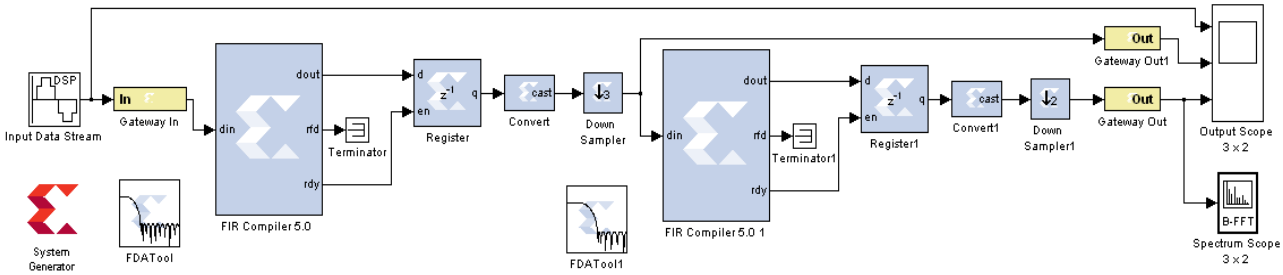


(b) Realization of single stage FIR Filter Structure for M=8

Fig. 6 Implementation structure for Single Stage FIR Filter



(a) Realization of two stage FIR Filter Structure for M=6 with M_1=2 and M_2=3



(b) Realization of two stage FIR Filter Structure for M=6 with M_1=3 and M_2=2

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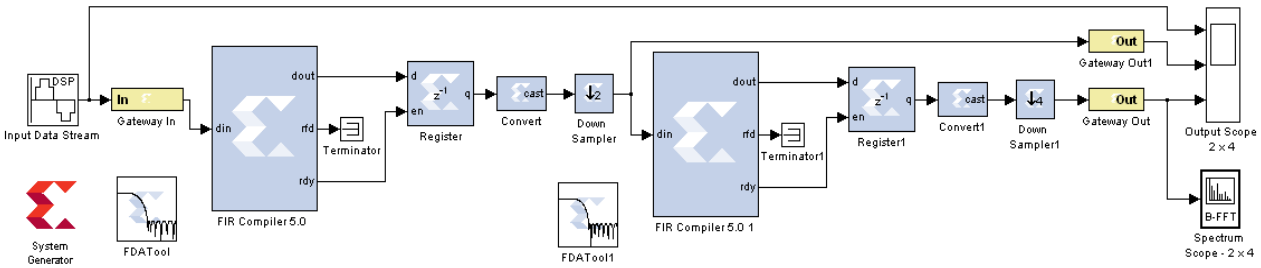
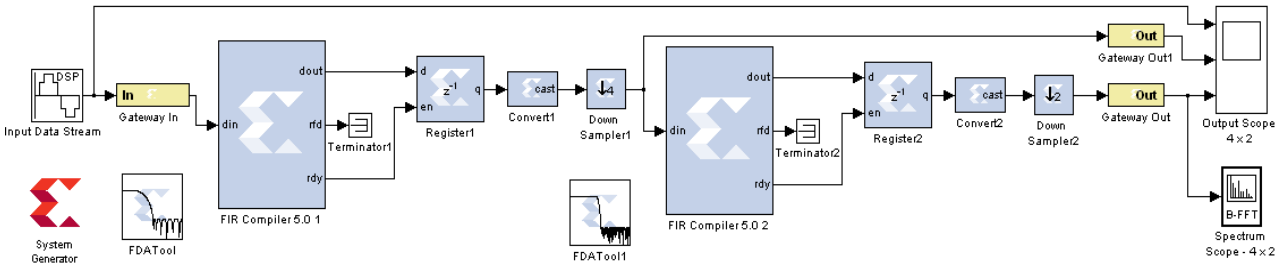


(c) Realization of two stage FIR Filter Structure for M=8 with M_1=2 and M_2=4

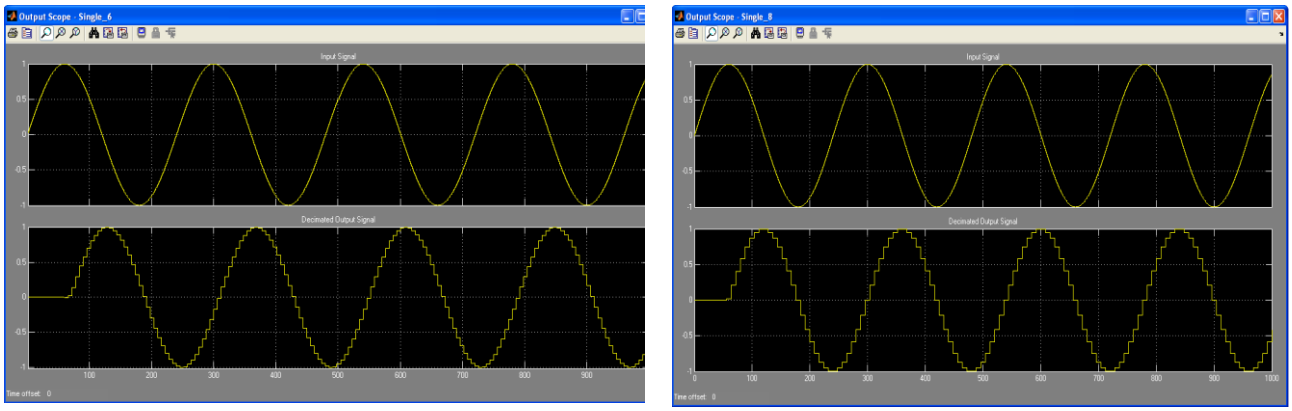


(d) Realization of single stage FIR Filter Structure for M=8 with M_1=4 and M_2=2

Fig. 7 Implementation structure for Two Stage FIR Filter

V. SIMULATION AND SYNTHESIS RESULTS

Figure 6 shows the Simulink model for single stage FIR filter for decimation factor M=6 and M=8. Figure 8 shows the simulation result of the single stage FIR filter structures. Figure 7 shows the two stage FIR filter structures with different combinations for the decimation factor M=6 and M=8 and figure 9 shows simulation result of two stage FIR filter structures. Table I and Table II shows the power consumption and device utilization summary for different FIR Filter structures respectively. Figure 10 and 11 shows device utilization and power consumption comparison between different FIR Filter structures for the decimation factor M=6 and M=8.



(a) Scope output of Single stage FIR Filter for M=6

(b) Scope output of Single stage FIR Filter for M=8

Fig. 8 Simulation Results of Single Stage FIR Filter

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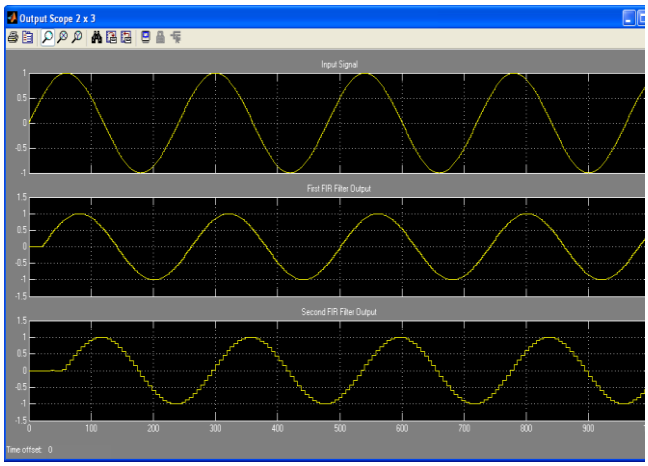
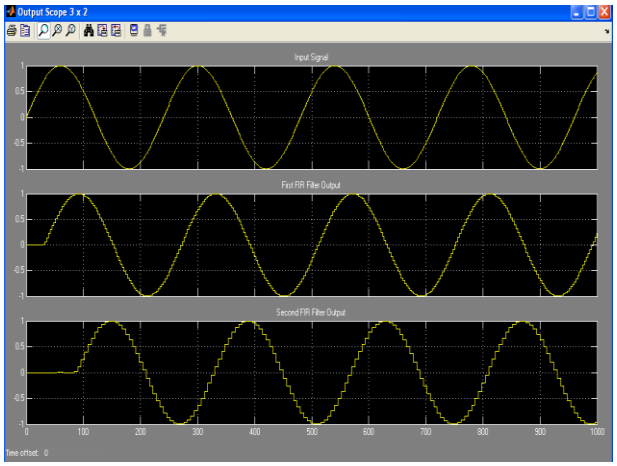
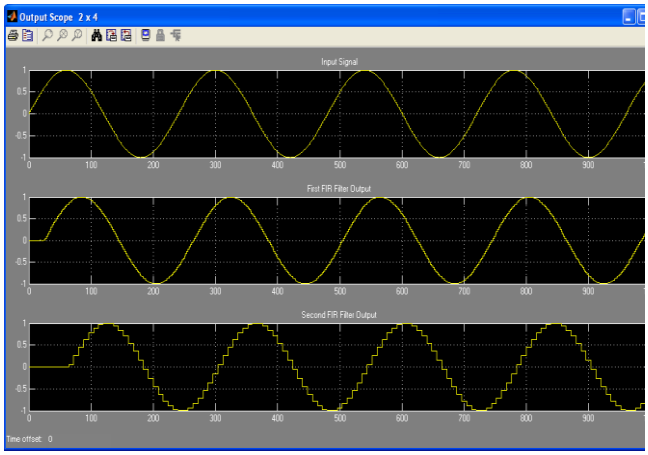


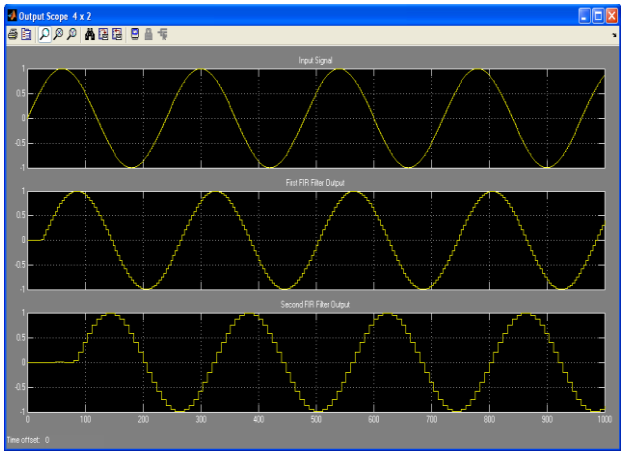
(a) Scope output of two stage FIR Filter for M_1=2 and M_2=3 (M=6)



(b) Scope output of two stage FIR Filter for M_1=3 and M_2=2 (M=6)



(c) Scope output of two stage FIR Filter for M_1=2 and M_2=4 (M=8)



(d) Scope output of two stage FIR Filter for M_1=4 and M_2=2 (M=8)

Fig. 9 Simulation Results of Two Stage FIR Filter

Table I Power Consumption Summary

Filter Structure	Decimation Factor	Power Consumption in Watts			Decimation Factor	Power Consumption in Watts		
		Quiescent	Dynamic	Total		Quiescent	Dynamic	Total
Single Stage FIR	M = 6	1.189	0.156	1.345	M = 8	1.19	0.219	1.409
Two Stage FIR	M_1 = 3 and M_2 = 2	1.188	0.106	1.294	M_1 = 4 and M_2 = 2	1.189	0.158	1.347
	M_1 = 2 and M_2 = 3	1.188	0.071	1.259	M_1 = 2 and M_2 = 4	1.189	0.069	1.258

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Table II Device Utilization Summary

(a) Device utilization summary for the Decimation filter structures with M=6

Device	Available	Single Stage FIR		Two Stage FIR			
		M = 6		M_1 = 3and M_2 = 2		M_1 = 2 and M_2 = 3	
		Used	Utilization	Used	Utilization	Used	Utilization
Number of Slice Registers	69120	1980	3%	2033	3%	1417	2%
Number of Slice LUT's	69120	2142	3%	1162	2%	935	1%
Number of LUT Flip Flop pairs used		2289		2134		1512	
Number of Bonded IOB'S	640	41	6%	41	6%	41	6%
Number of DSP48E's	64	30	47%	16	25%	12	19%

(b) Device utilization summary for the Decimation filter structures with M=8

Device	Available	Single Stage FIR		Two Stage FIR			
		M = 8		M_1 = 4 and M_2 = 2		M_1 = 2 and M_2 = 4	
		Used	Utilization	Used	Utilization	Used	Utilization
Number of Slice Registers	69120	2931	4%	2666	4%	1423	2%
Number of Slice LUT's	69120	3613	5%	1661	2%	934	1%
Number of LUT Flip Flop pairs used		3778		2773		1510	
Number of Bonded IOB'S	640	41	6%	61	10%	41	6%
Number of DSP48E's	64	45	70%	24	38%	12	19%

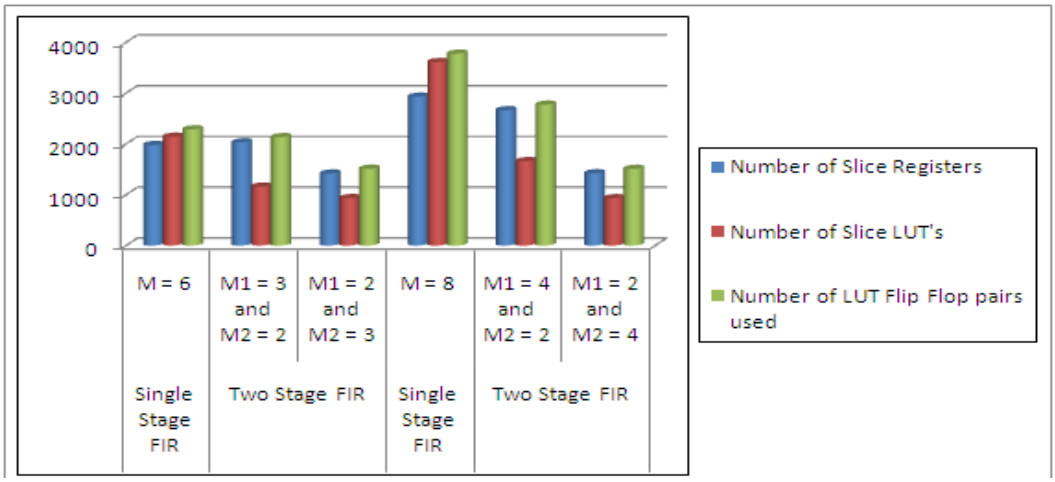

Fig. 10 Resource Utilization Comparison Chart between different Filter structures

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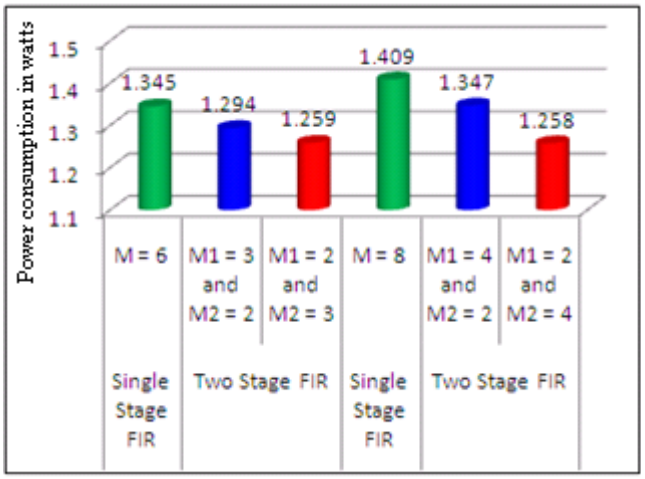

Fig. 11 Power consumption Comparison Chart between different Filter structures

VI. CONCLUSION

The single and two stage FIR filter is implemented with the help of Virtex-V FPGA kit and the simulation results are taken for different decimation factors M=6 and M=8 and the results are tabulated. Compare to single stage FIR filter structures, two stage FIR filter structures consume less power and utilize`` less LUTs. The order of the filter and coefficient of FIR Filter is estimated using FDA Tool. For the Decimation factor M=6; single stage FIR Filter, the estimated order is 59 and for Two Stage FIR filter the First Stage Filter order is 13 and the Second Stage is 29 for decimation factor M_1 = 2 and M_2 = 3 and for the Decimation factor M=8; single stage FIR Filter, the estimated order is 91 and for Two Stages FIR filter, the First Stage Filter order is 13 and the Second Stage is 45 for decimation factor M_1 = 2 and M_2 = 4. This low power design of FIR filter structure is best suited for any wireless application. For decimation factor M=8, is used in WiMAX.

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Biography

V.Jayaprakasan received his Bachelor's Degree in Electronics and Communication Engineering from Bharadhidasan University, Tiruchirappalli, India in the year 1999 and Master's Degree in Communication Systems from Anna University, Chennai, India in the year 2006. He has started his teaching profession in the year 2006 in Ganadipathy Tulsi's Jain Engineering College, Vellore. Earlier he has 11 years industrial experience in an electronics based industry. At present he is a Professor in Electronics and Communication Department. He has published 1 research paper in International Journal. He is a part time research scalar in Jawaharlal Nehru Technological University Anantapur. His areas of interest are Wireless communication, Networking and Signal Processing. He is a life member of ISTE.

M.Madheswaran received the BE Degree from Madurai Kamaraj University in 1990, ME Degree from Birla Institute of Technology, Mesra, Ranchi, India in 1992, both in Electronics and Communication Engineering. He obtained his PhD degree in Electronics Engineering from the Institute of Technology, Banaras Hindu University, Varanasi, India, in 1999. At present he is a Principal of Muthayammal Engineering College, Rasipuram, India. He has authored over one hundred and twenty five publications in international and national journals and conferences. Currently he is the chairman of IEEE India Electron Devices Society Chapter and Vice Chair of IEEE India Circuits and System Chapter. He was awarded the Young Scientist Fellowship (YSF) by the State Council for Science and Technology, Tamilnadu, in 1994 and Senior Research Fellowship (SRF) by the Council of Scientific and Industrial Research (CSIR), Government of India in 1996. Also he has received YSF from SERC, Department of Science and Technology, Govt. of India. He is a fellow of IETE and IE (India), life member of ISTE and also a senior member of IEEE. He is also the member of International Association of Computer Science and Information Technology (IACSIT) Singapore.