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Recovery Boosting Technique for Improving NBTI Recovery in SRAM Arrays

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Abstract- Negative bias temperature instability (NBTI) is an important Lifetime reliability problem in microprocessors. In order to overcome this problem many techniques has been initialized but all those results in Time delay and Instability that affects the performance of micro processors adversely, actually the Recovery boosting techniques and stress bias techniques are used for solving the performance problems. In this project a basic 6T SRAM is taken for the testing. SRAM is comprised of PMOS and NMOS, PMOS create the problem of NBTI as it is less stabilized in normal recovery boosting techniques an extra inverter is added and the output will be noted , by this process the NBTI reduced but that results in increased power and delay of the SRAM, this affects the performance of SRAM. In Fine Grained recovery boosting an extra PMOS inverter is added to this normal circuit while checking the circuit showed better power , delay and resistance to NBTI. After that 4T SRAM array is constructed. After that a memory system is designed.

Keywords : NBTI, PMOS, NMOS, SRAM, Fine Grained recovery boosting

I. INTRODUCTION

Computers and many electronic gadgets usually rely on stored information which is mainly data which can be used to direct circuit affections. The digital information is stored in memory devices. There are two types of memories based on what memory cells can be accessed at a given instant. SAM (Sequentially Access Memory) is accessed by stepping through each memory location until the desired location is reached. Magnetic tape is an example of SAM. The second category of memory devices is called RAM (Random Access Memory) where the memory can be randomly accessed at any instant. Compared to SAM the access time is to be faster. Most of the electronic gadgets memories are of RAM type.

One important hard error phenomenon is negative bias temperature instability (NBTI), the lifetime of the pMOS transistor is affected. NBTI occurs when a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor. The negative bias can lead to the generation of interface traps at the Si/SiO2. Interface, which cause an increase in the threshold voltage of the device. This increase in the threshold voltage degrades the speed of the device and reduces the noise margin of the circuit. One interesting aspect of NBTI is that some of the interface traps can be eliminated by applying a logic input of "1" at the gate of the pMOS device. This puts the device into what is known as the recovery mode. Memory arrays that use static random access memory (SRAM) cells are especially susceptible toNBTI. SRAM cells consist of cross-coupled inverters that contain pMOS devices. Since each memory cell stores either a "0" or a "1" at all times, one of the pMOS devices in each cell always has a logic input of "0." All modern processor cores are composed of several critical SRAM-based structures, such as the register file and the issue queue, so there is an important impact of NBTI on these structures to maximize their lifetimes.

II . OVERVIEW OF NBTI

At the time of oxidation of silicon, most of the Si atoms at the surface of the wafer bond with oxygen while a few atoms bond with hydrogen. When a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor (V_{gs}=-V_{dd}), the relatively weak Si-H bonds get disassociated, leading to the generation of interface traps at the Si/SiO2 interface. These interface traps cause the threshold voltage (V_t) of the pMOS increase, which in turn degrades the speed of the device and the noise margin of the circuit, eventually causing the circuit to fail. The period of time when the pMOS transistor is negatively biased is known as the stress phase or stress mode.

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$$\Delta V_{ts} = \left(\frac{qt_{ox}}{\varepsilon_{ox}}\right)^{3/2} \cdot K_1 \cdot \sqrt{C_{ox}(V_{gs} - V_t)} \cdot e^{-E_a/4kT + 2(V_{gs} - V_t)/t_{ox}E_{01}} \cdot T_0^{-0.25} \cdot t_{stress}^{0.25} \quad (1)$$

Where t_{stress} is the time under stress, t_{ox} is the oxide thickness, and C_{ox} is the gate capacitance per unit area.K1,Ea,T0,E01 and K are constants equal to 7.5 C^-0.5 nm , 0.49 eV,10^-8 s/nm , 0.08 V/nm, and 8.6174*10^-5 eV/K, respectively. When a logic input of "1" is applied at the gate, the transistor turns off eliminating some of the interface traps. This is known as the recovery phase or recovery mode.

$$\Delta V_t = \Delta V_{ts} \cdot \left(1 - \frac{2\xi_1 t_{ox} + \sqrt{\xi_2 e^{-E_a/kT} T_0 t_{rec}}}{(1+\delta)t_{ox} + \sqrt{e^{-E_a/kT}(t_{stress} + t_{rec})}}\right) \quad (2)$$

Where t_{rec} is the recovery time E2, E1 and d are constant equal to 0.5, 0.9, and 0.5 respectively. From the equations, one can observe for reducing the impact of NBTI. We can see that NBTI is affected by temperature, the stress and recovery times and the difference between V_{gs} and V_t . Reducing Vgs, temperature, the stress time and increasing V_t can reduce the stress on the transistors whereas longer recovery times recovery process. By using a lower V_{gs} can reduce performance. Although a higher V_t device is likely to be more resilient against NBTI, such devices are slower than their lower V_t.

III. SOLUTIONS FOR NBTI

There are two basic solutions for NBTI:

1) Reduce the stress on the pMOS transistors
2) Enhance the recovery process.

Stress reduction techniques aim to reduce the aging rate by controlling V_{dd}, V_t and temperature. And recovery enhancement techniques aim to increase the recovery time for the pMOS devices. Recovery boosting is a recovery-enhancement technique for SRAM structures.

A. Stress Reduction Technique

Stress reduction technique shows that aging mechanisms at runtime based on the operating conditions and use dynamic reliability management (DRM) to stay within the reliability budget. The use of stress reduction techniques is orthogonal to the use of recovery enhancement. Stress reduction techniques aim to reduce the aging rate by controlling V_{gs}, V_t and temperature. The another technique is recovery enhancement technique.

B. Recovery Enhancement Technique

In these devices is used to increase the recovery time for pMOS transistors in logic structures during idle periods and balance the degradation of the pMOS devices in SRAM-based memory structures when they hold invalid data. In this technique to periodically flip the contents of SRAM cells to balance the wear on the pMOS transistors. Recovery enhancement technique for caches where SRAM cells are put into the recovery mode. They reverse bias the pMOS devices to put them into a deep recovery state. When an array is put into the recovery mode, all the pMOS devices in any one of the inverters in all of the cells are put into the recovery mode followed by those in the other array. All of these recovery enhancement techniques aim to balance the degradation of the two pMOS devices in the memory cell by attempting to keep the inputs to each device at a logic input of "0" exactly 50% of the time.

In recovery boost mode, one of the devices is always negative biased condition. And also to connect the one of the inverter. The input of the inverter is to be "0 "and the output of the inverter is "1".With this we can find out the recovery boost mode condition. Due to the power and delay problem we go for Fine Grained Recovery Boosting. In this recovery boosting, we have to add two extra pMOS transistors which is connected to V_{dd}. And the output of the inverter is connected to ground of the SRAM cell i.e., V_{dd}. In Recovery Boosting technique that allows both pMOS devices in the memory cell to be put into the recovery mode by slightly modifying to the design of conventional SRAM cells. In this we have to found the circuit-level design of a physical register file and an issue queue that use such cells through SPICE-level simulation. After that we perform the architectural simulation.

IV. BASICS OF RECOVERY BOOSTING

6T SRAM cell is composed of a word line (WL),a pair of bitline(BL,BLB),two cross coupled inverters(I0,I1) and two access transistors. The cross coupled inverters store one bit of data. There are three basic operations such as read, write and hold. To read and write the data ,the cell is selected by raising WL to high. This activate the access transistors and connect the inverters in the cell to the bitlines. During the read operation ,both the bitlines are precharged high. Based on the data present in the cell, any one of the bitlines is discharged. Sense amplifier is used to detect the change to

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determine the value stored in the cell. During the write operation, one of the bitline is raised high and other is lowered depending the value to be written to the cell. When the cell is not selected(WL=0) for read or write, there is an expectation to hold the data stored in it. It is always to operate in the recovery boost mode.

The SRAM cell has cross coupled inverters. Each inverter charges the gate of the pMOS or nMOS devices of other inverter. At any given time one pMOS device will always be in stress mode. The goal of recovery enhancement is to put the pMOS devices into the recovery mode by feeding input values to the cell that will transition them into that mode. However, due to the cross-coupled nature of the inverters, only one of the pMOS devices can be put into the recovery mode. Therefore, previously proposed recovery-enhancement techniques attempt to balance the wearout of the two pMOS devices by putting each pMOS into the recovery mode 50% of the time by feeding appropriate input values.

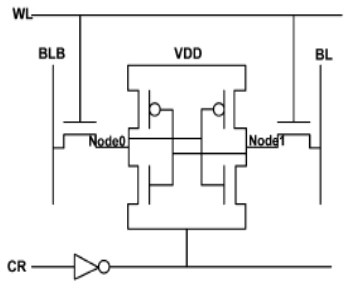

Fig 1 Modified SRAM cell that support Recovery Boosting

The basic idea behind recovery boosting is to raise the node voltages of a memory cell in order to put both pMOS devices into the recovery mode. This can be achieved by raising the ground voltage to the nominal voltage through an external control signal. The modified SRAM cell has the ground connected to the output of an inverter. CR is the control signal to switch between the recovery boost mode and the normal operating mode. During the normal operating mode, CR has a value of "1"(V_{dd}), which in turn connects the ground of the SRAM cell to a value of "0." Then the SRAM cell can perform normal operations of read, write, and hold. To apply recovery boosting, CR has to be changed to a "0" in order to raise the ground voltage of the SRAM cell to V_{dd} .

This circuit configuration puts both pMOS devices in the SRAM cell into the recovery mode. A cell can be put into the recovery boost mode whether its word line (WL) is high or low. The read and write operations on a cell, putting a cell into the recovery boost mode does not require an access to its word line. The drawback of this approach is that it can take a long time to raise both the node voltages to in a high-performance processor that operates at a high clock frequency. Our goal is to be able to switch between the recovery boost mode and the normal operating mode within a single cycle which is critical for a high-speed SRAM structure, where instructions need to be woken up and selected within a single clock cycle, in order to expedite the execution of dependent instructions. The Recovery Boost mode is applied when an entry of the structure holds data that is considered "invalid" at the architecture-level. The high-speed structures change their status between valid and invalid very fast. Consider an example, we find from architecture simulations that an issue queue entry stays invalid for about 50 cycles before it changes its status to valid. In such scenario, the modified SRAM will take 20cycles of the 50 cycles (40% of the invalid period) to shift between modes, given that shifting to the normal operating mode takes place during the end of the invalid period. Thus, only 30 cycles could be utilized for the recovery process.

If extra cycles are allocated to shift to the normal operating mode after the invalid period, which would have negative consequences on the processor performance. Therefore, single-cycle switching is required for the high-speed structures in the processor for the maximum utilization of the invalid states for the recovery process without any performance loss. Such single-cycle switching can be achieved by raising the bitlines along with the ground voltage is connected to V_{dd}. The several ways of incorporating such cells into SRAM arrays are present. Recovery boosting can be provided at a fine granularity. In the normal operating mode, the state of the bitlines change during read and write operations. Since a pair of bitlines is shared by all the memory cells in a given column in the array, those memory cells that are not being read from or written to will have the voltage on their bitlines is to be changed. The ordinary SRAM array, these bitline transitions do not affect the normal operation of the cells. To perform recovery boosting of a memory cell, both bitlines of the cell need to be raised to V_{dd}. So we can able to isolate the bitlines of the memory cells that are in the recovery boost mode from the bitlines that are used for accessing other cells in the array.

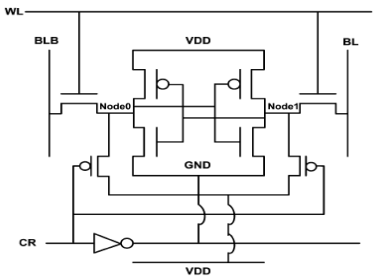

Fig 2 Block Diagram for Fine Grained Recovery Boosting

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V. FUNCTION OF FINE GRAINED RECOVERY BOOSTING

In this Fine Grained Recovery Boosting CR signal serves as the modified SRAM cell function. When a value of "0" is input to the CR line to transition the cell into the recovery boost mode, for raising the ground voltage, the two extra pMOS devices connected to the rail are also turned on. Therefore, by raising the ground and connecting the bitcell to , the cell can be transitioned into the recovery boost mode without affecting cells in other rows of the array.

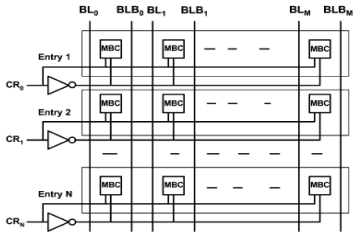


Fig 3 SRAM array with Modified cell

MBC-MODIFIED BIT CELL

A. *Power And Delay Calculation*

If the extra pMOS devices resilient against NBTI by using high Vt- transistors. Although high-Vt devices are slower, these devices are used only when transitioning the cell into the recovery boost mode and not when transitioning to the normal operating mode. These devices do not affect the performance but may delay the transition into the recovery boost mode. Since these devices do not lie on the performance critical path, they are sized so as to minimize the overall area. However, the pMOS devices do consume leakage power. The power consumption of SRAM varies widely depending on how frequently it is accessed it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. The static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption.

VI. SIMULATION RESULTS

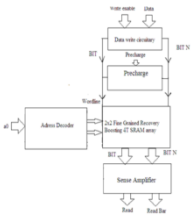
A. *Operation Of Basic 6T SRAM write*

Write operation performs the charging and discharging of the cell nodes. Here WL is the word line and BL is the bit line. WL is used to control the two access transistors. BL is used to transfer data for both read and write operation. It have two bit lines. Both the signal and its inverse are provided in order to increase the noise margin. In case of writing logic 1 to a 6T SRAM cell. We need to keep the bit line increase. Which in turn transfer to the cross coupled inverters and get stored there. Similarly logic 0 is stored to the 6T SRAM cell we need to keep the bit line increase. Which in turn transfer to the cross coupled inverters and get stored there.

B. *Modified 6T SRAM read Operation*

In this modified 6T SRAM cell we have to add an extra inverter. In this inverter cr is the control signal. In normal SRAM cell input of the control signal is 1. But in the case of Recovery boosting we have to add the control signal as 0.So we get the output as 1.With this we can find out the read and write operation. In this Fine Grained Recovery boosting cr,wl,q and qbar are the inputs and the b and bbar is the outputs are the outputs. Here we have to add two extra pMOS transistors and an inverter. Here also we give the input of the control signal as 0.So we get the output as 1. In this also wl,cr,b and bbar are the inputs and the q and qbar are the output for the write operation.After that 4T sram array was constructed and comparing to 6T fine Grained Recovery Boosting and 4T Fine Grained Recovery Boosting.As a result we get as 4T Fine Grained Recovery Boosting is better. Because in 4T SRAM the delay is to be decreased.

C.*A Memory System*



After the completion of 4T SRAM Fine Grained Recovery Boosting a memory system is constructed.It consist of precharging circuit,data write circuitary, decoder, Fine Grained Recovery Boosting array and sense amplifier. The Precharge Circuit is used to precharge the bit-lines, BIT and BITN, to logic 1 value during inactive state of memory cell. When memory cell is being written/ read, precharging is deactivated. The Data Write Circuit is used to write data and its complement onto the bit-lines. Writing a value into the SRAM cell is done by forcing one of the bit lines (BIT/BITN) high while keeping the other low. To write a „1" into the SRAM cell, the word line (WL) is Asserted, bit line BIT is made high and bit line BITN is made low. To write a 0 into the SRAM, bit line BIT is made low and BITN is made high. Before reading from the SRAM cell both bit lines (BIT, BITN) are pre-charged high and SRAM cell is selected. When WL selects the SRAM cell to be read, depending on the data in the SRAM cell, one of the bit lines is pulled down. If BIT is pulled down the stored data is 0. If

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BITN is pulled down the stored data is 1. Sense amplifiers are used to sense which line is being pulled down and perform the read operation of the stored data. READ and READ_BAR indicate the data stored and its complement during the read operation.

D.Waveforms

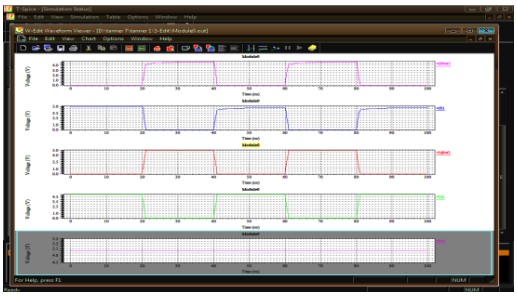

Fig a.Wave Form for 6T SRAM Recovery Boosting

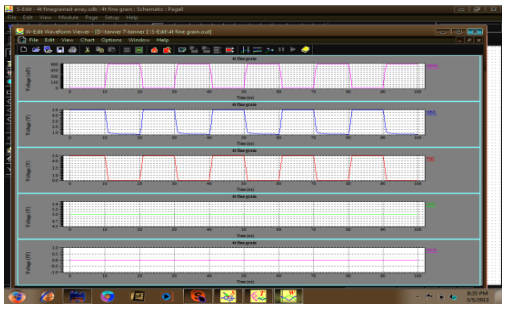

Fig b. 4T SRAM Fine Grained Recovery Boosting

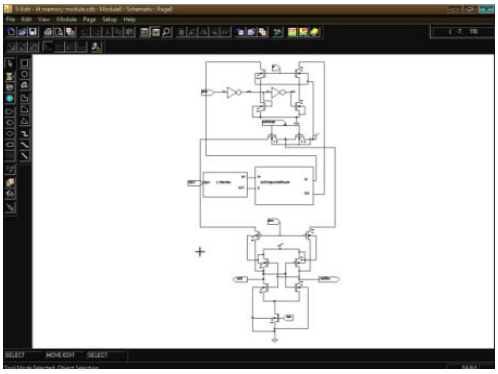

Fig C.Schematic Diagram for 4T memory System

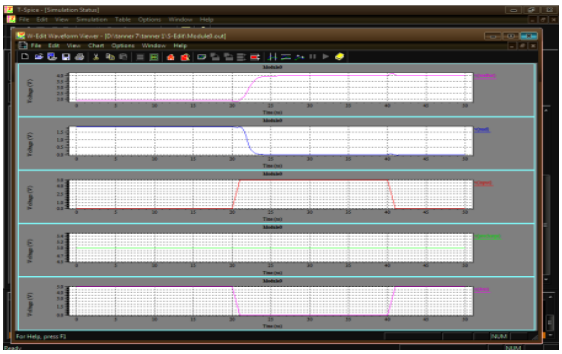

Fig d.Waveform for 4T memory System

TABLE
COMPARISON TABLE FOR SRAM ARRAY(delay)

S. NO	METHOD USED	6T SRAM	4T SRAM
1	NORMAL SRAM ARRAY	3.74	3.15
2	RECOVERY BOOSTING SRAM ARRAY	3.50	2.74
3	FINE GRAINED RECOVERY BOOSTING SRAM ARRAY	3.33	2.37

VII.CONCLUSION

NBTI is one of the most important silicon reliability problems facing processor designers. SRAM memory cells are especially vulnerable to NBTI since the input to one of the pMOS devices in the cell is always at logic “0.” In this paper, we propose recovery boosting, this technique that allows both pMOS devices in the cell to be put into the recovery mode by raising the ground voltage and the bitline to V_{dd}. First we go for designing a basic 6T SRAM array. In this we find out the read and write operation. Next we design the Modified Recovery boosting. In this case the power and delay gets increased. In order to overcome this problem we go for Fine grained Recovery boosting. After that 6T array is designed and also design a4T SRAM and its Recovery Boosting. By using this, the power and delay gets decreased. At last I constructed a memory system for 4T Fine Grained Recovery Boosting. Comparing to 6T SRAM array 4T array is best. Because in 4T SRAM array, delay is less.

In my future work To design a MAC unit by replacing the register with Fine Grain SRAM memory system

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Biography

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