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Analysis & Reduction of THD in Multilevel Inverter Using PSO Algorithm

S.Assly Steffy[1], B.Mangaiyarkarasi[2], S.Sherin Jasper[3], K.Priyanka[4], K.Soorya[5]

PG Student, EEE, Sri Shakthi Institute of Engineering and Technology, Coimbatore, India[1,2,3,4,5]

Abstract: The paper deals with harmonic reduction of cascaded multilevel inverter with non equal DC sources using particle swarm optimization algorithm. The proposed Scheme for multilevel inverter is multicarrier PWM control using PSO algorithm. The system is an effective replacement for the conventional method which has high switching losses and eliminates the use of transformer. The simulation result portrays the effective control in the switching angle to obtain minimum THD performance. The simulation of cascaded multilevel inverter is done in Matlab software package in Simulink environment. The application of this scheme is in grid and standalone applications.

Keywords: Particle Swarm Optimization, Harmonics, Cascaded Multi Level Inverter, Atmel AT89S52, Total Harmonic Distortion

I. INTRODUCTION

In high power systems, the multilevel inverters can appropriately replace the existing system that uses traditional multi-pulse converters without the need of the transformers. All the three multi-level inverter topologies(diode clamped, flying capacitors, cascaded multi level inverter) can be used in reactive power compensation without having the voltage unbalance problem. But the cascaded multi level inverter uses simple H-Bridge configurations which are connected in series, utilizes fuel cells, solar cells & biomass energy as DC sources.

With the help of a transformer having one primary winding and several secondary windings, the cascade H-bridge configuration can be used in back-to-back intertie application. This structure is therefore well suited for an ac power supply in vehicle system utilities.

The key features of a multi-level structure are as follows

- Harmonic content decreases as the number of levels increases.
- Here switching losses can be avoided and higher efficiency is obtained.
- Without an increase in the rating of an individual device, the output voltage and power can be increased.
- Multi-level inverters can easily be applied for high power applications such as large motor drivers and utility supply.
-

Because of the key feature, they have become indispensable in high power and high voltage applications.

II. HARMONICS

Harmonic Frequencies are integral multiples of the fundamental supply frequency. For a fundamental frequency of 50Hz, the third harmonic would be 150Hz and fifth harmonic would be 250Hz. Harmonics are a mathematical way of describing distortion to a voltage or current waveform. Fourier theory tells us that any repetitive waveform can be defined in terms of summing sinusoidal waveforms which are integral multiples (or harmonics) of the fundamental frequency. For the purpose of a steady state waveform with equal positive and negative half-cycles, the Fourier series can be expressed as follows:

$$f(t) = \sum_{n=1}^{\infty} A_n .\ sin\ (n\pi t\ /\ T)$$

Where

f(t) is the time domain function

n is the harmonic number(only odd values of n are required)

A_n is the amplitude of the nth harmonic component

T is the length of one cycle in Seconds

Harmonics should not be confused with spikes, dips, impulses, oscillations or other form of transients. A common term that is used in relation to harmonics is THD or Total Harmonic Distortion. THD can be used to describe voltage or current distortion and is calculated as follows:

$$THD(\%) = \sqrt{(ID_1^2 + ID_2^2 + \ldots\ldots\ldots + ID_n^2)}$$

ID_n is the magnitude of the nth harmonic as a percentage of the fundamental (individual distortion).

III. HARMONIC ELIMINATION

The multilevel fundamental switching scheme inherently provides the opportunity to eliminate certain lower order harmonics by varying the times at which certain switches are turned "ON" and turned "OFF" (i.e. varying the switching angles).Here 5^{th},7^{th},11^{th} and 13^{th} harmonics are minimized.

IV. CASCADED H-BRIDGE

A full-bridge inverter is known as an H-bridge cell. The inverter circuit consists of four main switches and four freewheeling diodes.

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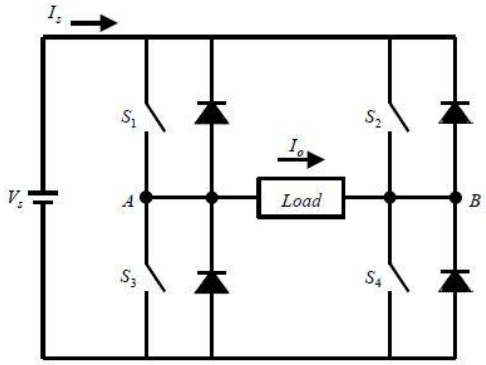


Fig.1.Cascaded H-Bridge inverter

V. LEVEL INVERTER MODEL

Multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. The maximum number of line voltage levels is 2m-1, where m is the number of phase voltage levels. The number of line voltage level depends on the modulation index and the given harmonics to be eliminated. The advantage of three-phase system is that all triplen harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. It has reduced Electromagnetic Capability (EMC) when operated at high voltage.

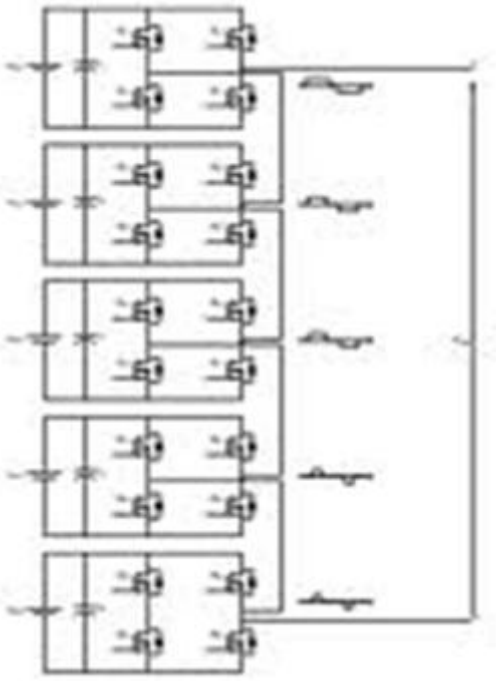


Fig.2. 11 Level cascaded multi level inverter

Even at low switching frequencies, smaller distortion in the multilevel inverter AC side waveform can be achieved (with stepped modulation technique). The output voltage is the sum of the output voltage of each H-bridge cell.

The phase voltage is the sum of each H-bridge outputs and is give as $V_{AN} = V_{dc1} + V_{dc2} + V_{dc3} + \ldots\ldots\ldots + V_{dc(S-1)} + V_{dcS}$

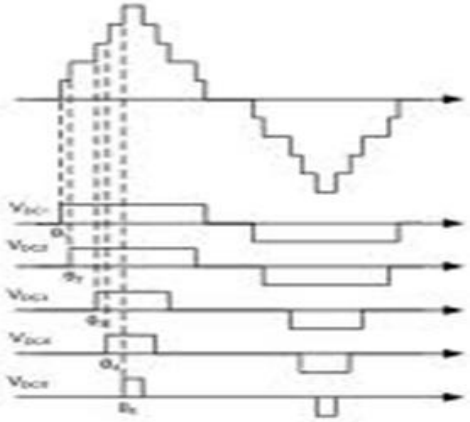


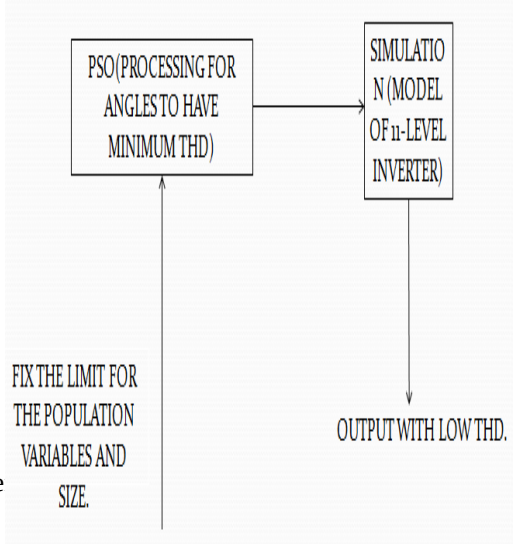
Fig.3. Waveform of 11 level inverter

VI. PARTICLE SWARM OPTIMISATION

The particle swarm paradigm is one of the latest population-based optimization methods, which does not use the filtering operation (such as crossover and/or mutation) and the members of the entire population are maintained through the search procedure. The PSO algorithm is an adaptive algorithm based on a social-psychological metaphor; a population of individuals (referred to as particles) adapts by returning stochastically toward previously successful regions.

Particle Swarm has two primary operators: Velocity update and Position update. During each generation each particle is accelerated toward the particles previous best position and the global best position. At each iteration a new velocity value for each particle is calculated based on its current velocity, the distance from its previous best position, and the distance from the global best position. The new velocity value is then used to calculate the next position of the particle in the search space. This process is then iterated for a set number of times, or until a minimum error is achieved.

Particle swarm optimization (**PSO**) optimizes a problem by having a population of candidate solutions, here dubbed particles, and moving these particles around in the search-space according to simple mathematical formulae over the particle's position and velocity.



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VII. ALGORITHM

1: **procedure** PSO
2: **repeat**
3: **for** i = 1 to number of individuals **do**
4:**if**
G(xi)>G(pi)
then
[G() evaluates goodness]
5: **for** d = 1 to dimensions **do**
6: pid = xid .
[pid is the best state found so far]
7: **end for**
8: **end if**
9: g = i .
[arbitrary]
10: **for** j = indexes of neighbors
do
11: **if**
G(~pj) > G(~pg)
then
12: g = j .
[g is the index of the best performer in the neighborhood]
13: **end if**
14: **end for**
15: **for** d = 1 to number of dimensions **do**
16: vid(t) = f(xid(t − 1), vid(t − 1), pid, pgd) [update velocity]
17: vid 2 (−Vmax,+Vmax)
18: xid(t) = f(vid(t), xid(t − 1)) . [update position]
19: **end for**
20: **end for**
21: **until** stopping criteria
22: **end procedure**

Where

PSO- Particle Swarm Optimizer.

t means the current time step,

t − 1 means the previous time step

Tmax the maximum number of time step the swarm is allowed to search.

P (xid (t) = 1) is the probability that individual i will choose 1 for the bit at the dth site onthe bit string.

xid (t) is the current state (position) at site d of individual i.

vid(t) is the current velocity at site d of individual i.

±Vmax is the upper/lower bound placed on vid.

pid is the individual's i best state (position) found so far at site d.

pgd is the neighborhood best state found so far at site d.

c1 social parameter 1, a positive constant, usually set to 2.0.

c2 social parameter 2, a positive constant, usually set to 2.0.

w(t) is the inertia weight (Inertia Particle Swarm).

wstart is the starting inertia weight (w(0) = wstart). (Inertia Particle Swarm)

wend is the ending inertia weight (w(Tmax) = wend). (Inertia Particle Swarm)

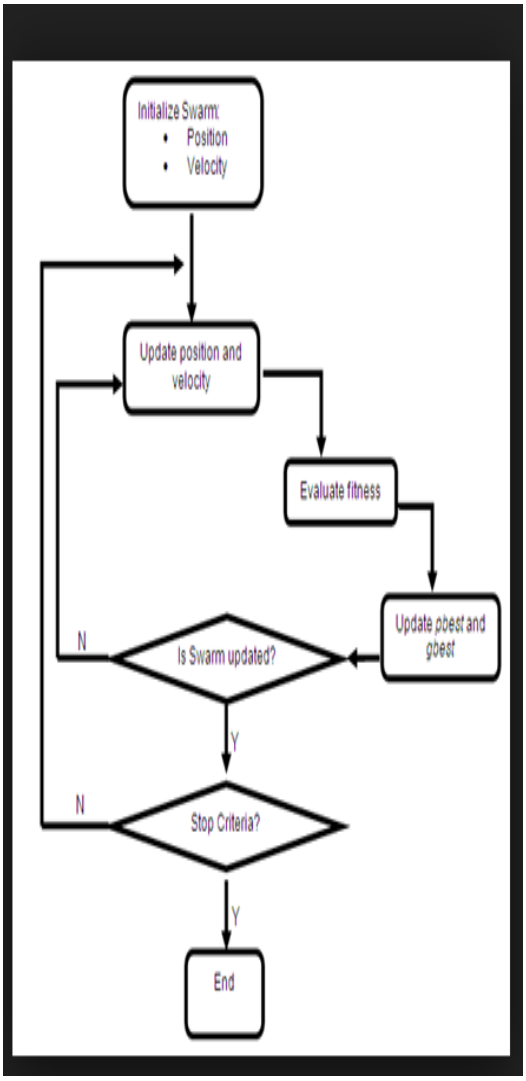

Fig. 4.Flowchart of PSO implementation

VIII PSO PROGRAMMING DETALS:

CONTENT	DATA
POPULATION SIZE	20
PARAMETERS USED	X,V,a,m,s,Q,phi1,phi2,phi,xp,pgdtemp, r4,k1,k2,k3,k4,k5,Vdc,vdc1,vdc2,vdc3, vdc4,vdc5,gbestvar,gbest,tempo,pgd,pid
MAXIMUM ITERATION	50
NO. OF EXECUTION TIMES	30
VOLTAGES	Vdc=100v,Vdc1=108v,Vdc2=98v, vdc3=90v,Vdc4=86v,Vdc5=80v Kn=vdcn/vdc

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IX. SIMULATION MODEL (11 level inverter)

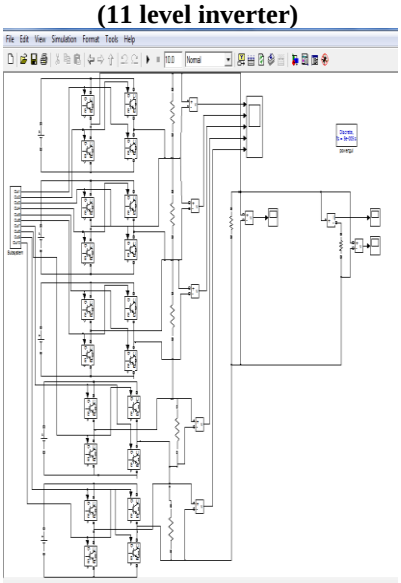

Fig.5. Simulation model of 11-level inverter

11-LEVEL OUTPUT

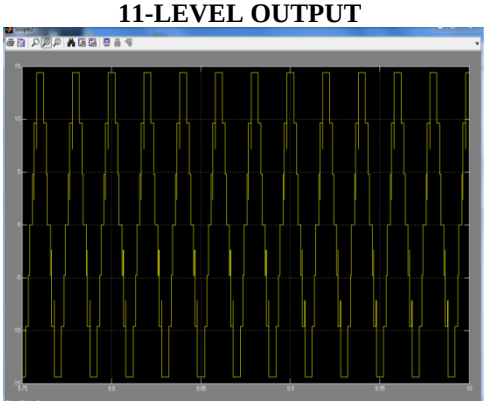

Fig .6. 11-Level Inverter Output

COMPUTED THD

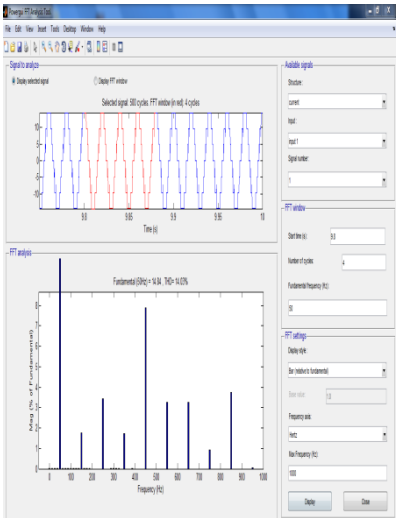

Fig .7. FFT analysis

X ATMEL 89S52

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pin out.

The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

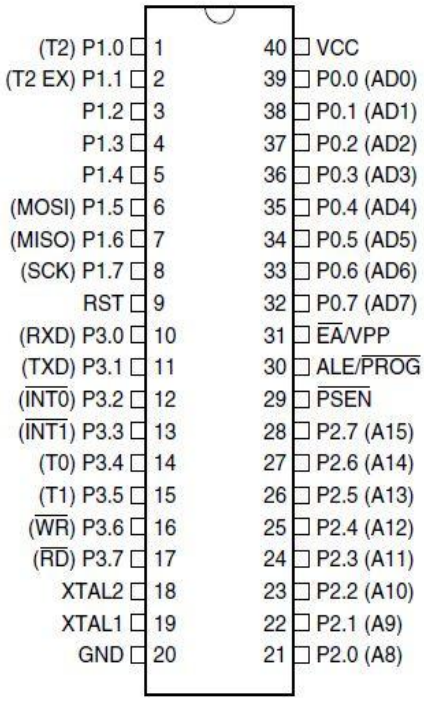

Fig.8. Pin Diagram

BLOCK DIAGRAM

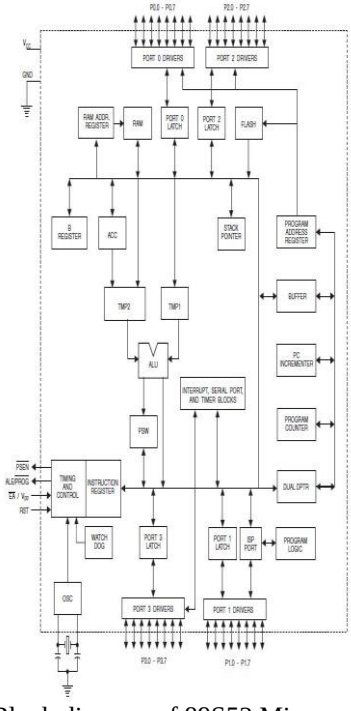

Fig.9.Block diagram of 89S52 Microcontroller

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XI. HARDWARE PROGRAM FOR THREE LEVEL OUTPUT

LABEL	CODING
START	LCALL DLY 1
	SETB P2.0
	SETB P2.1
	SETB P2.3
	SETB P2.6
	LCALL DLY 1
	CLR P2.6
	SETB P2.2
	LCALL DLY 2
	CLR P2.2
	SETB P2.6
	LCALL DLY 1
	CLR P2.0
	CLR P2.1
	CLR P2.3
	CLR P2.6
	LCALL DLY 2
	SETB P2.4
	SETB P2.5
	SETB P2.2
	SETB P2.7
	LCALL DLY 1
	CLR P2.2
	SETB P2.6
	LCALL DLY 2
	CLR P2.6
	SETB P2.2
	LCALL DLY 1
	CLR P2.4
	CLR P2.5
	CLR P2.2
	CLR P2.7
	LCALL DLY 1
	SJUMP START
DLY 1	MOV R1,#03
L2	MOV R4,#FF
L1	DJNZ R4,L1
	DJNZ R1,L2
DLY 2	MOV R1,#06
L2	MOV R4,#FF
L1	DJNZ R4,L1
	DJNZ R1,L2

XII. HARDWARE MODEL

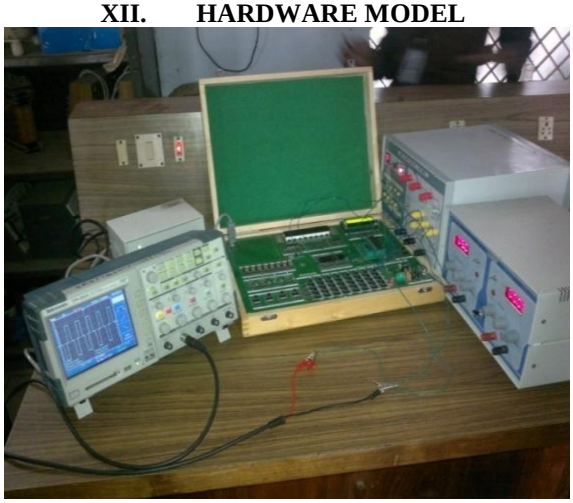
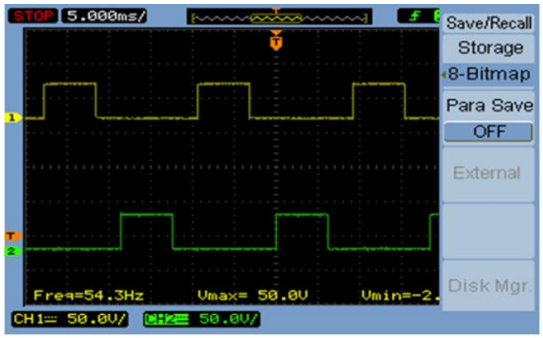


Fig.10.Hardware model

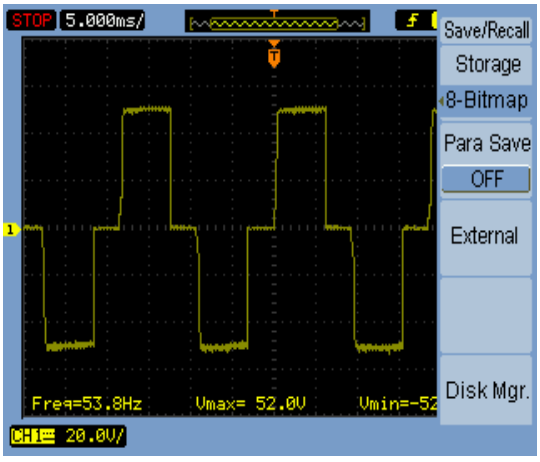
XIII THD ANALYSIS:

Sl.no	θ1	θ2	θ3	θ4	θ5	THD
1	0.2900	0.5500	0.6800	0.8910	0.8950	27.55
2	0.3500	0.5400	0.6600	0.8800	0.8800	20.50
3	0.5695	0.5785	0.7944	0.8782	0.9050	18.32
4	0.5500	0.5700	0.6600	0.6900	0.8700	12.26
5	0.4188	0.6501	0.8043	1	1	13.66
6	0.3970	0.5266	0.8233	0.9682	0.9863	19.44
7	0.3722	0.5145	0.7404	0.9446	0.9745	17.30
8	0.4242	0.5119	0.8792	1	1	23.55
9	0.3452	0.5252	0.7803	1	1	15.36
10	0.4059	0.5540	0.7336	0.9511	1	16.21
OPT	0.5500	0.5700	0.6600	0.6900	0.8700	12.26

XIV TRIGGERING SIGNALS FOR INVERTER



XV HARDWARE OUTPUT



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XVI. CONCLUSION

Thus in the 11 Level Inverter, the switching angles are found out through Particle Swarm Optimization algorithm and 5^{th},7^{th},11^{th} &13^{th} is minimized and thus Total Harmonic Distortion is reduced. And also for a 3 Level Inverter the switching angles are generated through 89S52 Microcontroller and a 3 level output waveform is generated.

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BIOGRAPHIES

S.Assly Steffy did her Bachelor of Engineering in Electrical & Electronics Engineering at Arunai Engineering College, Thirvuvanamalai and doing Master of Engineering in Power Electronics & Drives at Sri Shakthi Institute of Engineering and Technology, Coimbatore,India. Her research interests include drive application.

B.Mangaiyarkarasi did her Bachelor of Engineering in Electrical & Electronics Engineering at INFO Institute of Engineering, Coimbatore and doing Master of Engineering in Power Electronics & Drives at Sri Shakthi Institute of Engineering and Technology, Coimbatore, India. Her research interests include harmonic's study.

S.Sherin Jasper did her Bachelor of Engineering in Electrical & Electronics Engineering at Government college of Engineering, Tirunelveli and doing Master of Engineering in Power Electronics & Drives at Sri Shakthi Institute of Engineering and Technology, Coimbatore,India. Her research interests include PV application to Grid.

K.Priyanka did her Bachelor of Engineering in Electrical & Electronics Engineering at Tamilnadu college of Engineering, Coimbatore and doing Master of Engineering in Power Electronics & Drives at Sri Shakthi Institute of Engineering and Technology, Coimbatore,India. Her research interests include Industrial application.

K.Soorya did her Bachelor of Engineering in Electrical & Electronics Engineering at Avinashilingam University for women, Coimbatore and doing Master of Engineering in Power Electronics & Drives at Sri Shakthi Institute of Engineering and Technology, Coimbatore, India. Her research interests include Improvement of Power Quality.