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# Design of Resource Efficient FIR Filter Structure Using Adders and Multiplier

**P.C.Franklin[1], M.Ramya[2], R.Nagarajan[3], T.M. Mini Priya[4], M.Balamurugan[5]**

PG Scholar, Embedded System Technologies, S.A Engineering College, Chennai, India[1,3,4,5]

Lecturer, Electronics and Communication Engineering, S.A Engineering College, Chennai, India[2]

**Abstract:** This paper presents high speed digital Finite Impulse Response (FIR) filter relying on Wallace tree multiplier and Carry Select Adder (CSLA). Adder has three architectures such as basic CSLA using RCA (Ripple Carry Adder), CSLA using BEC (Binary to Excess-1 Converter) and CSLA using D-latch. In this paper we propose 4-tap FIR Filter architecture using 16-bit CSLA using D-latch and 8-bit Wallace tree multiplier. These multipliers and adders are used for high speed operation of digital FIR filter.

**Keywords:** CSLA, RCA, BEC, D-latch and Wallace tree multiplier.

## I. INTRODUCTION

Filters are used in wide range of applications such as multimedia and DSP (Digital Signal Processing) etc. Most of DSP computations involve the use of multiply accumulate operations and therefore the design of fast and efficient multiplier and adder units are important. More ever, the demand for portable applications of DSP architectures has dictated the need for low power designs [1]. Digital Finite Impulse Response filter (FIR) has performs lot of arithmetic and logical operations. In general, arithmetic and logic operation modules such as adder and multiplier modules, consume more chip area and delay for each operation is more. Input bit width of the modules is quite important in design parameter such as less delay and resource efficient filters. The resource utilization and power of digital FIR filter circuit is reduced by optimization of taps and bit width of input signal and filters coefficients [2]. The adders and Wallace tree multipliers are applied for filters to eliminate power consumption due to unwanted data transitions [3]. In [4] they presented a multipliers technique, based upon add and shift operation and common sub expression elimination for low area and high speed implementation of FIR filters. Finite impulse response filters are widely used in various DSP applications. Paper is structured as follows. Section2 gives mathematical relation for FIR filter, and section3 presents the design of adder unit used in our implementation. Section4 gives design of multiplication unit. Section 5 gives the design of FIR filter. Section 6 gives simulation and synthesis results. Section 7 gives conclusion of this project.

## II. MATHEMATICAL RELATION FOR FIR FILTER

Filters are very important part of digital signal processing applications. Filters have two uses, one is signal separation and other one is signal restoration. Signal separation is used only when the signal is contaminated with noise or other unwanted signals. Signal restoration is used only when the signal has been distorted. In general filtering is described by simple convolution operation such as

$Y(n) = x(n) * f(n) = \sum_{k=0} f(k)x(n-k)$

$= \sum_{k=0} x(k)f(n-k)$ (1)

The digital filters are commonly linear time invariant filters. The straight forward way of implementing LTI Finite Impulse Response filter is finite convolution of input series x(n) with impulse response coefficients is given by

$Y(n) = x(n)\ f(n)$ (2)

$= \sum_{k=0}^{L-1} f(k)x(n-k)$ (3)

Where L is the length of FIR filter, h(n) is filters impulse response coefficients, x(n) is input sequence and y(n) is output of FIR filter. The above equations can also expressed in Z domain as

$Y(z) = x(z)\ H(z)$ (4)

## III. REGULAR CARRY SELECT ADDER

CSLA compromise between Ripple Carry Adder (RCA) and carry look ahead adder (CLA).The main disadvantage of regular CSLA structure is the large area due to the multiple set of ripple carry adder. One set of RCA for carry as 0 and another set of RCA for carry as 1. The Fig. 1 shows [11] the 16-bit carry select adder. It is divided into five pairs of groups with different bit size RCA. The carry out calculated from the last stage that is least significant bit stage is used to select the calculated values of the output carry and sum. The selection of carry for the next stage is done by using a multiplexer.

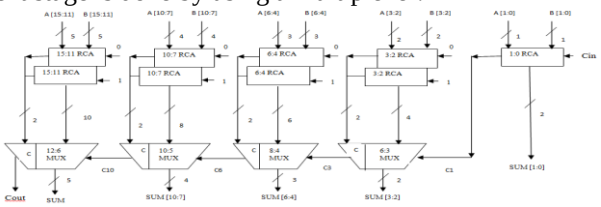


Fig.1. Regular CSLA

### *A. CSLA USING BEC*

The regular CSLA is not area efficient and delay for the operation is more because it uses multiple set of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry

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are selected by the multiplexers. To avoid this problem, the regular CSLA structure is modified using n-bit

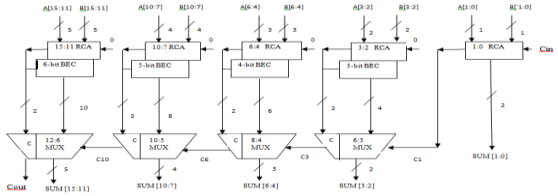

Fig.2. 16-bit CSLA using BEC

Binary to Excess-1 code converter (BEC) to improve the speed of operation [11]. To improve the speed of operation we can use the Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve less delay. The Fig. 2 shows the structure of 16-bit CSLA using BEC

*Binary to Excess-1 Converter*

One input of the 8:4 multiplexer 4-bit input such as (B3, B2, B1, and B0) and another input of the multiplexer is the BEC output. This can produce two possible results in parallel one is direct output and other is BEC output. There is no change in direct output. The multiplexer is used to select either the BEC output or the direct inputs according to the control signal Cin is shown in fig.3. If BEC input is X then O/P is "X+1". Compared with regular CSLA this can produces less delay for its operation and resource utilization also less.

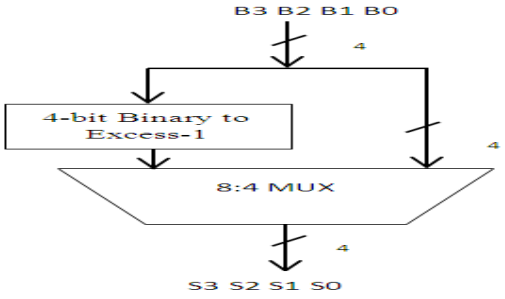


Fig.3. Operation of 4-bit BEC

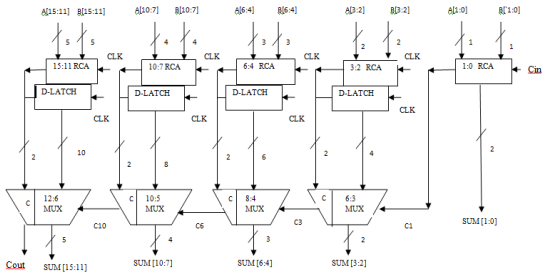

Fig.4. 16-bit CSLA using D-LATCH

*B. CSLA USING D-LATCH*

Here initially when en=1, the output of the RCA is Connected to the input of D-Latch and the output of the D-latch follows the input and given as an input to the multiplexer [10]. When en=0,there is no change in output which is same as that of previous state therefore the output from the RCA is directly given as an input to the multiplexer It can produce output only when the clock is en=1. Figure 4 shows the architecture of CSLA using D-LATCH. This can utilize only less resource for its operation and delay for the operation is less.

## IV. WALLACE TREE MULTIPLIER

Wallace tree is an implementation of adder tree designed for minimum propagation delay. It has three stages such as partial product generation stage, compression and reduction. The fig (5) shows the operation of Wallace tree multiplier. Here uses (8×8) Wallace tree multiplier [8]. Multiply each bit of the argument by each bit of the other;. Which can generates 8 set of partial products in row order. Depending on position of the multiplier bits the wires carry different weights. Reduce the number of partial products by layer of full adder and half adder. In this full adder is implemented using 3:2 compression technique and half adder is implemented using 2:2 compression technique. Group the wires into two numbers and add them using carry propagation adder.

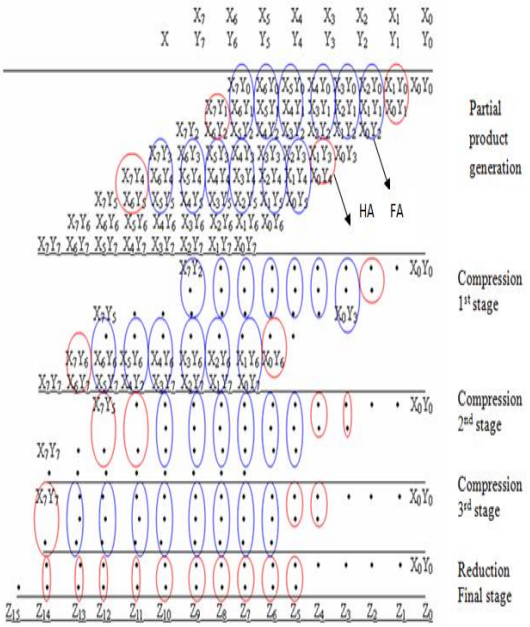


Fig.5. (8×8) Wallace tree multiplier

## V. DESIGN OF FIR FILTER

FIR filters are used in signal processing applications. Filter structure consists of delay element, adder and multiplier elements. The adder is replaced using CSLA with D-latch architecture and multiplier is replaced using Wallace tree multiplier is shown in fig (6).

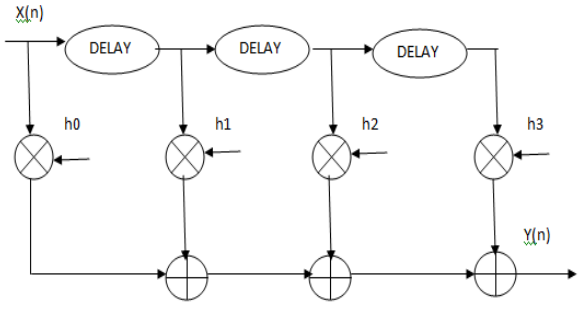


Fig.6. Structure of 4-tap FIR filter

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Here X(n) is input filter coefficients and h0,h1,h2 and h3 are transfer function coefficients Y(n) is output filter coefficient.

## VI. SIMULATION AND SYNTHESIS RESULTS

We perform the simulation and synthesis and summarize the results of all adders and multiplier. Functional verification of all the adders and multiplier are performed and these modified architectures are applied in 4-tap FIR filter finally results are summarized.

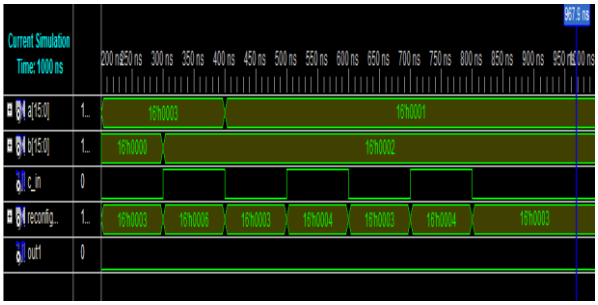


Fig.7. Output for regular CSLA

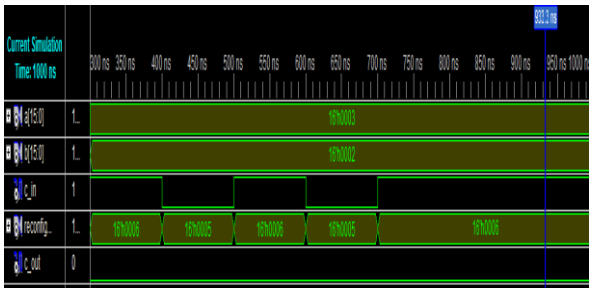


Fig.8. Output for CSLA using BEC

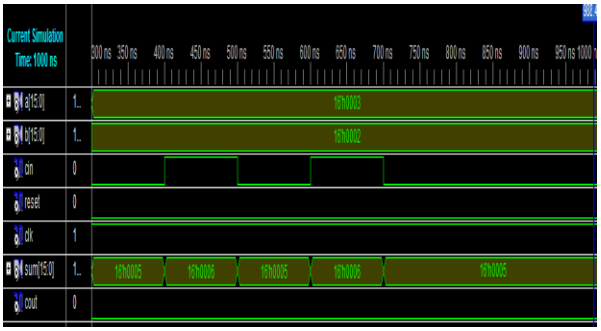


Fig.9. Output for CSLA using D-latch

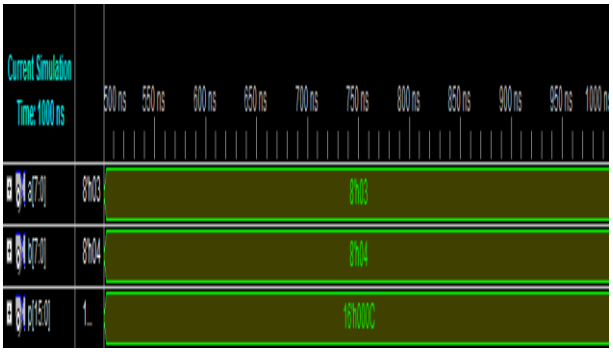


Fig.10. Output for Wallace tree multiplier

TABLE 1
COMPARISON OF ADDER ARCHITECTURES

After observation of simulation waveforms, synthesis is performed for calculation of delay and area and comparison of adder architectures are made in terms of area and delay and listed in the below table.

| Parameters | Regular CSLA | CSLA using BEC | CSLA using D-latch |
|---|---|---|---|
| Number of gates used | 30 | 28 | 18 |
| Destination paths | 662 | 437 | 365 |
| Delay(ns) | 7.195 | 7.370 | 5.984 |

From the above table it is clear that delay and resource utilization is less in CSLA with D-latch compared with CSLA with BEC and regular CSLA architectures.

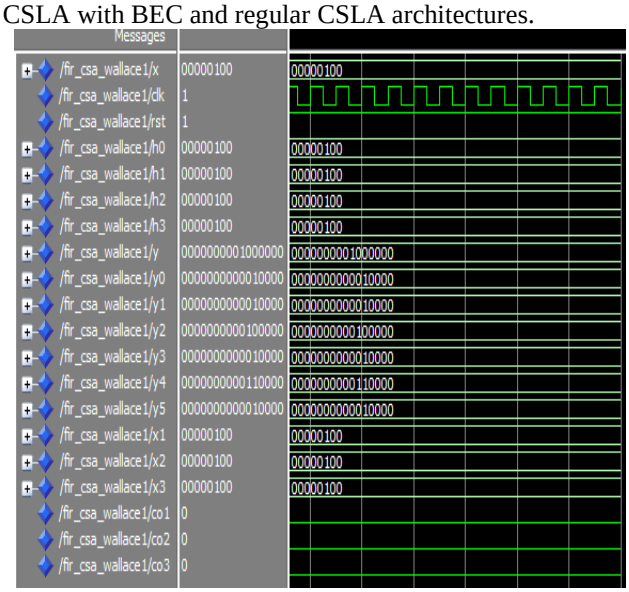


Fig.11. Simulation output for FIR filter using CSLA with D-latch and Wallace tree multiplier

Fig.11 shows the output for 4 tap FIR filter using CSLA with D-latch and Wallace tree multiplier. Here X is 8-bit input coefficient that is multiplied with 8 bit multiplier filter coefficients h0, h1, h2 and h3 produces 16-bit output. Both are sum together and produce filter output Y. Here multiplier uses Wallace tree multiplier and adder unit uses CSLA with D-latch.

## VII. CONCLUSION

Thus the models of CSLA are designed and are Implemented in VHDL using Xilinx 10.1 ISE tool and the results are compared in terms of delay and area .The CSLA with D-Latch proves to be the High Speed and Low area CSLA. And the Wallace tree multiplier also occupies less area. This adder and multiplier units are enhanced for FIR filter applications. . Thus a high speed and low power FIR filter can be designed using an Improved CSLA with D-latch and Wallace tree multiplier. The Improved FIR

filter architecture is therefore, high speed and area efficient for VLSI hardware implementation.

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