ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 2, February 2014

Effective Power Optimization Of Cms Scheme

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Abstract: Continuous scaling down of the transistor size causes the delay of local wires to decreases while delay of global wires remains the same. The current mode signaling (CMS) with effective bias circuit produce low power consumption over long on chip interconnect. This paper deals with variation tolerance with dynamic overdriving that produce less power consumption and proposed smart bias that increases the signal integrity through long distance communication. This proposed Smart bias is sensitive to both inter-die and intra-die variation. The CMS scheme and the proposed scheme is tested using 0.18um technology.

Index Terms: Dynamic Overdriving, On-Chip Interconnect, Current Mode Signaling (CMS), Smart Bias

I. INTRODUCTION

Performance of the transistor is continually improved by the scaling. However, the impact of scaling on the wires is reverse. The main goal of technology scaling is to continually decrease the gate delay and increase the gate density. Scaling down the transistor dimension reduces the transistor cost and area. Downscaling also leads to increase in the resistance and capacitance and produces the maximum delay in long chip wires. Global delay problem is thus reduced by inserting repeaters for the long distance communication in [1]. Many alternative repeaters are designed to reduce the power consumption over long distance communications [2]. In deep submicron the use of repeaters that consumes about 40% of power in 50nm technology. Due to continuous down scaling the expected distance between repeaters is reduced, showing increase in the power and area overhead [3]. An alternative circuit that is designed to limit the delay over on chip interconnect is the use of the Network on chip (Noc) [4]. This replaces the global interconnect buses with the specialized routers and the switches connected to the short range link. The delay in the short range link is still a challenge; this problem can be eliminated by insertion of via with repeaters. This can be implemented in three main classes: optical, wireless, and CMOS wires. In CMOS the current mode signaling technique is used, hence a speed of nearly equal to speed of light is achieved. Area is trade off in this scheme.

Another alternative approach used instead of the repeater is the self time regeneration approach [5]. In order to use the wide wires for achieving low loss throughput, the active circuit is positioned periodically along the line to compensate for attenuation and fast signal propagation. In addition, a transition monitoring mode is used, which senses and automatically reset the active circuit which boosts the signal where ever required.

Current mode signaling consumes the static power and hence they show the direct tradeoff between the speed and the power consumption. Dynamic overdriving scheme that is proposed in [6]-[7] has 60% improvement in energy/bit. Hence, dynamic overdriving scheme is used for process variation analysis. This reduction in the energy consumption is due to the low swing signaling. The CMS scheme is based on the low voltage swing and they reduce the noise margin of the data communication system. Hence, they are robust to process variation than the voltage mode repeater insertion scheme. As the technology downscales the process variation is the important concern in the device parameters. Process variation includes the inter-die variation and the intra-die variation. In case of inter-die variation they have identical device parameters but vary from die to die and batch to batch. In intra-die variation the process parameters are same.

The network on chip [6] does not discuss the impact of the inter die variation and intra die variation. The CMS scheme proposed in [8] contains the feedback scheme, which is less sensitive to inter-die variation. The Noc is robust only when the transistor parameters of transmitter and receiver side are identical. This also produces a mismatch between the transistor parameters of transmitter and receiver side [9]. In this paper, a CMS scheme is designed, which is robust to process variation and achieve high-speed over long distance communication. This achieves less power consumption over the voltage mode signaling scheme. The proposed CMS scheme uses the smart bias circuit at the transmitter side which makes high signal integrity for communication over long distance.

The CMS scheme is proposed with the low impedance receiver circuit. The input resistance is controlled largely by the geometry of transistors. The receiver circuit is an inverter whose output is shorted to its input as termination. This is equivalent to terminating the line to the ground through a diode connected n channel transistor and vdd to diode connected p channel transistor. The low impedance can be achieved by adjusting p and n channel transistor. This termination is fast because of absence of parasitic capacitance. The main advantage of the CMS scheme is that the line voltage is nearly constant. Compared with the

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voltage mode signaling the CMS scheme has reduced time constant and increased bandwidth.

II. CURRENT MODE SIGNALING SCHEME

Current mode signaling has the possibility of improving latency, throughput, and power simultaneously. The advantage of current mode comes from the fact that the line voltage is held nearly constant. This increases the bandwidth and reduces the time consumption because of low impedance termination. However, this leads to static power consumption [12]. Fig.1 shows the CMS scheme with feedback circuit that consumes high power and delay because of the feedback circuit.

The strong driver turns OFF when the line voltage crosses the switching threshold of the feedback inverter. The steady state voltage swing on the line is given by the product of the static current supplied by the weak driver and small signal impedance at the receiver. This FB scheme is robust against inter-die variation until transmitter and the receiver voltages remain the same.The strong driver circuit supplies the large current to the line during transition and weak driver provides a small steady state current to the line. NAND and NOR gates are turned ON by the strong inverter for short duration of time. This is controlled by the feedback inverter shown in the Fig. 1.

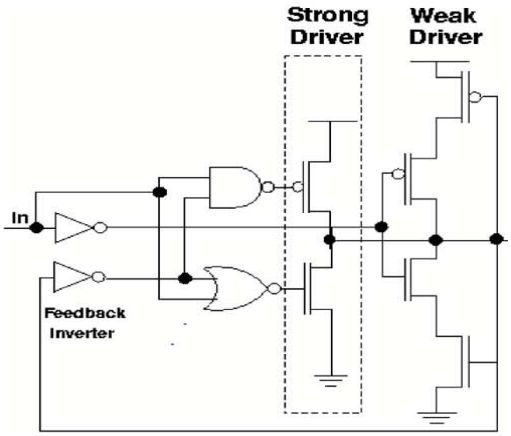

Fig. 1 CMS scheme-FB

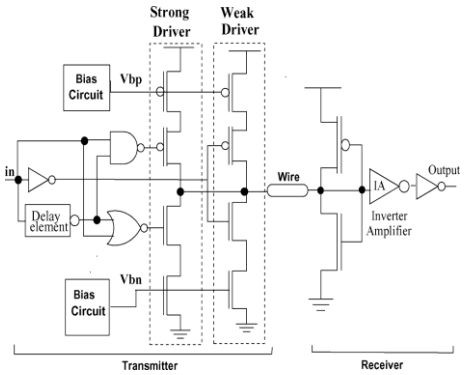

Fig. 2 CMS scheme with Bais

Because of delay and static power consumption in the FB scheme, the Bias circuit is used instead of the feedback shown in Fig. 2. Transmitter and recevier circuits are robust against process variation. The driver circuit is modelled as the current source and the receiver is modelled as the terminator circuit followed by an amplifier. The strong driver is turned ON by the delay element and not by the feedback. Strong and weak drivers are constant along all process corners.

III. BIAS GENERATION

Bias is used to establish a predetermined current throughout the circuit. The Fig. 3(a) shows a resistance based bias circuit. This does not change with the process variation and they consume larger power. Hence the diode connected transistor bias circuit is designed which has the long channel transistor as load and short channel transistor as sensor device shown in Fig. 3(b). Here the bias circuit does not change with the extreme process corners. This does not compensate the mobility variation. One solution is to use coarse and fine compensation shown in Fig. 3(c). The load transistor is compensated by the coarse bias circuit.

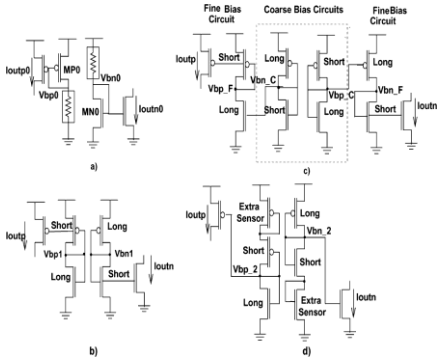

Fig.3. a) Resistance based; b) Diode connected transistor; c) Two step compensation; d) diode connected with extra sensor.

The change in the mobility variation is thus compensated by two sensor transistor and long channel transistor shown in Fig. 3(d). The combination of Fig. 3(c) and (d) shown in Fig. 4 is the corner aware bias circuit which is robust against both the inter-die and intra-die variations. This corner aware bias has the mobility variation and process dependence characteristics. To minimize the process dependence a bias circuit should sense the process corner and adjust the bias to compensate for the variation.

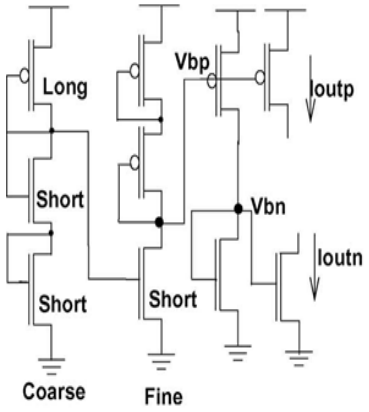

Fig.4 Corner aware Bias circuit

Long channel transistor has relatively less process variation compared to short channel transistor in the same process. From this difference a bias circuit is proposed which senses the process corner and try to increase the current in slow corners shown in Fig. 5. This is the simple bias circuit with input shorted with output.

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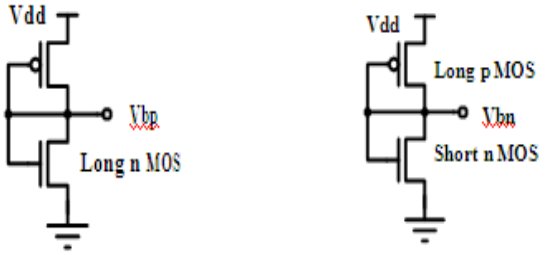

Fig.5 Proposed Smart Bias Circuit

IV. DELAY ELEMENTS

A delay element is a circuit that produces an output waveform similar to the input, but delayed by certain amount of time. It is impossible to take the input and output signal outside the package to measure delay. Delay of interconnect scheme is calculated by measuring the frequency of oscillation by choosing short wire between MUX and DEMUX shown in Fig. 6. The switch in the multiplexers and demultiplexers is designed using transmission gates where the multiplexer exhibits the same delay for all inputs.

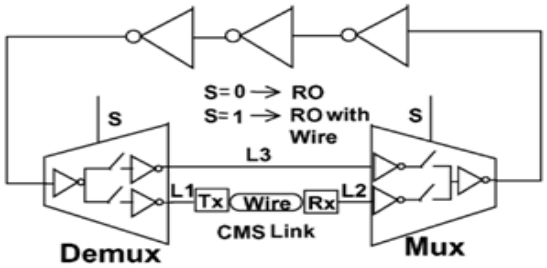

Fig. 6 Delay Measurement Circuit

The delay element is the ring oscilator were the output oscillates between two voltage levels, representing true of false. The NOT gates are attached in a chain, the output of the last inverter is fed-back as the input to the next inverter. Because of the feedback connection in the delay element the signal integrity is very low [10]-[11]. Proposed delay element is less sensitive to process variation and show better process corners as shown in Fig. 7.

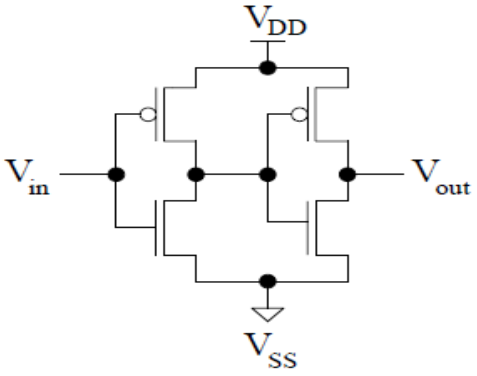

Fig. 7 Proposed Delay Element

A pair of cascade inverter is a simple delay element that delay an input signal by an amount equal to the combined propagation delay of two inverters shown in Fig. 7.
Since PMOS and NMOS transistors are never ON at the same time, the static power consumption is only due to the leakage current and is generally small. The short circuit power consumption is based on the signal integrity and the supply voltage with chain of inverters, with equal rise and fall time, the short circuit dissipation is 20% less compared to the dynamic power dissipation.

V. POWER ANALYISIS OF BIAS CIRCUITS AND PROPOSED CMS SCHEME

The power consumed by resistance based bias circuit is larger compared to all bias generation circuit. Due to the presence of resistance, area and the power consumption is high. The proposed smart bias circuit consumes less amount of power than other bias circuits. This consumes nearly 60% less power than the resistance based circuit. The diode connected transistor based bias circuit consumes 40% higher power than the proposed circuit. All comparisons are done with 0.18um technology. The proposed Bias circuit is less sensitive against inter die and intra die variations. Comparison of power consumption of existing system shown in Table I.

TABLE I
POWER ANALYSIS OF EXISTING SYSTEM

Existing System	Power(mW)
Bias:Corner Aware	0.35
Delay Element: Ring Osillator	

TABLE II
POWER RESULTS OF BIAS CIRCUIT

S.No.	Bias Generation Circuits	Power (mW)
1.	Resistance based	0.743
2.	Diode connected transistor based	0.495
3.	Two step compensation	0.575
4.	Diode connected with extra sensors	0.487
5.	Existing corner aware bias circuit	0.380
6.	Proposed bias circuit	0.348

Comparison of power consumption of exsiting system with bias circuit modification is shown in Table II. The proposed circuit consumes 15% less power compared to exsisting system. Table III shows power result of proposed system with bias circuit modification and delay element modification.

TABLE III
POWER ANALYSIS OF PROPOSED SYSTEM

Proposed System	Power(mW)
Bias Circuit : Smart Bias	0.33
Delay Element: Cascade Inverter	

VI. EXPREMENTAL RESULT

The current mode signaling output is the same as the output of the inverter where the output is delayed by

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certain amount of time. As the process technology changes the area and power consumption also varies.

The result using obtained in 0.18um technology with bias circuit modification and CMS signaling scheme. The proposed dynamic overdriving scheme shows lower power consumption. The run time can be varied with the input given to the circuit. As the technology changes they show variation in power consumption and channel length of the transistor.

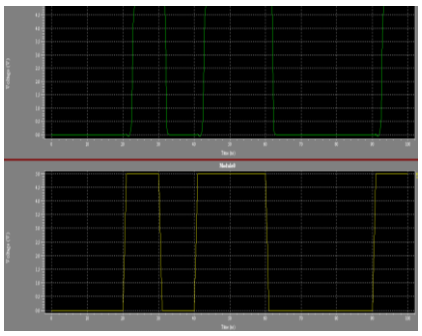

Fig. 8 Existing CMS scheme with corner aware and ring oscillator

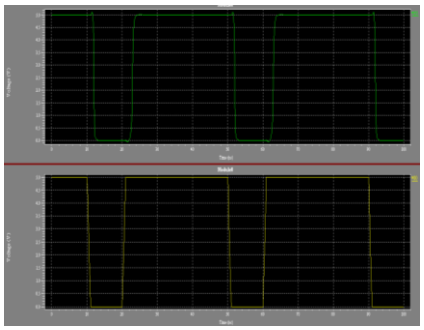

Fig. 9 Proposed CMS scheme with Smart Bias Circuit.

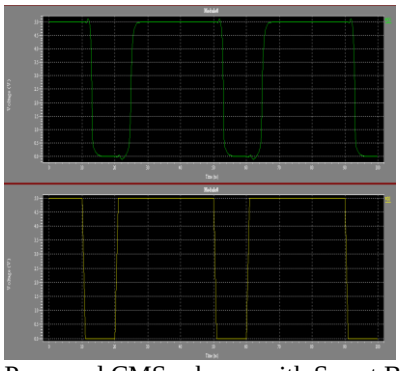

Fig. 10 Proposed CMS scheme with Smart Bias and Cascade Inverter.

VII. CONCLUSION

Delay, power, area and noise are all important parameter metrices in on chip signaling methodologies. A variation tolerance on chip signaling is designed which is robust against process variation.The proposed CMS scheme a is design which reduces the mobility variation between N-channel and P-channel transistor. The CMS-FB is more sensitive to supply noise than DC drift in the supply. The supply noise plays a major role in reducing the voltage swing on the line. The proposed CMS scheme consume only 0.33mW of power and is measured in 0.18um technology. Measurement results are sensitive to process variations.

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