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A Low Power Semi-Parallel Decoder Using Asm For Polar Codes

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Abstract: Polar codes are recently proposed as the first low complexity of codes that can provably achieve the capacity of symmetric binary-input memory less channels. We built an Asynchronous State Machine (ASM) to replace processing elements to control the decoding by state transition method results low power consumption. Our coding scheme also achieves the capacity of the physically degraded receiver-orthogonal relay channel. Though, it reduces power and logical elements to present a new low power technique for VLSI technology. Our proposed system avoids internal switching activity of registers by reusing the processing elements by folding technique. It drastically reduces static and dynamic power of the circuit along with area.

Keywords: Fast Fourier Transform (FFT), Asynchronous State Machine (ASM), Polar Codes, Successive cancelation decoder, Very Large Scale Integration (VLSI).

I. INTRODUCTION

In digital communication, transmission of data in digital form from source to user via communication channel can be done by some of the coding techniques. Shannon proved the existence of maximum rate known as channel capacity – through which the information transmitted over a channel can be reliable by using the codes to transmit the data which includes same error correcting coding. Many different capacity approaching codes have been developed like Low Density Parity Check Codes (LDPC) whose Bit Error Rate (BER) performance are near to SHANNON limit [8].

Polar Code has been recently discovered capacity achieving codes invented by Erdal Arikan. It is an Encoding/Decoding method (scheme) for achieving the capacity of Symmetric Binary Input Discrete Memory less Channel (BDMC) called Channel Polarization with low complexity [5]. For data transmission, polar codes can be effectively used for solving the encoding/decoding complexity to O(NlogN), N is code length. To decode one codeword, millions of computational nodes are required. Polar codes are linear block codes that can be find in almost all good channels with low computing complexity.

Polar codes have some of desirable properties like recursive structure that enables resource sharing and significantly simplifies the scheduling. In polar codes a good error correcting performance can be achieved when compared to other approaches. Because they do not require any randomness which avoid memory conflict problems. List decoding [2] non binary polar codes [4] are some of the work which used to improve the error correcting performance of polar codes. Here in this work, Encoding is made by polar codes where SC Decoding algorithm can be implemented with folding technique for low complexity without affecting the throughput [3].

To reduce the high complexity in each node, SC Decoding can perform its computation in logarithmic domain. When compared to LDPC decoder the hardware complexity can be further reduced by semi-parallel architecture. In our proposed work we minimize the processing elements complexity in both encoding and decoding.

II. ERROR CORRECTION AND DETECTION SCHEME

Generally Error Detection and Correction can be achieved by adding a redundancy bits to the message, where receiver can check the reliability of the message that got delivered and to recover the data that has been transmitted without any error. In systematic method, by using some deterministic algorithm the transmitter sends the original data along with check bits. In the receiver side by using the same algorithm the data is retrieved and compared with the received check bits. If the values are getting mismatched then at some point in the transmission side error has occurred. Unlike in non systematic method, the message will be encoded. Communication channel plays a major role for good error control performance. Random-error-detecting/correcting and Burst-error-detecting/correcting are two different channel models. Some codes are applicable for both random and burst errors. Before transmission, the sender encodes the data using error – correcting code (ECC), the redundancy is used to recover the data without needing the request for any retransmission is Forward Error Correcting Codes (FEC). If the channel capacity is varying heavily then the retransmission of erroneous data is made which is known as Automatic Repeat Request (ARQ). Without retransmitting minor errors can be corrected by combining both ARQ and FEC. Major Errors can be corrected by retransmission called Hybrid Automatic Repeat Request (HARQ).

By using checksum algorithm error detection can be realized, a hash function which adds a fixed length to the message for detecting purpose. Some of the detecting methods are as follows:

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A. *Repetition Codes*

To achieve an error free communication the data bits passing from one end to another through channel will get repeated in this scheme. The data to be transmitted should be sent in the form of blocks of bits. Each block will be transmitted for some predetermined number of times. Though it is simple method, they are inefficient and risky.

B. *Parity Bit*

To ensure the number of set bit at the outcome as odd or even the message bits should be concatenated. This is very simple scheme to detect a single or odd number of errors in the output. Even though the data is erroneous an even number of missed bits make the parity bit to appear correct.

C. *Checksum*

A checksum of a message is an arithmetic sum of message code words of a fixed word length. The sum may be negated by means of a one's-complement operation prior to transmission to detect errors resulting in all-zero messages.

D. *Cyclic Redundancy Check*

A Cyclic Redundancy Check (CRC) is a single-burst-error-detecting cyclic code and non-secure hash function designed to detect accidental changes to digital data in computer networks. They are well suited for detecting burst errors. It is characterized by specification called generator polynomial, which is used as the divisor in a polynomial long division over a finite field, taking the input data as the dividend, and where the remainder becomes the result. CRCs are particularly easy to implement in hardware, and are therefore commonly used in digital networks and storage devices such as hard disk drives.

III. CONVOLUTION CODES AND BLOCK CODES

Bit by bit basis of processing are convolution codes, will be appropriate for implementing in hardware and in viterbi decoder.

Block by block basis of processing are block codes where the data are encoded in block. When a sender transmit a very long data stream by this coding technique the stream are broken down into some pieces of fixed size. Each piece is known as message and by using the corresponding procedure the block codes encode the messages into codeword. Then all blocks of codes are transmitted to the receiver, where the original messages are retrieved from the received block by the decoding algorithm.

Here the overall transmission mainly relay on some parameters for its performance and Early examples of block codes are repetition codes, Hamming codes, followed by a number of efficient codes, Reed-Solomon Codes (RS) being the most notable due to their current widespread use. Turbo codes, Low-Density Parity-Check Codes (LDPC) [6] and POLAR CODES are relatively new constructions that can provide almost optimal efficiency.

IV. EXISTING ENDEC

The polar encoder for N=8 as shown in fig1, where 8 inputs of information bits need to be transmitted, in that each input line depends on one another[1]. To convert it in to a codeword, it should get additive in three stages. Obtained codeword is transmitted over the channel by passing through the buffer. This information bits are retained in the destination part by decoding the codeword.

SC Decoder with N = 8 has been used for decoding with two functions f and g with three stages depending on each other as shown in fig 2.

$$f(a,b) = \frac{1+ab}{a+b}$$
$$g(\hat{s},a,b) = a^{1-2\hat{s}}b$$

V. PROPOSED ENDEC

By using folding technique the processing element is reduced for transmitting the data through encoder and to retrieve the information from decoder.

A. *Polar Codes*

Polar codes are linear block of codes proposed by Arikan, a family of codes that achieves good channel capacity with low complexity in encoding and decoding. Its construction of generator matrix is done by using Kronecker power of the matrix G.

The Fig.1 represents the polar encoder for N=8, where $u_0 . . . . . u_7$ are the message bits that has to be transmitted from sender at the same time and $x_0 . . . . . x_7$ are those codeword that has to be passed over the channel. In the receiver side the received codeword are decoded to retrieve the original information. Here polarcodes exploits the channel polarization.

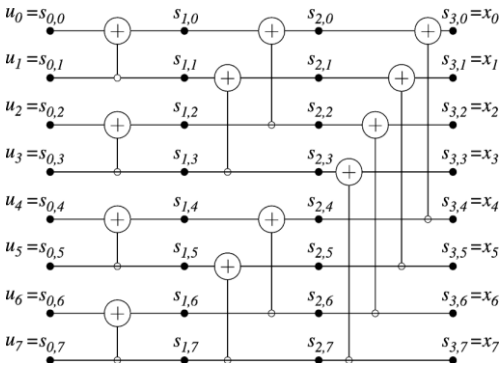

Fig1 Polar encoder for N=8

B. *Successive Cancellation Decoder*

The corresponding code word $x_0 . . . . . x_7$ sent over the channel with full utilization. In Successive cancellation decoder the message bits are retrieved which are denoted as$u_0 . . . . . u_7$. The information obtained back is as follows initialy u_0 , then comes u_1, finally u_{N-1} [7]. Assume the current stage *i*. Now denote the $u_0 . . . . . u_{N-1}$ as $\widehat{u_0}, ... \widehat{u_{i-1}}$. if *i* is not frozen set, then decoder estimates $\widehat{u_i}$.

$$\hat{u} = \begin{cases} 0, & if \ \dfrac{\Pr(y, \hat{u}_0^{i-1} | u_i = 0)}{\Pr(y, \hat{u}_0^{i-1} | u_i = 1)} > 1 \\ 1, & otherwise, \end{cases}$$

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This is likelihood ratio (LR) of $\widehat{u_i}$. Where $\widehat{u_0^{i-1}}$ is previously decoded bits $\Pr(y, \hat{u}_0^{i-1} | u_i = 0)$. If the probability of u_i is not effective then in both encoder and decoder the value is set to 0 so no information is transmitted through u_i [1].

For effective implementation of SC decoding of the code, Fast Fourier Transform (FFT) structure is used which is shown in Fig.2 for N=8. Here $y_0 . . . . . y_7$ are channel likelihood ratio (LR) is on right hand side where the message bits are on left side. The decision unit decide and represents, where the decoded output is correct or not, by denoting it as either 0 or 1. For instance, in Fig.5.3, for example $\hat{s}_{2,1} = \hat{u}$ EXOR $\hat{u}_3$.

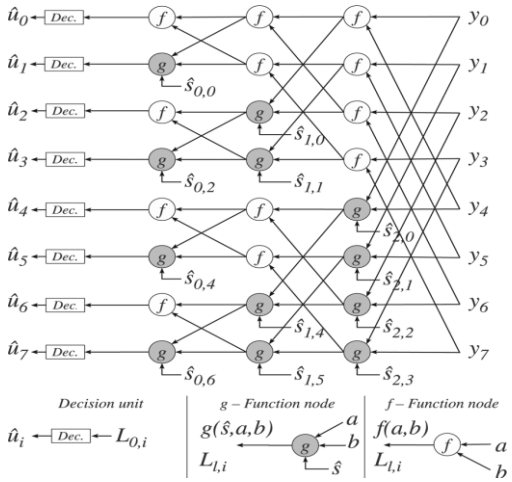

Fig 2 FFT structure of decoder of N=8

By using the folding technique the three stages of processing elements work is reduced to a single stage by minimizing the register. So that the power consumption will be reduced along with the area.

C. *Asynchronous State Machine*

In digital circuit design, sequential circuits or finite state machines are circuits containing some sort of memory, as opposed to combinational circuits which contains no memory. In combinational circuits output depends only on present input. In sequential circuits, the output depends not only on present input but also on the past output which needs the memory for storing its value where the memory is implemented with circuit elements called flip-flops that are clocked at specific times to update their contents. As in synchronous design the clocking scheme used in a circuit is very strictly specified, where as in flip-flop or sequential circuit, the clock signal must connect to a single system clock signal so that all the states in the system changes at the same time i.e. a global clock. Like in multi-phase clocking the clocking scheme can be more relaxed, a system of several clocks all derived from a common master clock, which allows a state to change at controllable times in the system operation. A case is there where no clock signals to make the system when a state to be changed. This is the asynchronous finite state machine. Here there is no special clock signal which causes state changes. Instead, the state machine reacts to changes on the input variables from the environment. The memory in sequential circuits arises from the feedback present in asynchronous design to implement states in the state machine operation. In asynchronous sequential circuit design, there are no artificial restrictions on circuit behavior.

VI. RESULT ANALYSIS

In signal processing, Polar code technique is implemented where a higher channel capacity can be attained. By using this, the utilization rate of channel will be achieved and the complexity of the Processing Elements is reduced by folding technique while transmitting the information bits from sender to receiver.

Initially streaming data's are loaded into an on chip memory and 8 samples are loaded into 2 radix butterfly unit in parallel for clock cycles as shown in fig 3. Processing elements compute precoding using input vector and encoding coefficients. The coefficients are loaded in a memory. After the 1st stage, precoded vectors are feedback to previous processing elements using buffer insertion method i.e folding technique. The encoded data's are forwarded to receiver via communication channel. At receiver, data's are again streamed into on chip memory and decoding using SC decoder whose structure is shown in fig 3. Received vectors and coder coefficients are multiplied together to retain the original data.

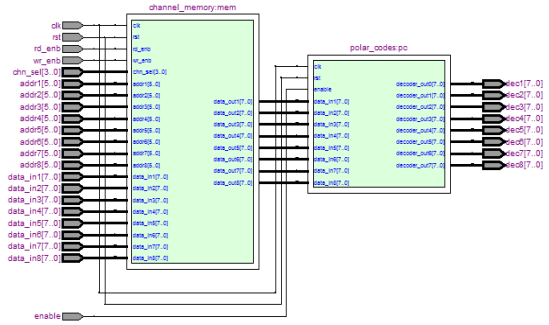

fig 3. RTL view

This shows the overall process of integrated view of both encoder and decoder. The Encoder which transmits its data to the decoder, where the original data is obtained. The chn_sel is nothing but the random generator to transmit the data. The data_in gives the input to the encoder, where the data_out to data_in represents the channel part (buffer). In the decoder side the data are retrieved based upon SC Decoder as shown in fig 2. The outputs dec1 to dec7 as shown in fig 3 are the decoded outputs.

The Fig 5 & 7 represents the intermediate results of encoder and decoder. The encoded data's are forwarded to receiver via communication channel which is shown in fig 6. At receiver, data's are again streamed into on chip memory and decoding using address decoder. The decision unit will represents the output as according to the decision whose simulation output is shown in fig 8. Received vectors and coder coefficients are multiplied together to retain the original data. Table shown below differentiates the existing and proposed area, power and throughput of whole transmission

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TABLE I
Area, Power and Delay Analysis

Parameter	Existing	Proposed
Power (mW)	343.76	136.47
Area	6012	3234
Throughput(Mhz)	157.98	140.02

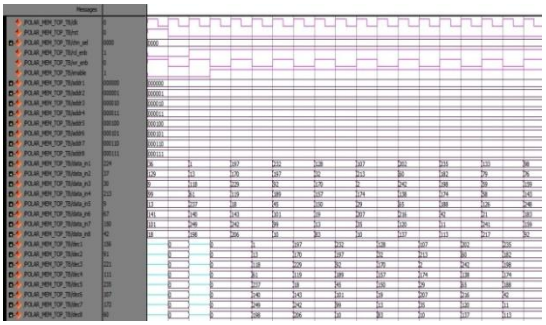

Fig 4: Simulation output

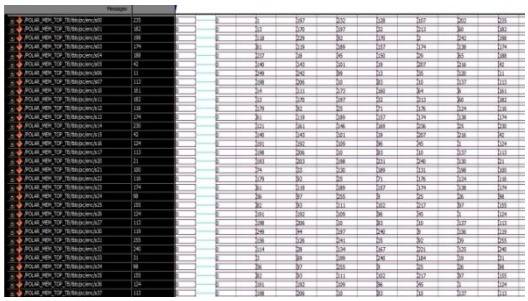

Fig 5: Intermediate output of encoder

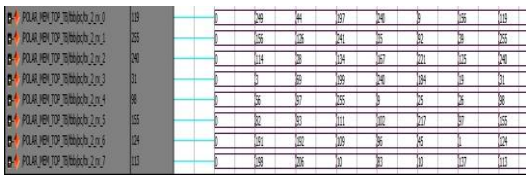

Fig 6: Transmitter to receiver

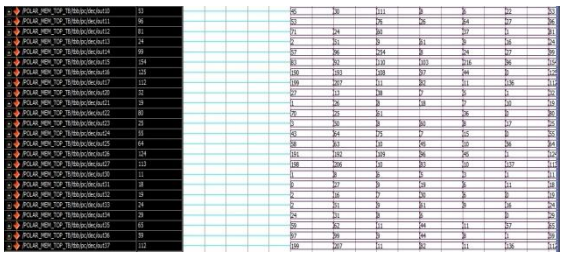

Fig 7: Intermediate output of decoder

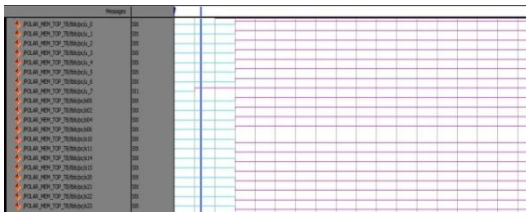

Fig 8: Decision unit output

VII. CONCUSION

Power consumption is an important factor in VLSI. It reduces the efficiency of the system. It also reduces battery endurance. In order to increase the efficiency power dissipation must be reduced. Our proposed system avoids internal switching activity of registers by replacing state machines. It drastically reduces static and dynamic power of the circuit. With the help of folding technique the power in proposed system is reduced when compared to existing and also area is minimized. Integration part of encoder and decoder has to be done by passing the values from the channel memory.

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BIOGRAPHIES

Lalithambigai M, pursuing M.E in VLSI Design at Sona college of technology, Salem. Her current interest includes design implementation of low power digital system.

M.S.Thaen Malar is Postgraduate Degree holder in applied electronics, working as an Assistant Professor of Electronics and Communication, in Sona College of Technology for the past two years. She is a Life Member of Indian society of Technical Education. She has published papers on various International journals and International conferences. Her area of interests includes Communication Engineering,VLSI Designs, DSP Integrated circuits and Advanced DSP.