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Comparative Study of Adder Cells Using Different Logic Styles

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Abstract: The main building block of many arithmetic system is the adder cells. The performance of multipliers is greatly influenced by the efficiency of the adders. Adder cells using different logic styles are discussed in this paper. Different logic styles include Cmos logic, Pass transistor logic, Transmission gates and Shannon based adders. The main aim of this work is to compare the performance of adder cells in terms of delay , power consumption, area and energy delay product. The adder cells are designed for 0.18um CMOS technology. Cadence tool is used for the simulation.

Keywords**:** Full adder, CMOS logic , Pass transistor logic, Transmission gate , Shannon based adder.

I. INTRODUCTION

Arithmetic functions such as addition and multiplication have a special significance in VLSI designs. Most of the applications require these basic operations, but good performance has been a challenge in silicon implementation. Adders are the fundamental circuit in all the arithmetic designs. With advances in technology, we need adders having high speed, low power consumption , regularity of layout and hence the less area or even a combination of them in one application, the growing demands of communication adder.

An adder or summer is a digital circuit that performs addition of numbers. Many computers and processors uses adders in the arithmetic logic units. Although adders can be constructed for many numerical representations such as binary coded decimal or excess-3 the most common adders operate on binary numbers[5].

Binary adders are the most essential logic elements within a digital system and also helpful in units other than Arithmetic units(ALU), such as multipliers , dividers, and memory addressing. Therefore the binary addition is essential that any improvement in binary addition can result in a performance boost for any computing system and help improve the performance of the entire system. This paper discusses about adder cells using various logic styles and comparing the performance between them in terms of power dissipation, delay and area.

II. FULL ADDER CELL

A full adder adds binary numbers A one-bit full adder adds three one bit numbers represented as A,B,Cin[6][7]. A and B are the 1 bit operands and Cin is the input carry which is responsible for the carry propagation. The circuit provides a 2 bit outputs. Output carry and sum typically represented by the signals Cout and S. The block diagram of full adder is shown below.

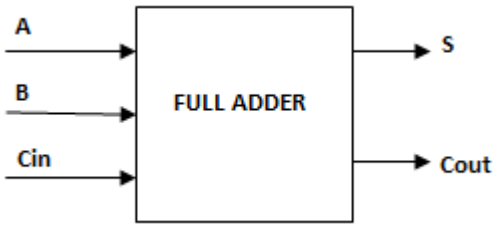

Fig1:Full adder

TABLE I
TRUTH TABLE

Input			Output	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

By using karnaugh map method the expression for sum and carry out are given as

Sum S = A xor B xor Cin (1)

Carryout Cout = (A xor B)Cin + AB (2)

III. LOGIC STYLES

The logic style used in circuit is mainly influenced the speed, size, power dissipation, and complexity of a circuit. The delay of the circuit is determined by the carry propagation, the number of transistors , transistor sizes , and intra- and inter-cell wiring capacitances[2]. Circuit a is depends on the number of transistors and their sizes and the interconnects. Power dissipation is determined by the

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switching activity and the node capacitances. The wiring complexity is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance.Design of full adders using different logic styles are discussed here.

A. Cmos logic

The equation 1 and 2 are based on logic gates. It requires XOR,AND gates. And the circuit diagram is as follows.

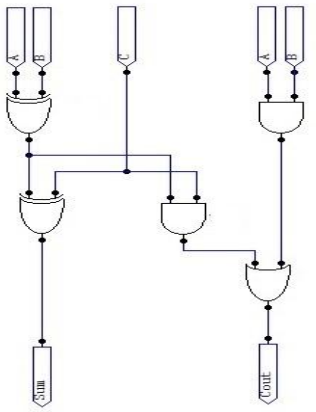

Fig2:Full adder Circuit

B. Modified circuit

The expression for sum and carry out can be modified by analyzing the truth table[6]. The expression for sum and carry out can be rewritten as

Sum = Cin (A+B+C) + A.B.C (3)

Cout = C(A+B)+A.B (4)

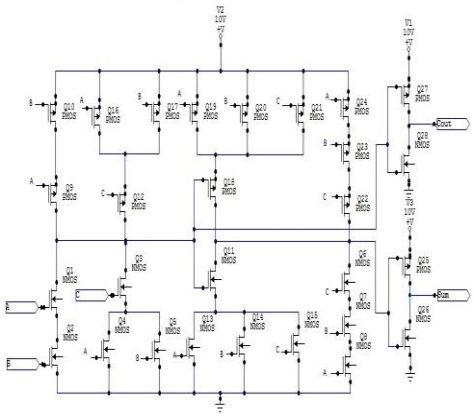

Fig3:Full adder modified Circuit

Figure 3 shows the circuit of full adder with modified expression. So the transistor count is reduced from 36 to 28.

C. Pass transistor logic

Pass transistors are single FET that pass the signal between the drain and source terminals instead of a fixed power supply value, nFETs are preffered for this application since the larger electron mobility implies faster switching than could be obtained with pFETs of the same size. Pass transistor requires less area and wiring and hence less power consumption[2]. The main drawback is the reduction of the full swing. This can be avoided by using Swing Restored Pass Transistor Logic.The cross coupled inverters are used for recovering the full swing.

From the truth table it can be seen that the sum is equal to the xor operation of A and B if Cin=0 otherwise sum will be the xnor of A and B. Following the same criteria the output Co is equal to the A.B if Cin is 0 otherwise it is A+B. Block diagram of full adder is shown below.

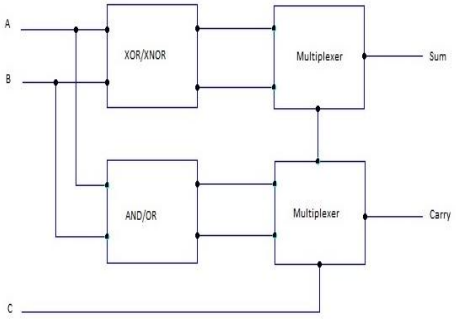

Fig4: Block diagram of PTL

The main problem with pass transistor logic is the reduction of voltage swing. It can be reduced by using swing restored PTL(SRPTL).The circuit is for sum is shown in figure 5 and carry circuit is shown in figure 6.

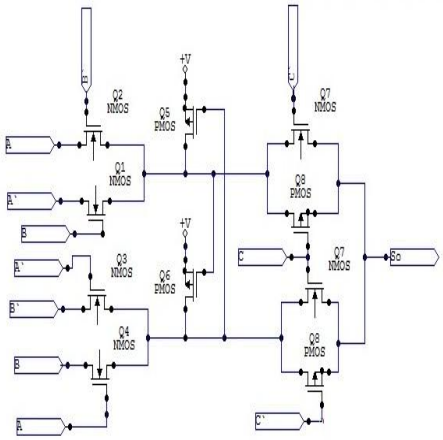

Fig5: Sum circuit

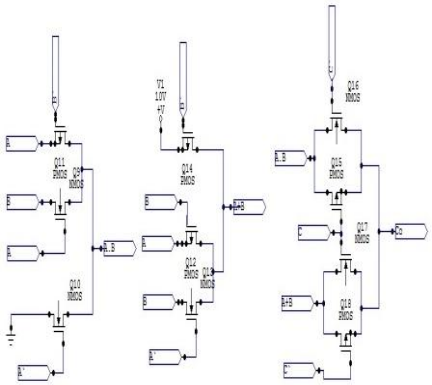

Fig6: Carry circuit

D. Shannon based adder cell

Shannon based adder is the adder cell using shannon theorem. Shannon based adder cell is mainly introduced to

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minimize the size and power consumption[1]. Shannon theorem states that any logic expression is divided into two terms. One with a particular variable set to 1 and multiplying it by a variable and then set the variable to 0 and multiplying it by the inverse. Design. The Shannon's theorem in a generalized way can be stated as a function of many variables, y(b0,b1,b2,y,bi,y,bn) can be written as the sum of two terms say one with a particular variable ai,set to 0 and one with it set to 1[1].

Y(b0,b1,b2,…,bi,….y,bn)=bi'y(b0,b1,b2,…,0,…y,bn)+ biy(b0,b1,b2,…,1,…y,bn) (5)

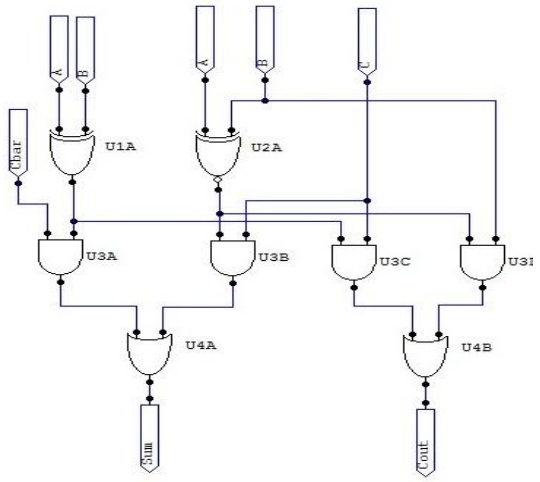

Fig7: Shannon based adder circuit

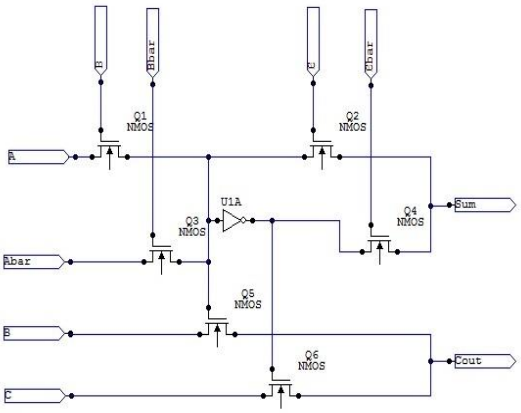

Fig8: Shannon based adder using PTL

Figure 7 shows the Shannon adder using logic gates and figue 8 shows the Shannon adder using pass transistor logic.

E. Transmission gate

Transmission gate logic consists of n-channel transistor and p-channel transistor with separate gate connections and common source and drain connection. The primary limitation of NMOS or PMOS only pass gate is the threshold drop (NMOS pass device pass a strong 0 while passing a weak 1 and PMOS pass devices pass a strong 1 while passing a weak 0). The ideal approach is to use the NMOS device to pull-down and the PMOS device to pull-up. The transmission gate combines the best of both devices by placing a NMOS device in parallel with a PMOS device.The circuit of transmission gate is shown in figure 9.

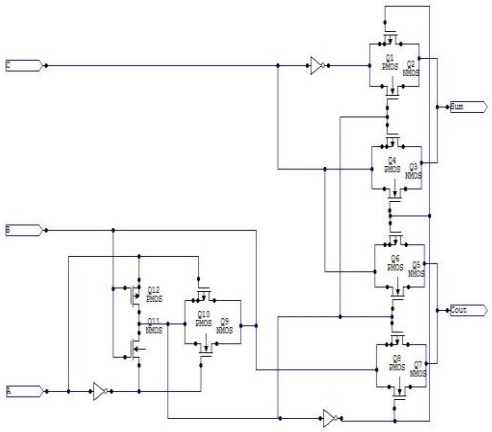

Fig.9: Transmission gate circuit

IV. SIMULATION RESULTS AND DISCUSSION

The waveform of the adder is shown below. Compared the performance of all circuits in terms of delay, area, power consumption and energy delay product. Comparison results are shown in Table 2.

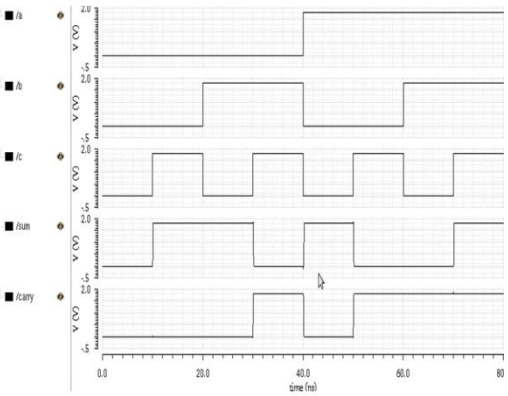

Fig.10: Waveform

TABLE II
COMPARISON

Adder Circuit using	Delay (ps)	Power consumption (uW)	Static Power (pW)	Energy delay product (zeptoJsec)	Transistor count
Logic gates	152.9	26.89	249.86	0.5841	36
Modified circuit	207.5	6.798	134.57	0.5794	26
SRPTL	44.56	8.433	206.604	0.0410	20
Shannon Based adder	30.84	27.81	506..9	0.0482	8
Transmission gates	11.05	4.078	160.435	0.0019	17

Table 2 shows the comparison of adder cells using different logic style such as logic gates,pass transistor logic,Shannon based adder and transmission gates.The comparison is in terms of delay,power consumption static power,area and transistor count. Transmission gates has the lowest total power consumption and reduced area and highest speed. Array multiplier is one of the application of adders.So the array multiplier using above mentioned adder cells using different logic styles is implemented and compared them interms of delay,area,power consumption and energy delay product.Comparison results are shown in table 3.

TABLE III
ARRAY MULTIPLIER-COMPARISON

Array multiplier using	Delay (ns)	Power consumption(uw)	Static Power (nW)	Energy delay product (zeptoJs)	Transistor count
Logic gates	50.73	170.9	2.1564	439.8	456
Modified circuit	50.47	150.6	1.7478	383.6	376
SRPTL	51.09	127.9	3.0265	333.8	256
Shannon Based adder	0.321	267.7	4.7295	0.027	160
Transmission gates	0.206	53.89	2.168	0.002	240

V. CONCLUSION

Adder cells using different logic styles such as CMOS logic, pass transistor logic , Shannon adder and transmission gates are discussed. And compared the performance of these adders in terms of delay,power,area and energy delay product.The experimental result shows that the adder cells using transmission gates have the highest speed and minimized area. It also has low power consumption and low energy delay product. The array multiplier using transmission gates have the best performance while compared to other logic styles. All these circuits are simulated in the Cadence simulation tool using 180nm technology.

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