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# Performance analysis of Effects of Parasitic Elements on the MOSFET Current–Voltage Model on its physical parameters

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**Abstract:** This work we analyze the parametric estimation for MOSFET switching delay, leakage current reduction , power dissipation and variation of temperature effects due to the parasitic devices. One solution to the problem of ever-increasing leakage is to force a non-stack device to a stack of two devices without affecting the input load. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. Logic gates after stack forcing will reduce leakage power, but incur a delay penalty, similar to replacing a low- Vt device with a high-Vt device in a dual-Vt design. Due to stacking of devices, the drive current of a forced-stack gate will be lower resulting in increased delay. Here we can design a full adder logic circuit using stack transistors.

## I. INTRODUCTION

Electronic appliances has triggered numerous research efforts in low power VLSI circuit design. The operating time of an electronic system powered with batteries is heavily restricted by its limited battery backup time. The need for reducing power dissipation in electronic systems varies from application to application. The VLSI chip circuit consist of many components, ranging from digital and analog to electro-mechanical and electro-chemical. The maximum power dissipated in the chip is due to parasitic components design inside the chip. IC power dissipats during switching or during the active mode of operation. there are two primary leakage sources, the active component and the standby leakage component. The leakage current is the current that flows between drain and source terminal when gate terminal is disacitve and no channel is present. The inactive gate terminal will leave the drain floating and their is no channel current flows. When the gate is active the the channel form between drain and source terminal , via a resistive path and enable mA range current to flow. The standby leakage may be made significantly smaller than the active leakage by changing the body bias conditions or by power-gating. For this the voltage scaling is the effective approach to reduce this power dissipation. But this voltage scaling also reduces the switching speed of the circuit, since the switching time is inversly praportional to supply voltage. To deal with this, systems may exploit dynamic voltage scaling to allow the lowest VDD necessary to meet the circuit speed requirements while saving the energy used for the computation.

### *Effect Of Parasitic Pn Junction On Switching Characteristics*

When a transistor is logically turned off, a non-zero leakage current flows through the channel due to the parasitc pn junction. This happens when the gate voltage is below the threshold voltage. Hence, this leakage current is known as subthreshold leakage. Subthreshold leakage increases significantly with technology scaling and hence is a concern in DSM designs. When the operating voltage is reduced, the threshold voltage must be reduced to compensate for the increase in delay. Reduction in threshold voltage drastically increases subthreshold leakage.

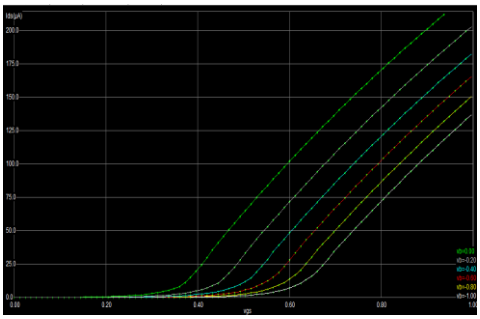

Fig 1 High leakage current VI Characteristic

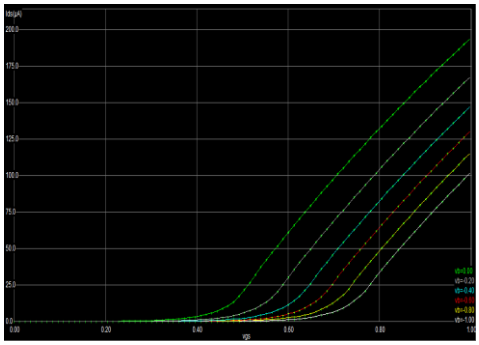

Fig 2 Low leakage current VI Characteristic

## II. SWITCHING POWER AND DELAY TRADEOFFS

We explain tradeoffs between switching power and delay in this section. In CMOS, power consumption consists of leakage power and dynamic power Dynamic power includes both switching power and short circuit power. Switching power is consumed when the transistors are in active mode and short circuit power is consume when a pull-up and pull-down network are on turning on and off. For 0.18u and above leakage power is small compared to dynamic power but 0.13u and below leakage power is dominant. Pswitching equation is for 0.18u and above are given below,

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$P_{switching} = f\ cvdd^2$

If the Vdd is small, then the Pswitching is small but it increases the Time delay of the gate.

$T_{switching} = k\ C / BVdd$

The equation above show that lowering Vdd can reduce the switching power but it increases the delay time.

***Leakage Control using transistor stack***

Power dissipation in VLSI circuits can be broadly divided into two categories: Dynamic or switching power, and Static or leakage power dissipations. Dynamic power dissipation results due to charging and discharging of internal capacitances in the circuit. Leakage power dissipation occurs during the static input state of the device. Leakage power dissipation is much more noticeable in low threshold voltage MOS transistors. This power dissipation arises because of the presence of subthreshold and gate oxide leakage currents. Subthershold leakage current flowing through a stack of series-connected transistors reduces when more than one transistor in the stack is turned off. The phenomenon whereby the leakage current through a stack of two or more OFF transistors is significantly smaller than a single device leakage is called the "stack effect". In both cases a transistor is added in series with one of the N or P networks. it will increase the resistance between the supply and ground. This decreases the gate leakage because of the transistor stack effect. Here we can design thefull adder logic circuit using stack transistor tecgnique. Fig 3 shows the layout design of full adder circuit with stack transistor connected and gate, or gate , not gate logics. The fig 4 and fig 5 shows the timing and current simulation of Full Adder Logic using stack transistors.

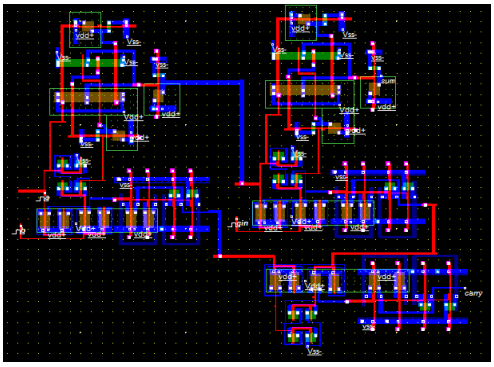

Fig 3 Layout design of Full Adder Logic using stack transistors.

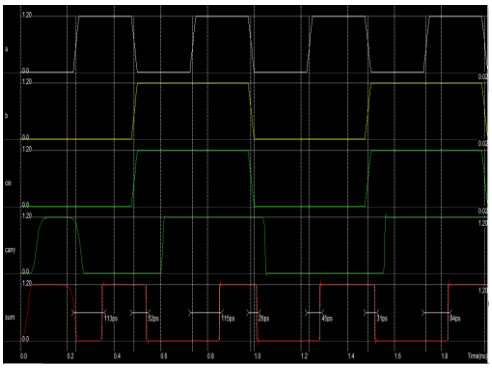

Fig 4 Timing simulation of Full Adder Logic using stack transistors.

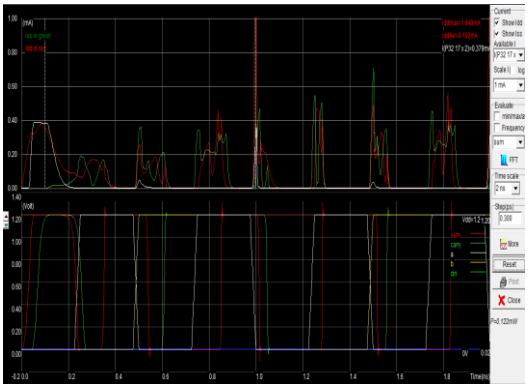

Fig 4 Current simulation of Full Adder Logic using stack transistors.

This work reviewed circuit optimization design techniques for controlling the OFF current of CMOS circuits in both standby and active modes of circuit operation. The subthreshold leakage control techniques that do not adversely affect the circuit performance and layout cost. This is especially important in light of both statistical process parameter variations and their impact on leakage currents. The average current for PMOS in this circuit is calculated as 1.948mA.

## III. CONCLUSION

A stack transistor base layout for full adder circuit is design which reduces the leakage current. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. Logic gates after stack forcing will reduce leakage power, but incur a delay penalty, similar to replacing a low- Vt device with a high-Vt device in a dual-Vt design.

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