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Design and Physical Verification of Low Power 4words X 4bits SRAM System using an Adaptive Voltage Level (AVL) Technique

Kumaraswamy N[1], Mahesh B Nelagar[2]

PG Student, VLSI Design and Embedded systems, PG Study centre VTU, Belgaum, India [1]

Asst. professor, VLSI Design and Embedded systems, PG Study centre VTU, Belgaum, India [2]

Abstract: The scaling of CMOS technology has significant impacts on SRAM cell random fluctuation of electrical characteristics and substantial leakage currents**.** Reduction of leakage current is very important for low power applications. This provides the motivation to the design of low leakage SRAM cells, because these high leakage currents are becoming a major contributor to total power dissipation of CMOS circuits. Memory leakage suppression is critically important for the success of power-efficient designs, especially for ultra- low power applications. In order to achieve low power design there many techniques are presented earlier like Multiple Vdd supply, Multiple Vth technique, SVL scheme, but these techniques will reduce only subthreshold leakages in SRAM cell and leaves gate leakage as remains. The proposed adaptive voltage level (AVL) circuit is added to Asymmetric 10T-SRAM cell, to reduce the sub-threshold leakage and as well as gate leakage, which controls the effective voltage across the SRAM cell in inactive mode. And Simulations are performed with 90nm CMOS technology process file and the leakage power and leakage currents of all the cells are measured and compared. Simulation results revealed that there is a significant reduction in leakage power for this proposed cell with the AVL circuit.

Keywords: AVL scheme, Gate leakage, Low power, Subthreshold leakage, SRAM cell.

I. INTRODUCTION

Scaling of technology will impact on several factors such as, the supply voltage, gate oxide thickness and channel length must be reduced. In future, the gate oxide thickness may be as low as 0.15nm for CMOS technologies [1]. As a result, the reduction in gate oxide thickness increases gate leakage current and subthreshold leakages in CMOS circuits. This will results high drain voltage and negative gate voltage, field crowding occurs at drain edge causing gate induced drain leakage (GIDL). And also this high drain voltage application to a short channel device results in lowering of barrier height and shifting of point of maximum barrier to the left causing drain induced barrier lowering (DIBL). If the supply voltage is below the threshold voltage, the process parameters and the variability of the SRAM increase severely [2]. Some of the SRAM stability issues are process-induced device variation, decreasing ION / IOFF and threshold voltage random variation [3]. Due to increase in Vt fluctuations and process variations, SRAM cell cannot be operated at further scaled supply voltages without functional failures causing yield loss.

In this paper we proposed a new Asymmetric 10T-SRAM cell which we have designed and compared with the conventional 6T SRAM cell. In this work we have added four extra transistors to reduce the leakage current and total power. And further more we added proposed AVL technique to Asymmetric 10T-SRAM Cell to suppress both gate leakages and subthreshold leakage.

This paper is organized as follows:
Section II covers the standard 6T SRAM cell which is the baseline for comparison with proposed Asymmetric 10T SRAM cell. Section III explains about various leakage currents occurring in the transistor of 6T-SRAM cell. Section IV presents various leakage power reduction techniques. Section V describes the proposed Asymmetric 10T-SRAM Cell. Section VI presents the 4words X 4bits memory array architecture. Section VII presents the simulation results and comparison of the proposed techniques. Section VIII gives the information about physical design of proposed method. Finally, conclusion is given in Section IX.

II. STANDARD 6T SRAM CELL

Fig.1 shows the conventional 6T SRAM bitcell. A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (P1, P2, N1, N2) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional *access* transistors (N3, N4) serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL in figure) which controls the two *access* transistors N3 and N4 which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. An SRAM cell has three different states. It can be in: *standby*, *reading* and *writing*. If the word line is not asserted, the *access* transistors N3 and N4 disconnect the cell from the bitlines, the state is called standby state. Assume that the content of the memory is a **1**, stored at Q. The read cycle is started by precharging both the bit lines to a

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logical **1**, then asserting the word line WL, enabling both the *access* transistors. The second step occurs when the values stored in Q and QB are transferred to the bit lines by leaving BL at its precharged value and discharging BL through N2 and N4 to a logical **0**. On the BL side, the transistors P1 and N3 pull the bit line toward V_{DD}, a logical **1**. If the content of the memory was a **0**, the opposite would happen and BL would be pulled toward **1** and BLB toward **0**. Then these BL and BLB will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was **1** stored or **0**. The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a **0**, we would apply a **0** to the bit lines, i.e. setting BL to **1** and BLB to **0**. A **1** is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in.

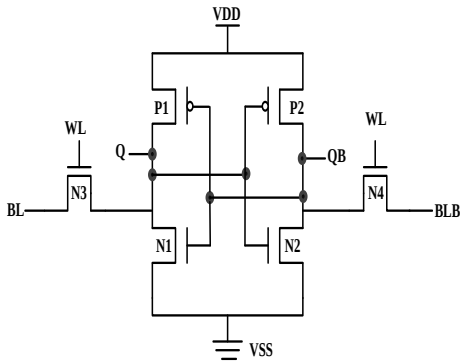

Fig.1: Basic SRAM Cell.

III. LEAKAGE CURRENTS ON SRAM

The leakage currents occurring on the SRAM cell are sub-threshold leakage current and gate leakage current, minor amount of DIBL and GIDL.

A) Sub-threshold leakage current:

The sub-threshold leakage current occurs between the drain and the source of the transistor. These leakage current occurs when the gate voltage (Vg) is less than the threshold voltage (Vth). The curve between gate source voltage (VGS) and the sub-threshold current (ISUB) is shown in fig.2.

B) Gate leakage current:

The sub-threshold leakage occurs only on the standby condition. But, the gate leakage current shown in fig.3 occurs both on the ON and OFF state.

The technology scaling results in the reduction of gate oxide thickness. This causes a high electric field and tunnelling of electrons between the substrate and gate. And this results in the gate oxide tunneling current. If positive bias is applied to gate, tunneling occurs from substrate to gate. If negative bias is applied, tunneling occurs from gate to substrate.

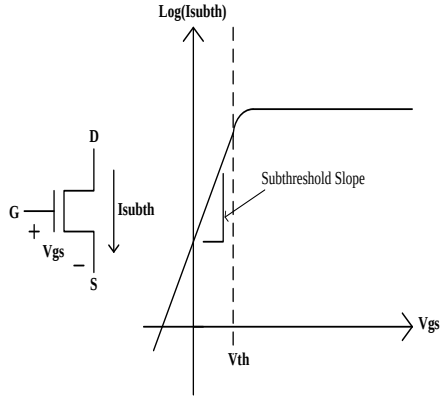

Fig.2: Sub-threshold leakage current of transistor.

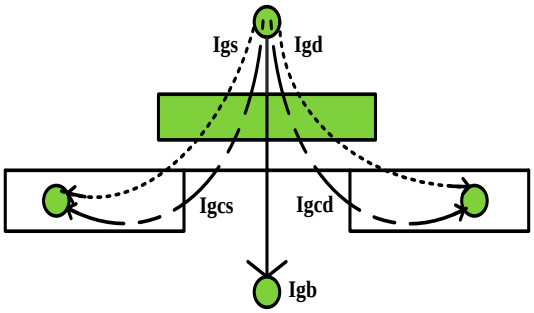

Fig.3: Gate leakage current.

C) DIBL:

The source and drain separation is large for long channel devices. In these devices, the Veto is independent of the channel length and the drain voltage. But, in the short channel devices, the source and drain separation width is small. And also the Vth is dependent on drain voltage i.e, Vth varies with the drain voltage. This is referred as Drain induced Barrier Lowering (DIBL).

D) GIDL:

Gate Induced Drain Leakage (GIDL) occurs due to the high electric field occurring in the drain junction of the transistor. It mainly occurs in the OFF state. The high drain voltage and the negative gate voltage causes field crowding at the drain edge. This process results in gate induced drain leakage known as IGIDL.

IV. LEAKAGE CURRENT REDUCTION TECHNIQUES

The various techniques for reducing the leakage current are A) Dynamic VDD B) Multiple Vth C) SVL D) AVL.

a. Dynamic VDD technique:

In the dynamic VDD scheme, normal supply voltage is given to the circuit during the active mode. During standby condition, reduced supply voltage is given. For this process, an extra peripheral circuitry known as the efficiency voltage converter is needed. These reduced supply voltage decreases the leakage current.

The Drawback *of this technique* the supply voltage reduction, results in low SNM (Static Noise Margin) and data flipping failures.

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b. Multiple Vth scheme:

The multiple Vth scheme offers both high and low threshold transistors in the same chip which can be used for dealing the leakage problem. The high threshold transistors are used for suppressing the sub-threshold leakage and the low threshold transistor is used for achieving high performance. The following methods are used for achieving multiple threshold voltages: i) Multiple channel doping ii) Multiple oxide CMOS iii) Multiple channel length iv) Multiple body bias.

c. SVL Scheme:

This reduces the leakage current and also reduces noise margin.

The drawback of this technique is that it cannot able to reduce the gate leakage current.

V. PROPOSED ASYMMETRIC 10T-SRAM CELL

The schematic of the proposed 10-transistor SRAM cell is shown in fig.4. Transistors P1-N1, P2-N2, and access transistors N3-N4 constitute the conventional 6T SRAM cell. The four additional NMOS transistors N5-N6 and N7-N8 are used to reduce power dissipation. One of the advantage of this cell is it uses the same three control signals (WL, BL and BLB) as in conventional 6T SRAM cell hence no architectural changes in the SRAM cell.

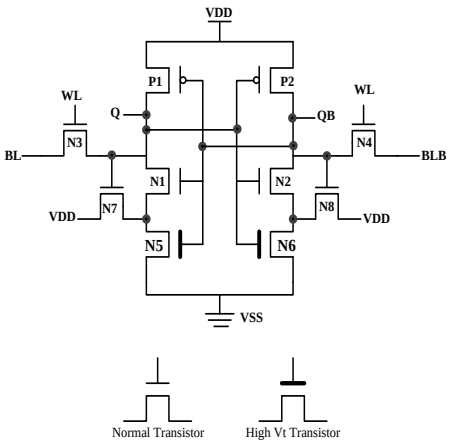

Fig.4: Proposed 10T-SRAM Cell.

Both the gate terminals of the access transistors are connected to the word line (WL) and their drain terminals are connected to bit line (BL) and bit line bar (BLB). The word line is used to activate/deactivate the cell. The bit lines are used to perform read and write operation of the cell. Two extra NMOS transistors connected to each pull down transistors of the 6T SRAM cell reduce leakage due to stack effect. Gate terminals and source terminals of other two additional NMOS transistors are connected to source terminals of the access transistors and drain terminals of pull down transistors respectively. Drain terminals of both the NMOS transistors are connected to supply voltage (V_{DD}). The two output signals Q and QB are used to store true and complement value.

A) Leakage control using AVLS:

Proposed asymmetric 10T- SRAM cell incorporating AVLS scheme is shown in Fig.5. In this scheme, a full supply voltage of VDD is applied to SRAM in active mode while a reduced supply voltage of VD is applied in inactive mode. This additional subthreshold leakage current through access transistors can be reduced by making the bit lines floating.

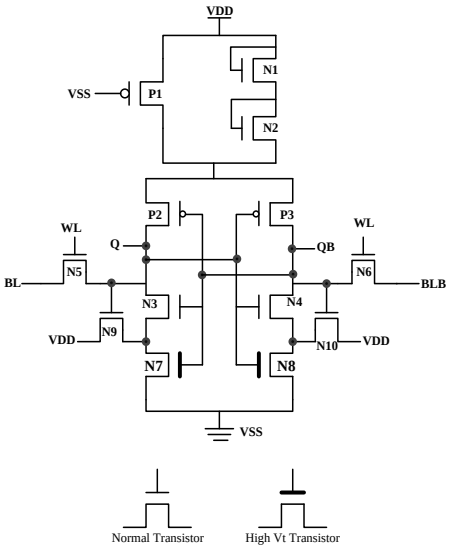

Fig.5: Proposed Asymmetric 10T-SRAM Cell with AVLS scheme.

B) Leakage control using AVLG:

Proposed asymmetric 10T-SRAM with AVLG circuit is shown in fig.6. It will provide 0V at ground node during the active mode and increased voltage during the standby mode [4]. This scheme is similar to that of the diode footed cache design scheme for controlling the leakages in SRAM. In that, a diode is designed with high threshold transistor for raising the ground level in standby mode [5].

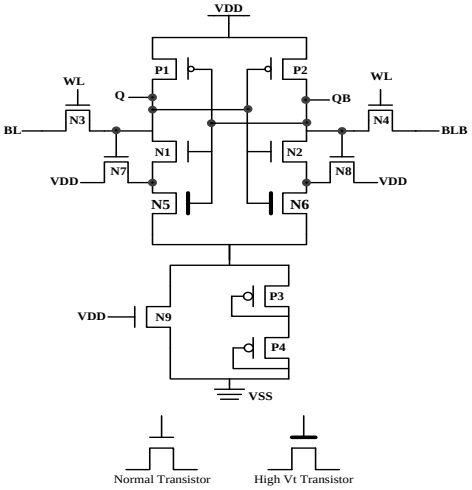

Fig.6: Proposed Asymmetric 10T-SRAM Cell with AVLG scheme.

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C) Leakage control using AVL:

This approach is the combination of both AVLS (Adaptive voltage level scaling at supply) i.e. reducing power supply to the circuit in static mode and AVLG (Adaptive voltage level scaling at ground) techniques i.e. increasing ground potential to circuit in inactive mode[6]. With reduced power supply & *increased ground potential, the leakage power is reduced to a large extent. Fig.7. shows the logic diagram for AVL technique.*

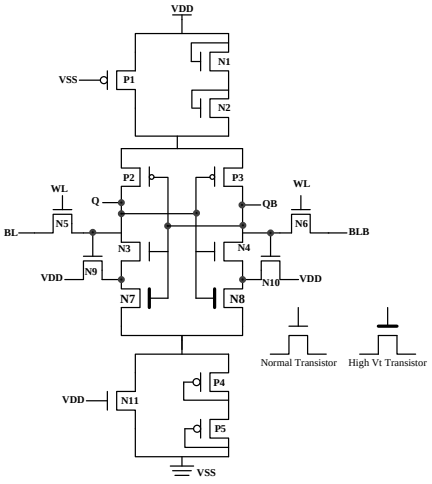

Fig.7: Proposed Asymmetric 10T-SRAM with AVL scheme.

VI. 4words X 4bits MEMORY ARRAY ARCHITECTURE

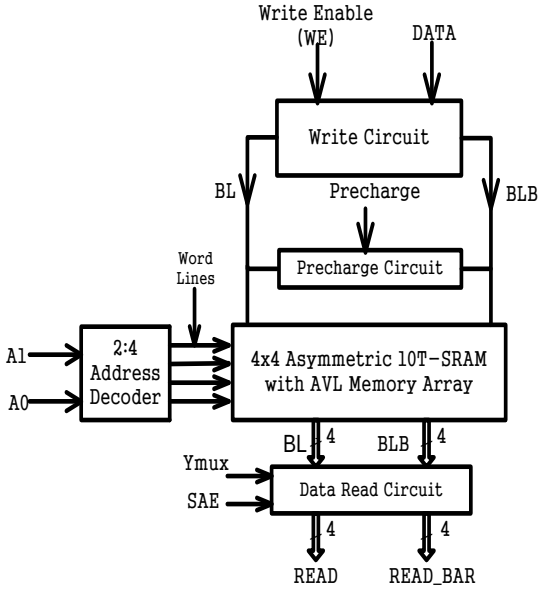

Fig.8: Block Diagram of 4words x 4bits Asymmetric 10T-SRAM with AVL Memory System.

4words x 4bits array for SRAM system is shown as a block diagram in fig.8. The 4x4 array for SRAM system is implemented using sixteen Asymmetric 10T SRAM with AVL cells. These are divided into 4-columns of 4-bits each. Sixteen Asymmetric 10T-SRAM with AVL cells, address decoder, precharge circuitry, data write circuitry, and sense amplifiers are designed to cater to the 4words x4bits SRAM array in 90nm technology. The complete top level schematic of data write and read for memory array system is shown in Figure.9. This schematic shows all the different peripheral circuits combined with the static RAM cells, and forms a complete working SRAM system for data write and read.

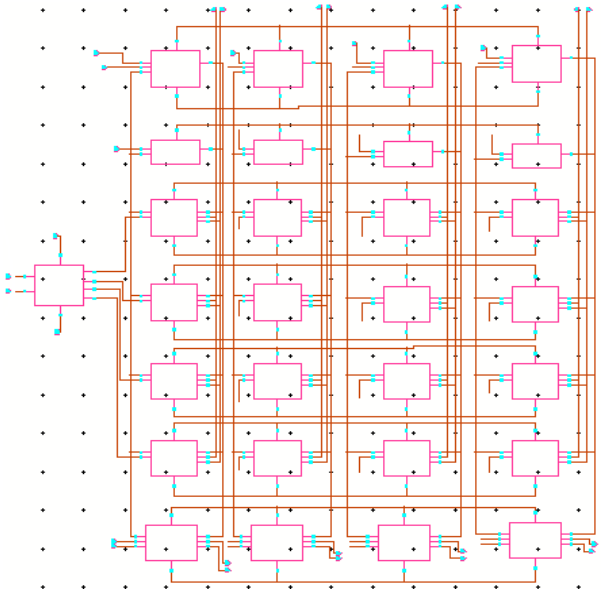

Fig.9: Top Level Schematic of 4words x 4bits SRAM System.

a) Address Decoders:

Address decoders drive the signals that go across the memory core. It drives WL which traverses through all the memory cells in each row of the memory system. Lyon-Schediwy 2:4 decoder [6] shown in fig.10. is adapted to the proposed SRAM array system to address 16 bit capacity of memory and in order to reduce area and power. It activates the WL signal which is necessary for selecting one of the rows. It has two input lines A_0A_1 and eight output word lines (WL_0-WL_3). These output word lines are connected to each cell in every row. This address decoder is connected to SRAM system as shown in the fig.8.

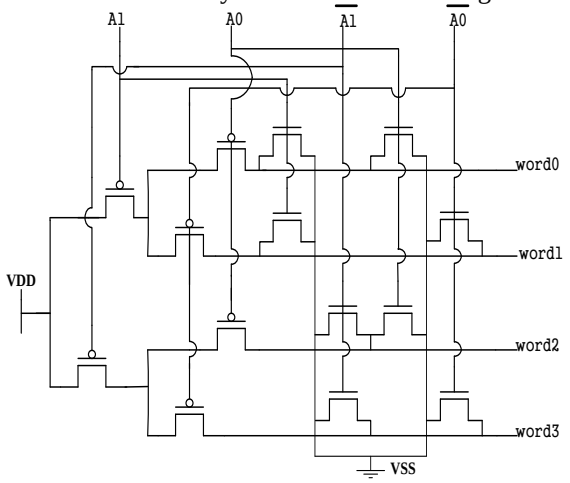

Fig.10: Lyon-Schediwy 2:4Row Decoder.

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b) Precharge circuit:

Precharge circuit [7] which is shown in fig.11 are employed in order to precharge BLs to VDD before the start of read cycle which is necessary for proper sensing. During the read operation, the precharged bitlines either retain charge or discharge depending on the data stored in the SRAM cells selected by WL. Fig.8 shows the position of the precharge circuit in a SRAM column.

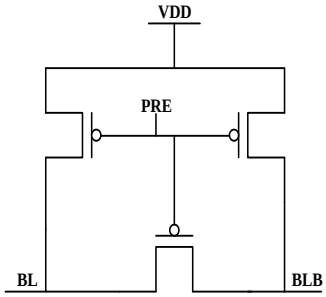

Fig.11: Precharge Circuit.

c) Write Column Circuit:

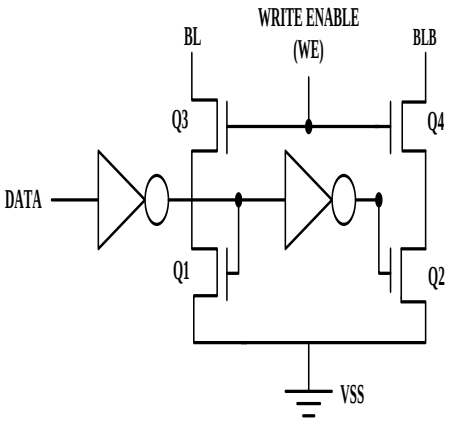

Fig.12: Write Driver circuit.

Write driver circuit is employed in each column of the memory array system. This circuit is activated by enabling the WE (write enable) signal. Once the WE signal is enabled, it starts writing the data and its complement into the internal nodes Q and QB through access transistors of the SRAM cell. Fig.8 shows the position of the write circuit in single column SRAM system. Fig.12 shows the circuit diagram of write driver which consists of 8-transistors.

d) Read Column Circuit:

An analog differential sense amplifier [8] shown in fig.13 is used as a read circuit for reading the data in the SRAM system. This is activated for read operation by enabling the signal SAE. Every column in the SRAM system has one read circuit. Fig. 5 shows the position of the Sense Amplifier in single column SRAM system.

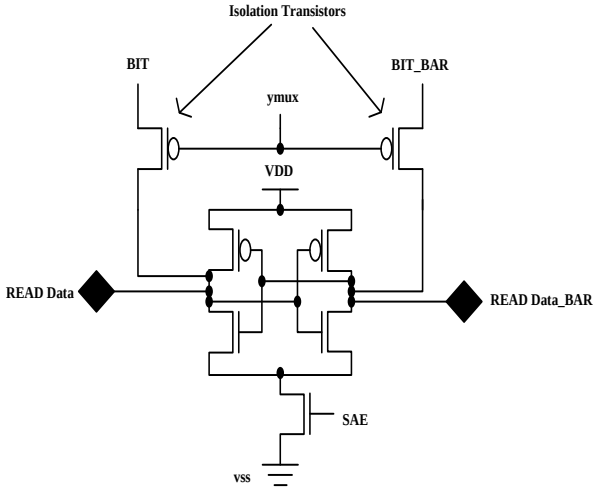

Fig.13: Sense Amplifier.

VII. SIMULATION RESULTS AND DISCUSSIONS

This section describes the simulation results verified for 4 cycles of 'Read' and 'write' operations. All simulations have been performed with *Cadence* 90nm CMOS process Technology. To design and simulate the SRAM cell, *Cadence Virtuoso* Schematic Editor is used and verified the functionality through simulations using *Cadence Virtuoso Spectre* tool. Using *Cadence Virtuoso ADE* Visualization and Analysis XL Browser and XL Calculator power dissipation is measured. The layout is drawn and verified for *DRC, LVS and RC* extraction using *Cadence Assura* tool. Fig.14 shows the transient response of single cell Asymmetric 10T-SRAM. Figs.15, and 16 are the simulated waveforms for 4 X 4 Asymmetric 10T-SRAM with AVL system 'Writing' and 'Reading' and figs. 17 and 18 shows the waveforms for single column 'Writing' and 'Reading'. And fig.19 shows leakage currents on different 4 X 4 SRAM memory systems.

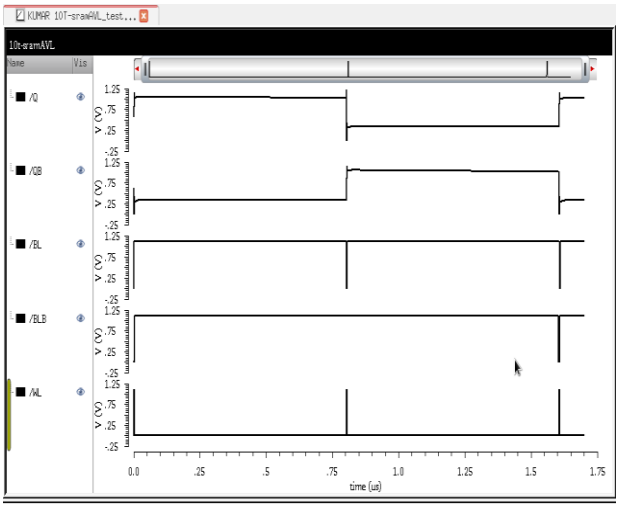

Fig.14: Waveforms of Asymmetric 10T-SRAM with AVL Cell.

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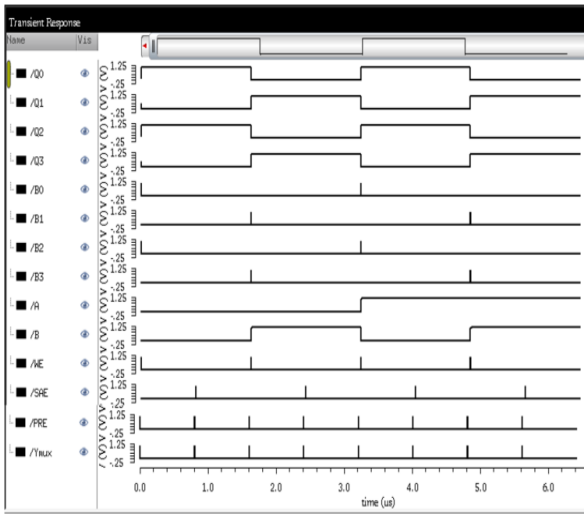

Fig.15: Simulation results of Asymmetric 10T-SRAM with AVL 4 x 4 memory system for writing data 0101.

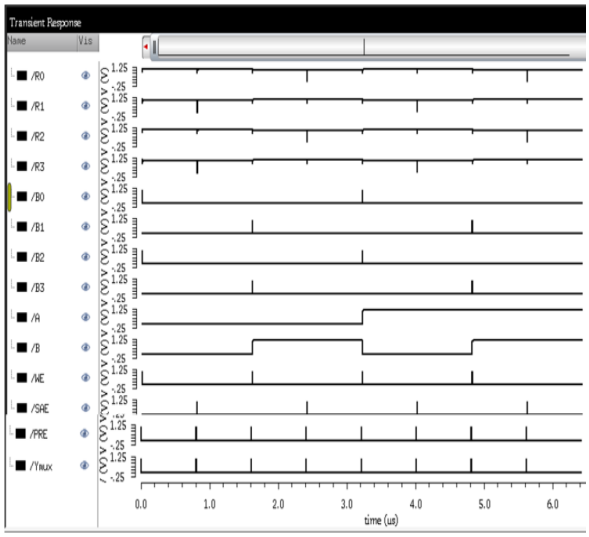

Fig.16: Simulation results of Asymmetric 10T-SRAM with AVL 4 x 4 memory system for reading data 0101.

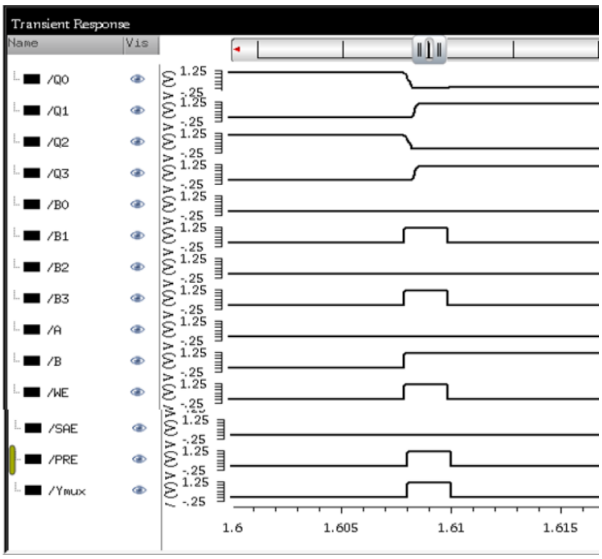

Fig.17: Simulation results of Asymmetric 10T-SRAM with AVL single column system for writing data 0101.

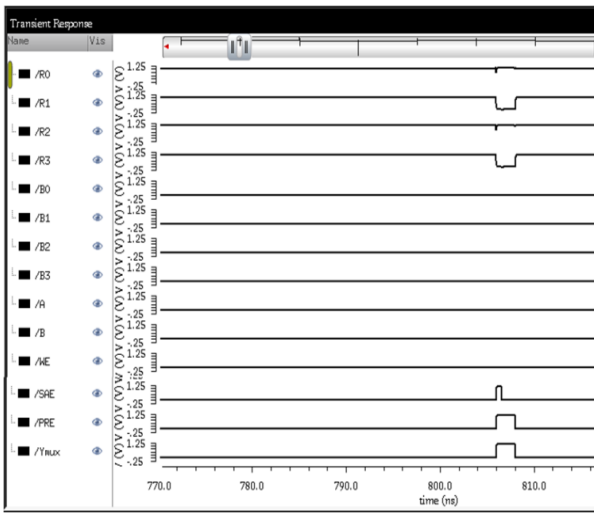

Fig.18: Simulation results of Asymmetric 10T-SRAM with AVL single column system for writing data 0101.

Table I: Total Power dissipation, and Leakage Current for 4 X 4 SRAM Memory system (VDD = 1.1V)

4X4 SRAM array systems	Total Power(µW)	Leakage Current(µA)
Conventional 6T-SRAM	767.4	696.67
10T-SRAM	542.6	494.199
10T-SRAM with AVLS	542.3	493.363
10t-SRAM with AVLG	315.48	286.8
10T-SRAM with AVL	304.466	276.787

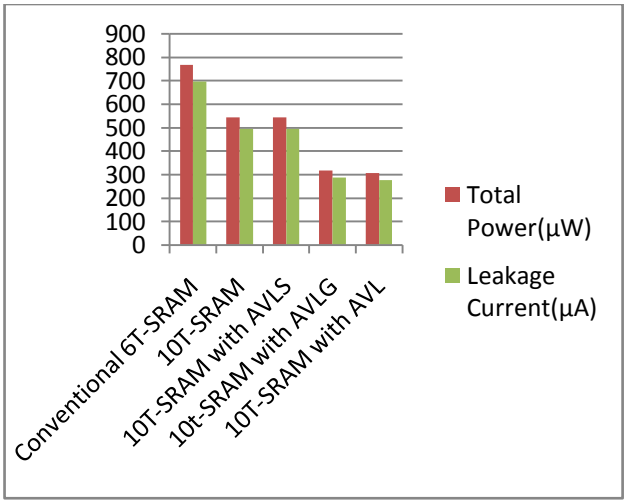

Fig.20: Power and Leakage currents Comparison for different 4 X 4 SRAMs.

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VIII. Physical Design

Physical implementation of single bit Asymmetric10T SRAM with AVL (fig.21) and 4 X 4 Asymmetric 10T SRAM with AVL system (fig. 22) is developed using *Cadence virtuoso layout* tool and verified the layout for *DRC*, *LVS* and *RCX* using *Cadence Assura tool* and no errors were found.

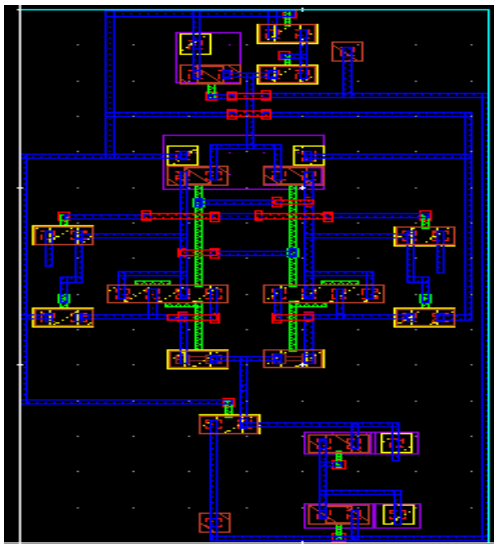

Fig.21. Layout of Asymmetric 10T-SRAM with AVL cell.

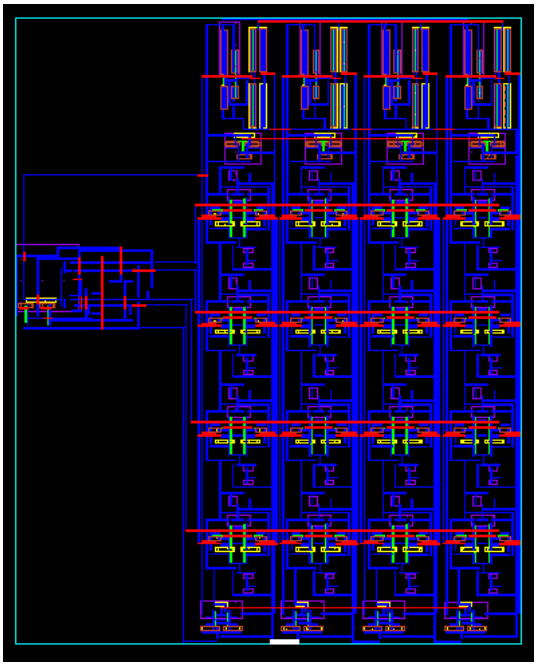

Fig.22. Layout of 4 x 4 Asymmetric 10T-SRAM with AVL Array

IX. CONCLUSION

In this work, 4words X 4bits array functional asymmetric 10T SRAM with AVL methods are implemented in 90nm CMOS process technology. After comparing the results of proposed SRAM with conventional SRAM, the proposed SRAM has good performance while reducing power dissipation and leakage currents. Simulation results show that the proposed SRAM cell achieves low leakage as well as total power dissipation with better data retention at 1.1V supply voltage

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BIOGRAPHIES

Kumaraswamy N was born in Tumkur, Karnataka, India in 1990. He received the B.E degree in Electronics and Communicaion from Visvesvaraya Technological University, Belgaum, India in 2012. He is currently pursuing M.Tech in VLSI Design and Embedded System at Dept of PG Studies, Visvesvaraya Technological University, Belgaum. Research interests are Low Power Memory Design.

Mahesh B Neelagar was born in Bagalkot, Karnataka, India in 1984. He received the B.E degree in Electronics and Communicaion from Visvesvaraya Technological University(VTU), Belgaum, India Further he received MTech degree from same university in VLSI Design & Embedded Systems course. He is currently working as Assistant Professor in VLSI Design and Embedded System Dept at PG Studies, VTU, Belgaum. He has 2 years of teaching experience .Area of Research interest are VLSI Design &Real time embedded system design.