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Design of a Variable point FFT processor for 4G Standards

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Abstract: In this paper, We propose a design of a variable point FFT processor using FPGA in which OFDMA Technology is applied. The FFT processor use Verilog HDL language to describe the circuit, use Quartus II 7.2 software to build the model, and use ModelSim SE 6.2b software to verify the timing function. Therefore, this design can be applied to real-time signal processing system, completes the main computing modules in the OFDMA system. The performance of the system is analyzed using MATLAB software and the result shows that The SINR of wireless OFDMA in the presence of CFO (carrier frequency offset) and frequency selective fading becomes a ratio of correlated random variables, and recent research results have not provided exact expressions for its average. In this paper, we have presented a new non-direct mathematical analysis which led to the derivation of a simple new expression for the average SINR of OFDMA in the presence of CFO over multipath Rayleigh fading.

Keywords: FPGA, OFDMA, CFO

I. INTRODUCTION

In telecommunications, 4G is the quarter cohort of cellular wireless standards. It is a replacement to 3G and 2G class of standards. Speed demands for 4G service set the peak download speed at 100 Mbit/s is aimed at high kinesis communication[1] (such as from trains as well as cars) plus 1 Gbit/s is aimed at truncated kinesis communication (such as ramblers as well as stationary users).

A 4G system is expected to provide a comprehensive and secure all-IP based mobile broadband solution to laptop computer wireless modems, smartphones, and other mobile devices. Facilities such as ultra-broadband Internet access, IP telephony, gaming amenities, plus gushed multimedia may possibly be provided to manipulators.

Pre-4G technologies such as mobile WiMAX and first-release 3G Long term evolution (LTE) have been on the market since 2006 and 2009 respectively, and are often branded as 4G. The current versions of these technologies did not fulfill the original ITU-R requirements of data rates approximately up to 1 Gbit/s for 4G systems. Marketing materials use 4G as a description for Mobile-WiMAX and LTE in their current forms.

IMT-Advanced acquiescent varieties of the exceeding binary ethics are under development and baptized as “LTE Advanced” and “Wireless MAN-Advanced” correspondingly. ITU has unequivocal that “LTE Advanced” and “Wireless MAN-Advanced” should be accorded the official designation of IMT-Advanced[3]. On December 6, 2010, ITU announced that current versions of LTE, WiMax and other evolved 3G expertise that do not bear out "IMT-Advanced" requirements could be considered "4G", so long as they epitomize harbingers to IMT-Advanced plus "a sizable level of enhancement in recital and competencies per esteem to the preliminary third cohort systems currently arrayed."

In all suggestions for 4G, the CDMA spread spectrum wireless technology cast-off in 3G systems and IS-95 is abandoned and replaced by OFDMA and former frequency-domain equalization chaos. This is combined with MIMO (Multiple In Multiple Out), e.g., multiple antennas, dynamic channel allocation and channel-dependent scheduling.

Orthogonal Frequency Division Multiple Access (OFDMA) is a cellular air interface used in 4G communications networks such as WiMAX and LTE, based on OFDM for multiple, simultaneous users. OFDMA has several benefits ranging from increased flexibility to improved throughput and robustness[4]. By assigning subchannels to specific subscribers, transmissions from several subscribers can occur simultaneously without interfering, thus minimizing an effect known as Multiple Access Interference (MAI). Furthermore, sub channelization enables the concentration of transmit power over a reduced number of subcarriers. This results in increased link margins which in turn, lead to improved range and coverage.

- OFDMA is a variant of orthogonal frequency multiplexing (OFDM), a alphanumeric multi carrier modulation chaos that is widely used in wireless systems.
- Rather than transmitting a high data frequency brook of data with a sole hauler, OFDM makes habit of a hefty number of meticulously spaced orthogonal sub carters that are conveyed in parallel.
- A piece sub carrier is tempered by means of a unadventurous modulation scheme such as QPSK, 16QAM, 64QAM at a low symbol rate.
- The amalgamation of hundreds and thousands of sub carriers empowers data rates analogous to conventional sole carrier modulation chaos in the identical bandwidth.

In the stint purview, sentinel recesses are interleaved between each of the cryptograms to thwart inter symbol

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interference at the receiver instigated by multi path delay spreading the wireless channel.

II. PROBLEM DESCRIPTION

Orthogonal frequency-division multiplexing (OFDM) has become very popular in wireless communications. After its adoption in the recently developed wireless local area network (LAN) and broadband wireless access (BWA) standards, this technique is seen today as a strong candidate for future generations of cellular mobile networks. In current systems, OFDMA is used with time-division multiple access (TDMA), i.e., users sequentially share the available radio resources and all carriers are allocated to the equivalent manipulator in the course of a prearranged OFDMA symbol. A second possibility for the access scheme is to combine OFDM with code-division multiple access (CDMA), a technique that is known as multicarrier CDMA (MC-CDMA).

A third possibility is to use orthogonal frequency division multiple access (OFDMA), in which different groups of carriers are assigned to different users. This technique has a number of interesting features, the basic one for wireless communications systems being that it increases the achievable cell range for a given transmit power. Indeed, the transmit power available at the user terminal in TDMA and CDMA systems is transmitted over the entire channel bandwidth. In contrast, the same power only occupies (1/M)th of this bandwidth in an OFDMA system, which splits the total number of carriers N into M groups of N/M carriers each and assigns these groups to different users. For a given transmit power, such an OFDMA system gains 10log(M) dB in terms of signal-to-noise ratio (SNR) on the uplink, and this translates into a substantial range extension.

OFDMA also leads to range extension on the downlink by allocating more power to the group of carriers assigned to distant users and less power to the group of carriers assigned to users that are close to the base station. While the reduced user signal bandwidth is an advantage for OFDMA in terms of cell range, it increases sensitivity to multipath fading. This is particularly true in OFDMA with clustered carriers, where all carriers assigned to a user may fade simultaneously[8]. In terms of robustness to frequency-selective fading, the second variant of OFDMA, which uses groups of carriers that are regularly spaced across the channel bandwidth, is more appealing. But if encoded, this variant too is sensitive to multipath fading and requires channel coding to reduce its sensitivity. Therefore, exactly as in OFDM, the conventional approach to combat multipath fading in OFDMA is to use error correction coding. In this paper, we investigate another technique to cope with multipath disappearing in spaced-carrier OFDMA[4]. It entails of coalescing OFDMA with code division multiplexing (CDM) such that the vigor of data cryptograms is banquet across the carriers allocated to the equivalent manipulator. This scattering convalesces a prodigious transaction of the frequency assortment forfeiture that is intrinsic to mutually OFDM transmission and OFDMA-based networks.

III. PROPOSED SYSTEM

We propose a design of a variable point FFT processor using FPGA in which OFDMA Technology applied. The FFT processor use Verilog HDL language to describe the circuit, use Quartus II 7.2 software to build the model, and use ModelSim SE 6.2b software to verify the timing function. Therefore, this design can be applied to real-time signal processing system, completes the main computing modules in the OFDMA system.

The performance of the system is analyzed using MATLAB software and the result shows that The SINR of wireless OFDMA in the presence of CFO (carrier frequency offset) and frequency selective fading becomes a ratio of correlated random variables, and recent research results have not provided exact expressions for its average. In this paper, we have presented a new non-direct mathematical analysis which led to the derivation of a simple new expression for the average SINR of OFDMA in the presence of CFO over multipath Rayleigh fading.

A. FFT PROCESSOR

The FFT module is the core part in the OFDMA system, IEEE Std 802.16-2005 [7] defined clearly: the core module of OFDMA physical layer is the FFT module, which can be used in the FFT points are: 2048 points (back compatible with IEEE Std 802.16-2004), 1024 points, 512 points and 128 points. The design about variable point FFT processor is just based on FFT module in OFDMA system application.

B. 64 point FFT module

This module is the most frequently used in the design. Four kinds of input data length all must first pass through the 64 points FFT module. The same idea in the module based on 2D Fourier transform algorithm is composed of two 8-point FFT modules. So 8-point FFT module is the kernel in this part, its performance affects the whole design.

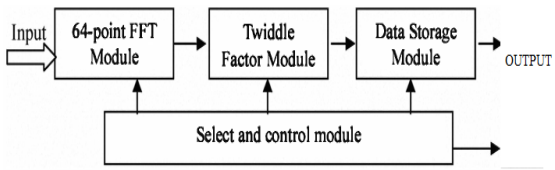

Fig 1. Block diagram of overall design of FFT processor

The 8-point FFT processor architecture consists of a single radix-2 butterfly (which is referred as the butterfly processing element), a dual-port FIFO RAM, a coefficient ROM, a controller and an address generation unit. The Input data is [1 -1 0.5 -3 2 -2.5 0 4] and the result of 8-point FFT module and the result of MATLAB are shown in Table 1.

It is inferred that: the results of the 8-point FFT module match that from Matlab. And the result error is within the allowable range. Therefore, it's acceptable to adopt the 8-point FFT processor as the kernel module of the 64-point FFT module.

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TABLE I. Comparison of

Results of S-point FFT		Results of Matlab
Rea/parts	11Ulginaryparts	
I	0	1.0000
5.01045	3.38915	5.0104 + 3.389li
2.50005	4.50005	2.5000 + 4.5000i
-7.01045	4.38915	-7.0104 + 4.389li
6	0	6.0000
-7.01045	-4.38915	-7.0104 -4.3891i
2.50005	-4.50005	2.5000 - 4.5000i
5.01045	-3.38915	5.104 -13891i

C. Altera FPGA

A Field-Programmable Gate Array (FPGA) is an cohesive circuit premeditated to be arranged by the customer or designer after manufacturing hence "field-programmable". The FPGA configuration is usually itemized by means of a hardware description language (HDL), comparable to that rummage-sale for an application-specific integrated circuit (ASIC). FPGAs can be rummage-sale to contrivance any logical function that an ASIC might achieve. The capability to modernize the functionality after conveyance, partial re-configuration of the slice of the proposal and the squat non-recurring manufacturing costs comparative to an ASIC design (nevertheless the commonly sophisticated unit cost), bargain pluses for sundry applications. It can be constructed to achieve multifaceted combinational functions, or purely unpretentious logic gates like AND and XOR. In maximum FPGAs, the logic blocks also embrace memory rudiments, which may be unpretentious flip-flops or additional comprehensive chunks of memory.

TABLE II. Features Offered In FPGA

Features	Xilinx virtex II Pro	Altera stratix	Actel axcelerator	Lattice is pXPGA
Clock management	DCM Up to 12	PLL Up to 12	PLL Up to 8	Sys CLOCK PLL up to 8
Embedded memory blocks	Block RAM Up to 10 Mbit	Tri Matrix Memory Up to10 Mbit	Embedded RAM Up to 338K	Sys MEM Blocks Up to 414K
Data processing	CLB and 18-bitx 18-bit Multipliers	LE's and embedded multipliers	Logic modules (C-cell &R-cell)	PFU based
Programmable I/O s	Select IO	Advanced IO Support	Advanced IO Support	Sys IO
Special features	Embedded power PC405 Cores	DSP blocks	Per pin FIFO's for bus application	Sys Hs 1 for high speed serial interface

D. De0 altera cyclone iii kit

The Procedure For Downloading A Circuit From A Host Computer To The DE0 Board Is Described In The Tutorial Quartus II Introduction. This Tutorial Is Found In The DE0_Tutorials Folder On The DE0System CD-ROM, And It Is Also Available On The Altera DE0 Web Pages. The User Is Encouraged To Read The Tutorial First, And To Treat The Information Below As A Short Reference The DE0 board contains a serial EEPROM chip that stores configuration data for the Cyclone III FPGA. This configuration data is automatically loaded from the EEPROM chip into the FPGA each time power is applied to the board. Using the Quartus II software, it is possible to reprogram the FPGA at any time, and it is also possible to change the non-volatile data that is stored in the serial EEPROM chip. Both types of programming methods are described below. JTAG programming: In this method of programming, named after the IEEE standards Joint Test Action Group, the configuration bit stream is downloaded directly into the Cyclone III FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration is lost when the power is turned off.

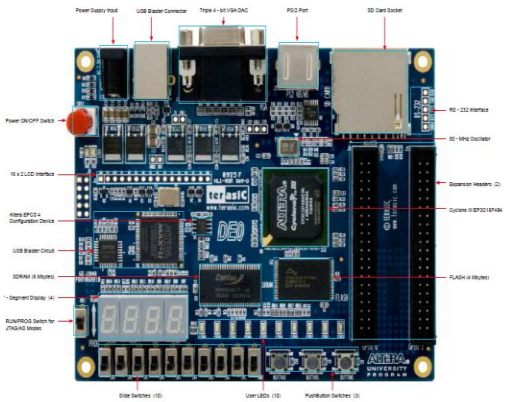

Fig 2. ALTERA FPGA KIT

AS programming: In this method, called Active Serial programming, the configuration bit stream is downloaded into the Altera EPCS16 serial EEPROM chip. It provides non-volatile storage of the bit stream, so that the information is retained even when the power supply to the DE0 board is turned off. When the board's power is turned on, the configuration data in the EPCS16 device is automatically loaded into the Cyclone III FPGA. The sections below describe the steps used to perform both JTAG and AS programming. For both methods the DE1 board is connected to a host computer via a USB cable. Using this connection, the board will be identified by the host computer as an Altera USB Blaster device. The process for installing on the host computer the necessary software device driver that communicates with the USB Blaster.

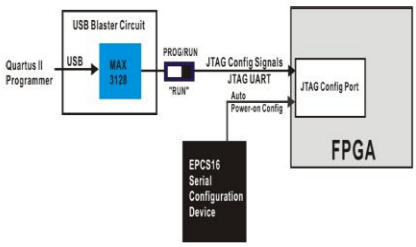

Fig 3. The JTAG Configuration Scheme

To download a configuration bit stream into the Cyclone III FPGA, perform the following steps:

- Ensure that power is applied to the DE0 board
- Connect the supplied USB cable to the USB Blaster port on the DE0 board.
- Configure the JTAG programming circuit by setting the RUN/PROG switch (on the left side of the board) to the RUN position.

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- The FPGA can now be programmed by using the Quarts II Programmer module to select a configuration bit stream file with the .sof filename extension.

To download a configuration bit stream into the EPCS16 serial EEPROM device, perform the following steps:

- Ensure that power is applied to the DE0 board
- Connect the supplied USB cable to the USB Blaster port on the DE0 board.
- Configure the JTAG programming circuit by setting the RUN/PROG switch (on the left side of the board) to the PROG position.
- The EPCS4 chip can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the .pof filename extension

Once the programming operation is finished, set the RUN/PROG switch back to the RUN position and then reset the board by turning the power switch off and back on; this action causes the new configuration data in the EPCS4 device to be loaded into the FPGA chip. In addition to its use for JTAG and AS programming, the USB Blaster port on the DE0 board can also be used to control some of the board's features remotely from a host computer. The DE0 board provides four pushbutton switches. Each of these switches is de-bounced using a Schmitt Trigger circuit. The four outputs called KEY0… KEY3 of the Schmitt Trigger device are connected directly to the Cyclone III FPGA. Each switch provides a high logic level (3.3 volts) when it is not pressed, and provides a low logic level (0 volts) when depressed. Since the pushbutton switches are de-bounced, they are appropriate for use as clock or reset inputs in a circuit.

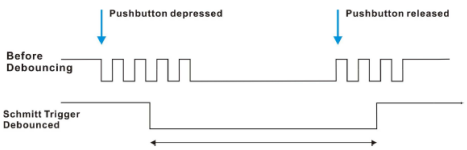
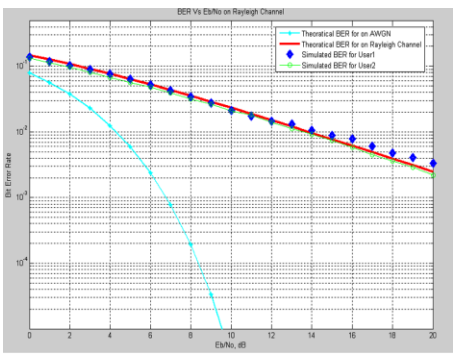


Fig 4. Switch De-bouncing

There are also 10 toggle switches (sliders) on the DE0 board. These switches are not de-bounced, and are intended for use as level-sensitive data inputs to a circuit. Each switch is connected directly to a pin on the Cyclone III FPGA. When a switch is in the DOWN position (closest to the edge of the board) it provides a low logic level (0 volts) to the FPGA, and when the switch is in the UP position it provides a high logic level (3.3 volts).

IV. SIMULATION RESULTS



Performance of OFDMA The results confirm that at the BER of 10 to 5, an SNR gain of approximately 3 dB is achieved when the size of the carrier groups and the spreading factor are doubled. This gain holds only for the first steps and it decreases at further steps, so that in the limit (with SF = 64), performance of this scheme coincides with that of MC-CDMA. The figure also shows the matched filter bound (MFB), which is approximately 10 dB to the left from the OFDMA performance on this channel.

V. CONCLUSION

In this paper, a variable point FFT processor was designed using FPGA and was applicable to OFDMA system successfully. The processor use Verilog HDL language to describe the circuit, use Quartus II 7.2 software to build the model, and use ModelSim SE 6.2b software to verify the timing function. The results showed that: the successful completion of the design altered input points FFT computation, design precision 16-bit, and limited to 100MHz clock frequency, the overall timing design stability, FFT processing result was correct. Therefore, this design can be applied to real-time signal processing system, completes the main computing modules in the OFDMA system. The performance of the system is analyzed using MATLAB software and the result shows that The SINR of wireless OFDMA in the presence of CFO and frequency selective fading becomes a ratio of correlated random variables, and recent research results have not pro-vided exact expressions for its average. In this paper, we have presented a new non-direct mathematical analysis which led to the derivation of a simple new expression for the average SINR of OFDMA in the presence of CFO over multipath Rayleigh fading.

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