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Design of SPI to I2C Protocol Converter and Implementation of Low Power Techniques

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Abstract- Enabling embedded systems having only SPI interfaces to connect with I2C peripherals provides design flexibility through interoperability and power flexibility. But SPI interfaces cannot directly connect with I2C peripherals. The best way to deal with this problem is to create an SPI to I2C interface using protocol converter. Protocol Converters are generally used for transforming data and commands from one device or application to another. This work mainly focuses on protocol conversion from SPI to I2C through "read" and "write" commands. Also an effective low power technique such as clock gating insertion, dynamic power gating and use of Multi-threshold standard cells for reducing leakage power are implemented over this design.

Key words: SPI, I2C, Protocol converter, Low power Techniques.

I. INTRODUCTION

Serial Peripheral Interface (SPI) is the interface present in most of the embedded systems. SPI supports full duplex communication with higher throughput. Whereas Inter Integrated Circuit (I2C) is a two wired bus used to enable communication between two or more devices that are normally on the same board. The throughput of I2C is normally less than that of SPI. In order to connect embedded systems having only SPI interfaces to I2C peripheral devices to achieve power and design flexibilities, SPI to I2C protocol converter is implemented.

Technology trends and specially portable applications drive the quest for low power VLSI design. The focus is on developing low power circuits without affecting too much on the performance (area, latency,

speed). Hence a novel approach of low power technique called dynamic power.

Gating is used over the implementation of SPI to I2C protocol converter. The rest of the paper is organised as follows. In the next section the implementation of SPI to I2C protocol converter is explained. The dynamic power gating which is a low power technique is explained next. The results of the implementation are presented in the section IV. Finally the conclusion and futurescope is dicussed.

II SPI TO I2C PROTOCOL CONVERTER

A Protocol Converter is a device used to convert standard or proprietary protocol (for example SPI) of one device to the protocol (for example I2C) suitable for the other device or tools to achieve the interoperability. Figure1 shows the block diagram of SPI to I2C protocol converter. The proposed architecture is as follows: The SPI to I2C protocol converter will contain one internal SPI slave and internal I2C master. All the requests signals will be generated by master block. When an external SPI master wants to read/write data into external I2C slave, it will send the read/write command and corresponding address of I2C slave through

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internal SPI slave. SPI slave then sends the command, address and data (in case of write) to the I2C master and the internal state machine will do the necessary data conversion.

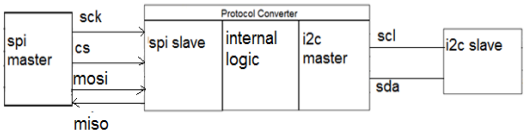

Figure1: Block diagram of SPI to I2C protocol converter

The sequence of actions that take place in the internal logic of the protocol converter are as follows:

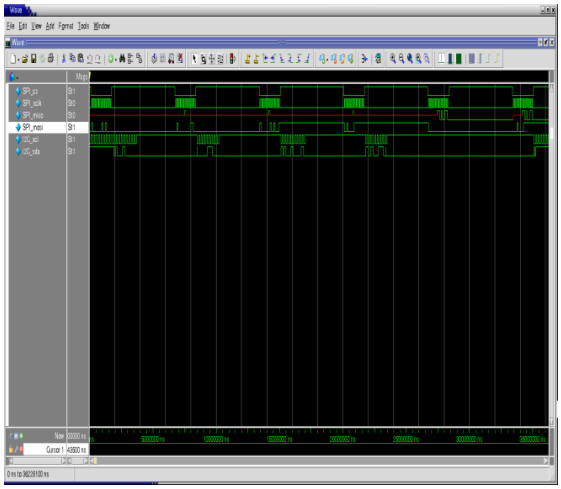

Figure2: SPI to I2C read and write operation

➢ SPI first sends the Start bit command and the external I2C slave address. For example SPI sends Start bit command as 8'h80 and slave address of 8'h90. This is shown in the first clock phase of SPI sclk in the waveform.

The above signal is converted into I2C protocol format. The following information is obtained on the sda line.

Start bit (0)	7bit address	Write command (0)	Acknowledgment (0)

This has been shown in the 1st clock phase of scl in the waveform.

➢ SPI sends the write command and data to be written into the external I2C slave. For example SPI sends write command 8'h40 and data 8'0C. This is shown in the second clock phase of SPI_sclk in the waveform.

The data is send through sda line to the I2C slave. This has been shown in the 2nd clock phase of scl clock.

➢ SPI send Repeat Start bit command and external I2C slave address for read operation. For example SPI send 8'h80 and 8'h91. Shown in 3rd clock phase of SPI sclk.

The above information is converted into I2C format. Now this time start bit is converted to Repeat Start bit and the address converted to 7bit address followed by Read command (1) and acknowledgement (0). This is shown in 3rd clock phase of scl.

➢ SPI sends the Read command and dummy bit. Wait for two cycles by sending some dummy bit and then read the data from I2C. For example SPI reads data h'A6 from I2C.

➢ Finally SPI sends the Stop bit command which is represented by stop bit (1) in the sda line.

This SPI to I2C protocol converter design is simulated using modelsim simulator. This design can be implemented on FPGA and is power friendly. Hence low power techniques can be applied over this design.

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III IMPLEMENTATION OF LOW POWER TECHNIQUES

Following Low power techniques have been implemented for this design in order to calculate power.

- Clock Gating Insertion
- Dynamic Power Gating
- Use of Multi-Threshold standard cells for reducing leakage power.

Clock gating: It is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating.

Dynamic Power Gating: It is effective for reducing leakage power. Power gating is the technique wherein circuit blocks that are not in use are temporarily turned off to reduce the overall power of the chip. This temporary shutdown time can also call as "low power mode" or "inactive mode". But power gating comes with following overhead. Power gating affects and adds lot of complexity to the design much more than compared to the clock gating. It increases time delays as power gated modes have to be safely entered and exited. The possible amount of leakage power saving in such low power mode and the energy dissipation to enter and exit such mode introduces some architectural trade-offs. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is the other option

Use of Multi-Threshold Standard Cells: Each design has some timing critical area and timing non critical area. The timing non critical area design should be designed with high threshold voltage standard cells where as the critical area should be designed with low threshold voltage standard area. High threshold value cells are slower are speed but consumes less leakage power. However there are certain limitations such as high delay and thus leading to degraded performance, and it involves multiple timing trials.

In order to calculate power for the design several things such as synthesis, physical design and power analysis have to be performed.

Clock gating cell has been introduced through synthesis. The tool used is Design Compiler with 28 nm technology, ss3sigma operating condition and 50 MHz operating frequency.

The basic physical design flow is implemented in Magma Talus tool which is as follows:

Fix Time (hyper cells model based synthesis)
Fix Cell (defining floor plan , placement and power plan)
Fix Clock (clock tree synthesis)
Fix Wire (routing)

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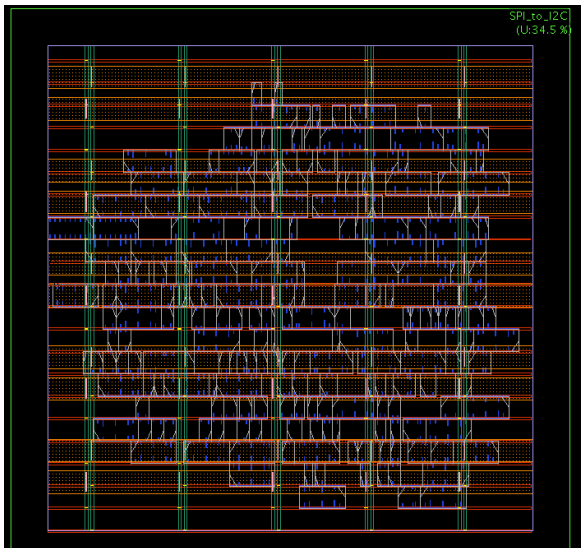

Figure 2: Physical design view of SPI to I2C converter with power grid and routing

IV RESULTS OF POWER CALCULATION

Power during Synthesis

Power during Synthesis	Without Clock Gating	With Clock Gating
Leakage power	1.5865e-02 uw	1.5806e-02 uw
Internal power	7.0024e-03 mw	6.3706e-03 mw
Switching power	6.6670e-04 mw	6.784e-04 mw
Total power	7.6850e-03 mw	7.0649e- 03 mw

Power after Physical design (calculated in Red hawk):

Power after physical design	Without Clock Gating	With Clock Gating
Leakage	3.5186e-05	4.8547e-05
power	watt	watt
Internal power	1.4442e-05 watt	1.1625e-05 watt
Switching power	1.7349e-06 watt	1.7999e-06 watt
Total power	5.1362e-05 watt	4.8547e-05 watt

Power with Dynamic Power gating:

Power with Dynamic Power gating:	Switch cell ON	Switch cell OFF
Leakage power	3.5122e-05 watt	1.7485e-05 watt
Internal power	1.1592e-05 watt	0
Switching power	1.7713e-06	0
Total power	4.8486e-05 watt	1.7485e-05 watt

V CONCLUSION AND FUTURE SCOPE

Unarguably the power is going to be the key differentiator and driver for the deep-submicron products in the future. There are a plethora of power management techniques available to be used. However the most effective power management approach seams to be targeting the architecture itself and make the device low power by design. This work hits the core of low power design which is architecture novelty for low power design. Both the dynamic as well as leakage power saving is achieved in this work. In terms of designing the protocol converter, there is scope for the improvement. For example here the internal clock at the top level which originally has to be generated internally inside the I2C master through state machine is considered. Also the rate at which I2C clock i.e. scl to toggle should be decided by the SPI clock so that there should not be any data

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loss. As each protocol has different data format, clock has to be synchronized between them so that no data loss happens.

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