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Novel power –up sequence control for MTCMOS designs

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Abstract: Power gating is effective for reducing standby leakage power as multi-threshold CMOS (MTCMOS) designs have become popular in the industry. However, a large inrush current and dynamic IR drop may occur when a circuit domain is powered up with MTCMOS switches. This could in turn lead to improper circuit operation. We propose a novel framework for generating a proper power-up sequence of the switches to control the inrush current of a power-gated domain while minimizing the power-up time and reducing the dynamic IR drop of the active domains. We also propose a configurable domino-delay circuit for implementing the sequence. Experimental results based on state-of-the-art industrial designs demonstrate the effectiveness of the proposed framework in limiting the inrush current, minimizing the power-up time, and reducing the dynamic IR drop. Results further confirm the efficiency of the framework in handling large-scale designs with more than 40 K power switches and 50 M transistors.

Keywords: multi threshold, CMOS, leakage power, VLSI

I. INTRODUCTION

CMOS circuits are used in many applications from gate arrays to control logic. They have the advantage over NMOS circuits in that they do not require active pull-up loads. For a CMOS inverter stage only one of the transistors conduct at a time. In the low output state the pull-down transistor conducts and the pull-up transistor is off. When the output is high the pull-up transistor conducts and the pull-down transistor is off. Pure CMOS circuits conduct very little current and, at low digital frequencies, consume small amounts of power. Most of the power dissipation is due to a changing logic state because both the pull-up and pull down transistors are conducting. Thus, CMOS circuits dissipate an increasing power for increasing digital signal frequency. The performance of CMOS circuits is not as dependent on the length to width ratio as only the pull-up or pull-down transistors conduct at a time. As was seen in the previous chapter the unit resistance of n-diffusion is approximately 10 kW per square for 5 mm technology and 20 kW per square for 0.90 µm technology. The p-type diffusion has a higher unit resistance and is approximately 25 kW per square (for 5 mm) and 40 kW per square (for 1.2 µm). Thus for an inverter, using 5 mm technology, with transistor ratios of 1:1 (2l´2l) the pull-up PMOS transistor will have a resistance of 25 kW and the pull-down resistance will be 10 kW. These resistances can be used to determine the maximum drive current in the low and high state, and also the power dissipation. that the N-channel, Enhancement-mode MOSFET (e-MOSFET) operates using a positive input voltage and has an extremely high input resistance (almost infinite) making it possible to interface with nearly any logic gate or driver capable of producing a positive output. Also, due to this very high input (Gate) resistance we can parallel together many different MOSFETs until we achieve the current handling limit required. While connecting together various MOSFETs in parallel may enable us to switch high currents or high voltage loads, doing so becomes expensive and impractical in both components and circuit board space. To overcome this problem Power Field Effect Transistors or Power FET's where developed.

We now know that there are two main differences between field effect transistors, depletion-mode only for JFET's and both enhancement-mode and depletion-mode for MOSFETs. In this tutorial we will look at using the Enhancement-mode MOSFET as a Switch as these transistors require a positive gate voltage to turn "ON" and a zero voltage to turn "OFF" making them easily understood as switches and also easy to interface with logic gates.The operation of the Enhancement-mode MOSFET, or e-MOSFET, can best be described using its I-V characteristics curves shown below. When the input voltage, (VIN) to the gate of the transistor is zero, the MOSFET conducts virtually no current and the output voltage (VOUT) is equal to the supply voltage VDD. So the MOSFET is "fully-OFF" and in its "cut-off" region.

II. LITERATURE SURVEY

Energy efficiency is important to battery-powered portable devices such as smart phones, GPS, PDAs, and tablets. However, the leakage current of these devices has increased significantly with the shrinking of semiconductor process technologies. The most straightforward and effective method for reducing standby leakage is power-gating, which cuts off the power supply (or ground) to a power- gated domain hen it is in an idle state and resumes the power supply when it is in an active state.

The multi-threshold CMOS (MTCMOS) technique [1] employs high-Vt transistors to implement always-on circuits, such as power switches, retention flip-flops, and always-on buffers, to minimize their leakage power

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consumption. The power up/down of a gated domain is controlled by turning the header (or footer) power switches on or off. These switches are parallel-connected between the mesh of the chip's true VDD (or ground) and the mesh of the gated domain's virtual VDD (or virtual ground). This power-switch fabric, also called a distributed sleep transistor network (DSTN [2]), along withits control scheme significantly affect the characteristics of the MTCMOS design [1]–[13], [19]–[22], and thus need to be carefully designed.

The number and size of the transistors used in the power switch fabric determine the voltage drop between the true VDD and the virtual VDD [5]–[7]. This voltage drop degrades circuit performance, and must be kept below a user-specified value. Using a larger number of power switches can achieve a smaller voltage drop at the expense of more area overhead. After the power switches are allocated, the sequence that turns on the power switches for a domain (called the power-up sequence) determines the voltage ramp-up time and the inrush current of the domain. The ramp-up time is the time during which the virtual VDD rises from ground level to the required operating level for active mode. The inrush current is the maximum transient current flowing through the power switches during the sleep-to-active mode transition.

There is generally a tradeoff between the ramp-up time and the inrush current [8]–[12]. A short ramp-up time may incur a large inrush current. It is necessary to constrain the inrush current of a domain, as an excessive inrush current may lead to excessive IR drop in other active domains resulting in chip malfunction. For example, an on-chip low drop out (LDO) voltage regulator may fail to boot up due to its being incapable of handling an excessive current surge. This can in turn damage certain power-sensitive IPs, such as a USB.

III. SUB THRESHOLD LEAKAGE CONTROL AND GATE PARTITIONING

A more effective method of dealing with sub threshold leakage currents is to employ dual Vt technology, where the process has both high and low threshold voltage devices. By having two different flavors of devices, one can utilize specialized circuit topologies to take advantage of the speed benefits of low Vt as well as the leakage reduction benefits of high Vt devices. For example, in a technology with a sub threshold slope of 100mV/ Decade, a 300mV change in Vt will produce 3 orders of magnitude reduction in sub threshold leakage currents. As a result, dual Vt techniques can be very effective as one continues to scale threshold voltages since multiple flavors of transistors are available. On the other hand, source biasing techniques are much less effective than dual Vt techniques inherently, and will also become less effective with future scaling because the intrinsic leakage will continue to worsen, body effect will be less effective with increased short channel effects, and the biasing ranges will be reduced at low supply voltages. Dual Vt techniques on the other hand will provide inherently fast and non-leaky devices that can be engineered through the process to provide the desired performance characteristics.

Dual Vt technology is becoming increasingly attractive in modern advanced CMOS technologies because the cost of an additional threshold voltage is relatively inexpensive for a process technology, requiring only an extra implant step. Yet the added flexibility of multiple threshold voltages for circuit designers is very valuable and can be used effectively to help provide high performance circuit operation while reducing sub threshold leakage currents during both active and standby circuit operation.

Dual Vt Gate Partitioning:

One of the most straightforward applications of dual Vt technology is simply to partition a circuit into critical and non critical regions, and to only use fast low Vt devices when necessary to meet performance goals. This approach will reduce sub threshold leakage currents both in the active and standby modes since low Vt devices are only sparingly used[16]. In general, high performance device operation and low sub threshold leakage currents are mutually exclusive properties because each tends to push threshold voltage in opposite directions. For example, during the active mode, if circuits need to be fast then inherently they will be more leaky as well. As a result, it makes sense to only use fast low Vt devices where necessary in order to maintain high performance operation, and slow high Vt devices in peripheral or I/O circuitry, for example, that is not speed critical. However, in aggressive high performance low power circuit topologies that have many balanced critical paths, many of the gates cannot be slowed down, and there is only limited leakage reduction that can be achieved. One dual Vt partitioning scheme that can be applied to random combinational logic can be to first implement the logic with all low Vt devices (to ensure fastest performance), and to selectively implant non critical gates to be high Vt. However, the difficulty is that non critical gates which were made high Vt can then become critical gate.

IV. TECHNOLOGY OF MTCMOS

The basic MTCMOS structure , where a low Vt computation block is gated with high Vt power switches. When the high Vt transistors are turned on, the low Vt logic gates are connected to virtual ground and power, and switching is performed through fast devices. However, by introducing an extra series device to the power supplies, MTCMOS circuits will incur a performance penalty compared to CMOS circuits, which worsens if the devices are not sized large enough. When the circuit enters the sleep mode, the high Vt gating transistors are turned off, resulting in a very low subthreshold leakage current from VCC to ground. MTCMOS is only effective at reducing standby leakage currents and therefore is most effective in burst mode type application, where reducing standby power is a major benefit.

Although both PMOS and NMOS gating transistors , only one polarity sleep device is actually required to reduce

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leakage if the logic block is purely combinational. NMOS sleep transistors typically are more effective because they have lower on resistances than a corresponding PMOS device, and subsequently can be made smaller for the same current drive. One possible advantage of using high Vt PMOS sleep devices though is that the body terminals can be tied to virtual VCC instead of the actual power supply, which may simplify the logic structures because libraries PMOS cells may not need to be modified. In any case, Figure 2-2 shows a simplified MTCMOS block that can be implemented with only an NMOS sleep device if the low Vt logic block is purely combinational.

It is important for the sleep transistor to have a high enough conductance during the active mode because the series resistance acts to degrade performance. One simple way to improve the conductance of the sleep device in the active mode is to overdrive the gate voltage (i.e. above VCC for the NMOS device), and similarly the leakage reduction can be improved by under-driving the gate (i.e. below ground for the NMOS device) during the standby mode. Cutting off leakage currents by under driving the gate is actually more useful for low Vt sleep devices, although reliability issues may become a concern. Even without under-driving though, MTCMOS circuits can achieve several orders of magnitude reduction in leakage currents, which results from two effects.

First, the total effective leakage width of the original CMOS circuit is reduced to the width of a single off high Vt NMOS transistor (provided it is smaller than the original pull down width), and second the increased threshold voltage results in an exponential reduction in leakage currents. To first order, the leakage behavior of the sleep device is characterized entirely by the threshold voltage of the NMOS sleep transistor (neglecting the drain voltage impact on leakage).

A small reduction can be further achieved if the internal logic gates are configured such that all the NMOS core devices are off during the standby state (thereby creating a source biasing scenario), but the savings are negligible compared to the leakage reduction already achievable with a high Vt NMOS device.

MTCMOS circuits are thus very effective at solving the sub threshold leakage problem during standby modes in future technologies. The sleep state mode operation is very straightforward, simply involving turning off the power switches, and will produce guaranteed leakage reduction of several orders of magnitude. On the other hand, the active mode circuit operation behaves theoretically just like an ordinary CMOS implementation, so existing architectures and designs can easily be ported to an MTCMOS implementation. One serious drawback to the widespread use of MTCMOS techniques though is that appropriate sleep transistor sizing becomes difficult for large circuit blocks[26]. Another problem (to be addressed in a later chapter) is that sequential circuits will lose data when the power transistors are turned off

V. DESIGN CHALLENGES

A specialized case of dual Vt technology that is more effective at reducing leakage currents in the standby mode is MTCMOS (Multi-Threshold CMOS) first described in [18]. This technique involves using high Vt transistors to gate the power supplies of a low Vt logic block, and is described in more detail in the next chapter. MTCMOS gates are especially effective at reducing standby leakage currents because the leakage currents can be shut off with high Vt gates during the standby state, yet during the active state the internal logic can operate at high speeds through low Vt devices.

Body Biasing Techniques

A final technique of controlling sub threshold leakage currents is to adjust device body biases (in a triple technology for example) to tune device threshold voltages directly. Unlike dual Vt approaches, where explicit high Vt and low Vt devices are used to provide low leakage and high performance devices, body biasing techniques use the body terminal LVt (Critical LVt HVt Initially all LVt Path) Some non critical path gates become HVt bias values as another control knob to tune threshold voltages dynamically. For example, application of maximum reverse bias, subject to device reliability and on chip voltage generation limits, can increase device threshold by several hundred mV, resulting in exponential reductions in leakage currents. A variant of the body biasing technique, where the source terminals rather than the body terminals are biased was shown in[23]. Body biasing techniques, including dynamic tuning applications, are explored in more detail in later chapters.

This work is geared towards exploring novel circuit techniques to provide sub threshold leakage control by exploiting the use of dual threshold voltages and body biasing. These basic principles for limiting sub threshold leakage currents have been explored previously in the literature, but circuit solutions have not been complete or robust enough to be applied to real VLSI systems. This thesis attempts to explore the main difficulties with existing solutions, and also explores new circuit structures and architectures that are very effective at limiting sub threshold leakage currents in both active and standby modes. The more detail MTCMOS techniques for reducing leakage currents during the standby state. Of particular difficulty with this technology is properly sizing the high Vt sleep devices to ensure that performance is maintained for all input vectors. These transistor sizing issues are explored in detail in this thesis, and a novel hierarchical sleep transistor sizing methodology was developed to ensure that MTCMOS will be fully functional even in a large system. the other hand explores a new type of dual Vt approach that was developed, imbedded dual Vt, which eliminates the need for using series high Vt power switches associated with MTCMOS. A special case of the imbedded dual Vt principle was applied to domino circuits, which illustrates how sub threshold leakage currents can be drastically reduced during standby states without effecting overall

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performance. then explores several novel sequential circuits that can retain state during low leakage standby modes, while still providing high speed active operation. In the literature, several sequential circuit approaches have been proposed, but many of these had poor performance or added too much control overhead to be useful. This thesis takes a more fundamental approach at addressing sequential circuit architectures, and begins with an in depth analysis of potential sneak leakage paths that can arise in sequential circuits (this analysis has been missing, and sometime incorrect in prior art). By fully understanding these limitations involved with sequential circuit design, new latch and flip flop architectures have been developed that have better performance and are more efficient than existing approaches.

Furthermore, a novel MTCMOS leakage feedback gate structure is also introduced, which provides a variant on MTCMOS circuit techniques where gates no longer have to float during standby states. This novel circuit idea has many important applications including improved flip flop structures and CMOS-MTCMOS.

VI. RESULTS

The results pertaining to the above study are presented in this section. The figures

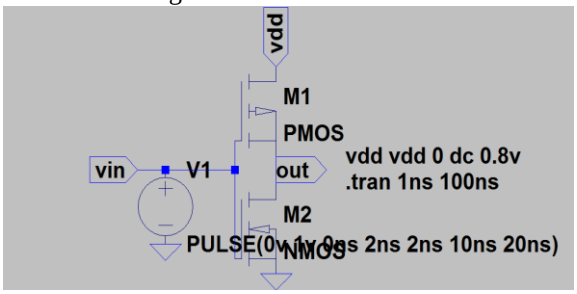

Fig.1 Simulated model of the proposed structure

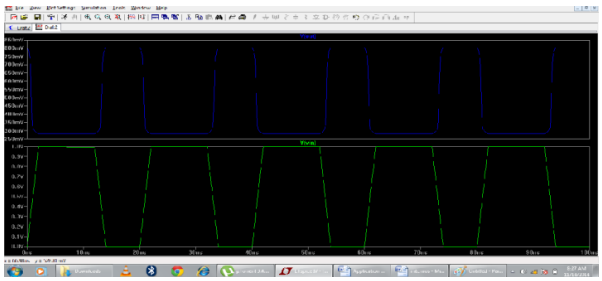

Fig.2: Input and output waveforms

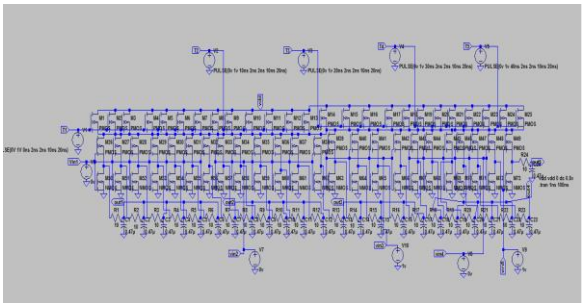

Fig.3: Layout description

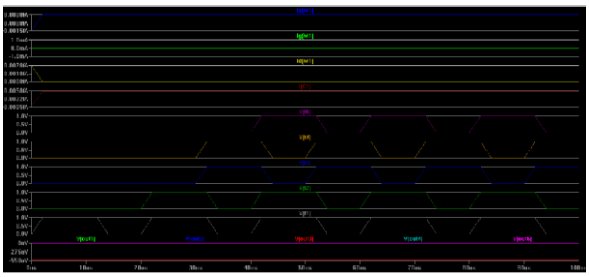

Fig.4: response of the proposed system

We evaluate the proposed approach based on an industrial smart-phone design utilizing an in-house chip implementation flow [13], [14]. The power switches are the mother-daughter switches (HDRDID2BWPHVT) from a TSMC 40 nm MTCMOS cell library [17].

VII. CONCLUSION

We have presented a power-up sequence generation method to address the problem of minimizing ramp-up time under peak inrush current constraint for MTCMOS designs. The proposed framework includes a current budget algorithm based on an effective model, an analytical routing guidance and a configurable domino-delay controller. Experimental results demonstrate the effectiveness of the proposed framework in minimizing the ramp-up time while mitigating the dynamic IR effect on the active domains under a specified peak current limit. We have not incorporated the effects of package model in this work.

One necessary step in our future work is to explore an analytical model considering package RLC parasitic. For package selection and cost reduction, it is possible to extend our work toanalyze the impact of decoupling capacitance on ramp-up time, inrush current and dynamic IR drop. Considering the inductance imposed by the package would result in a different inrush current estimation. We would like to address this point in our future work.

However, we can still consider our proposed framework as a conservative method to limit the inrush current since the package inductance will slow down the voltage ramp up and hence the actual inrush current will be smaller than our estimation. So the power-up sequence generated by our proposed method can still satisfy the inrush current constraint.

In nano-meter technology, device variations can alter the inrush current very much in each process-voltage-temperature corner. If we consider all the variations, the resulting power-up sequence may be either overestimated or underestimated. Our present version can only adjust the time interval and the reference clock post-silicon. Thus, some on-chip hardware performance monitors with an adaptive voltage or body-bias controller should be taken into account for variation control.

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