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Survey on Performance of CMOS Sensors

T.Jaya Bharathi[1], N.Mathan[2]

M.Tech VLSI Design, Sathyabama University, Chennai[1]

Assistant Professor, Department of ECE, Sathyabama University, Chennai[2]

Abstract: This paper presents a survey on CMOS Image Sensors (CIS) based on active Pixel Sensors (APS). Due to its properties, the APS is used in low voltage, low power and its applications in portable imaging systems such as disposable cameras and on-chip autonomous security cameras are random access, faster readout and low noise with peripheral circuitry.

Keywords: CMOS Image Sensors(CIS),Active Pixel Sensors(APS),Digital Pixel Sensors(DPS),pulse Width Modulation(PWM).

I. INTRODUCTION

The CMOS active pixel sensor (APS) is a second generation solid state sensor technology that was developed at Jet Propulsion Laboratory (JPL). The wide use of CMOS Active Pixel Sensors began during the year 1993.The goal of the advanced imager technology effort at JPL has been the development of a "camera on a chip," which would have a full digital interface. To achieve smaller and simpler electronics sensors will require the imaging instruments be highly integrated. By using CMOS APS technology low power, low volume, highly integrated imaging systems can now be realized. A complete imaging system could require an optics group, a power supply, a CMOS APS imaging array with on-chip analog-to-digital converter (ADC) and a microprocessor to upload the instructions to the imager and download the image data In this mechanism, the pixels were designed in a 2D structure, with access enable wire shared by pixels in the same row, and output wire shared by column.

Rochass et al proposed that each pixel did not have an amplifier, so an amplifier was connected at the end of each column. High power consumption, greater noise andslow output were some of its disadvantages. In 1969, the active pixel sensor was first introduced by adding independent amplifiers for each pixel. Thus in 1970, the Charge Coupled Device was invented. Thus they were very useful in the working of cameras. During the early 1990′s the CMOS process was well developed and was considered to be the base for all types of logic devices as well as microprocessors. This further led to the invention of CMOS APS.

A. Dickinson et al proposed that pixel array has on–chip timing, control, correlated double sampling and fixed pattern noise (FPN) suppression circuitry. It has three transistors in each pixel with a typical pixel pitch of 15x minimum size of the technology . The photodiode APS has higher QE than the photogate pixels, because there is no overlying polysilicon which is required for photogate. The output photodiode signal is supposedly independent of detector size because a decrease in detector size is compensated by an increase in conversion gain with less pixel capacitance. However, peripheral capacitances from the perimeters of the detector increase the total capacitance of the sensing node and thus, decrease the conversion gain.

II. PASSIVE PIXEL SENSORS:

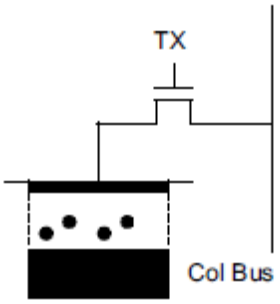

Fig:1 Passive pixel sensors(PPS)

C.G. Sodini I.L. Fujimori et al(2000) proposed that the PPS consists of a photodiode and a select transistor. A charge integration amplifier (CIA) readout circuit is located at the bottom of the column bus to keep the voltage on the column bus constant. With a given pixel size, it has the highest design fill factor because it has only one transistor for the readout. QE (quantum efficiency) can be quite high due to the large fill factor and absence of an overlying layer of polysilicon as found in CCDs.

Fig.1 shows that the passive pixel structure has the major problems of their readout speed and noise level due to large capacitive load. Since the large bus is directly connected to each pixel while it is read out,RC time constant is very high and therefore, the readout speed is slow. In addition, due to the large capacitive load, a passive pixel's readout noise is typically high, with the order of 250 electrons rms, compared to commercial CCDs with less than 10 electrons rms of read noise. Therefore, the passive pixel does not scale well to larger array sizes or faster pixel
readout rates.

A. Advantages of PPS:

- Maximized fill factor
- Smaller pixel size as technology scales
- 1 transistors,2lines
- High yield due to its simplicity
- High QE due to few overlaying devices
- Slow readout and high noise due to high bus capacitance.

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III. ACTIVE PIXEL SENSORS:

When the passive pixel sensor was introduced by Weckler in 1967, the problems of the passive pixel were quickly realized and a sensor with an active amplifier within each pixel, called an active pixel sensor, was proposed as shown in the Fig:2.

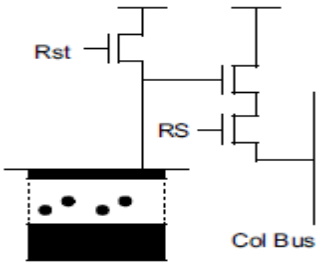

Fig:2 Active pixel sensors(APS)

A. Dickinson, B. Ackland et al(2002)proposed that pixel array has on–chip timing, control, correlated double sampling and fixed pattern noise (FPN) suppression circuitry. It has three transistors in each pixel with a typical pixel pitch of 15x minimum size of the technology . The photodiode APS has higher QE than the photogate pixels,because there is no overlying polysilicon which is required for photo gate. The output photodiode signal is supposedly independent ofdetector size because a decrease in detector size is compensated by an increase in conversion gain with less pixel capacitance. However, peripheral capacitances from the perimeters of the detector increase the total capacitance of the sensing node and thus, decrease the conversion gain.

Despite of the reduction of the capacitance in the pixels, read noise is limited by the reset noise on the photodiode since correlated double sampling is not truly correlated without frame memory. As the pixel size scales down, photosensitivity decreases and the reset noise scales as C1/2, where C is the photodiode capacitance. Therefore, the tradeoff can be made in designing pixel fill factor (photodiode area), dynamic range, Signal-to-Noise Ratio (SNR) and conversion gain (μV/e-).

Applications of APS:

- Pixel consists of floating reversed biased pn-junction
- 3 transistors,4 lines pixel
- Sense node and integration node are same
- Moderately high quantum efficiency

IV. PHOTOGATE ACTIVE PIXEL SENSORS

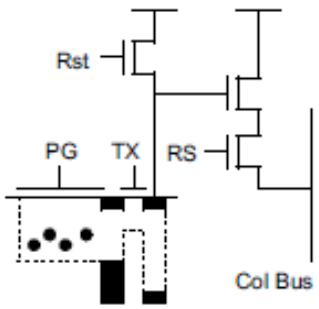

Fig: 3 Photogate active pixel sensors

Fig.3 shows the basic idea of photogate pixel comes from CCD.**Andrew J. Blanksby and Marc J. Loinaz (1995)**proposed while photon generatedcharge is integrated under a photogate with high potential well, the output floatingnode is reset and the corresponding voltage is read out to one of S/H in CDS. When theintegration is done, the charge is transferred to the output floating node by pulsing signal onthe photogate. Then the corresponding voltage from the integrated charge is read by the source follower to the second S/H of the CDS. The CDS outputs the difference between the reset voltage level and the photo-voltage level. The correlated double sampling can suppress reset noise, 1/f noise, and FPN due to Vt and lithographic variations in the array. Therefore, the main noise of the photogate is photon shot noise that cannot be suppressed by any means.

The photogate has a pixel pitch typically equal to 20x the minimum size of the technology due to five transistors in each pixel. The floating diffusion capacitance is typically made with a small capacitance of the order of 10 fF yielding a conversion gain of 10-20 μV/e- and 2e reset noise. However, due to the overlaying polysilicon, there is a reduction in quantum efficiency, particularly in the blue. However, the reduction of noise level increases the total dynamic range and SNR.

Application on photogate active pixel sensors

- Pixel consists of a MOS capacitor coupled to a floating reverse biased p-n junction
- 5 trnsistors,6 lines per pixel
- Sense node and integration node are separate
- Low noise,low QE

V. PINNED PHOTODIODE APS

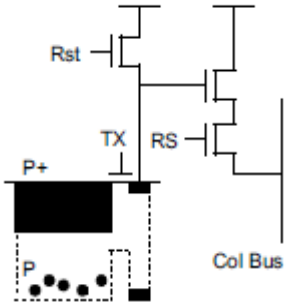

Fig.4 Pinned Photodiode APS

R. M. Gruidash, T. H. Lee et al (1997) proposed that the pixel consists of pinned diode (p+-n-p), where photon collection area is dragged away from the surface in order to reduce surface defect noise such as dark current. Photon-generated charge is integrated under a pinned diode and transferred to the output floating diffusion for the readout. Fig.4 shows that similar to the photogate, sense node and integration node are separated so as to optimize the noise. However, the main difference from the photogate is that the potential well for the charge collection is generated by buried intrinsic layer (or n type layer) instead of pulsed gate voltage in the photogate.

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Each pixel has four transistors and five control lines, resulting in fill factor, which is higher than photogate, but lower than photodiode. In addition, due to a small photon collection area of pinned diode, it has a very small full well for photon-generated charge collection with lower QE, compared to the photodiode.

Application of pinned photodiode aps

- Pixel consists of pinned diode(p+-n-p)
- 4 transistors,5 lines per pixel
- Sense node and integration node are separate
- Low noise,QE lower than that of PD

VI. DIGITAL PIXEL SENSORS

Stuart Kleinfelder, SukHwan et al(2002)analysed that the impact of CMOS technology scaling on analog integrated circuits has become increasingly significant in recent years, so it is difficult to maintain the advantages of high performance in CMOS active pixel sensors (APS). However, it is possible to design low-noise CMOS digital pixel sensors (DPS) with technology scaling. There are obvious advantages for DPS. Using pixel-level ADC in DPS not only reduces the required design in analog circuits, but also improves its system performance, particularly in terms of noise.

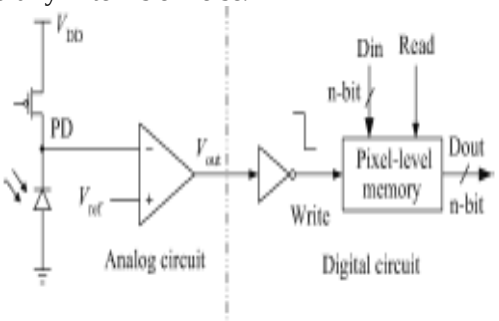

Fig.5 Digital pixel sensors

Fig.5 shows that in addition to pixel-level A/D conversion in voltage mode, present researches mainly focus on DPS based on pulse width modulation (PWM) in time domain. In PWM DPS, the photocurrent information could be converted into time measurement and the data also could be compressed and stored in pixel level.

VII. DPS WITH SELF RESETING ASYNCHRONOUS SCHEME.

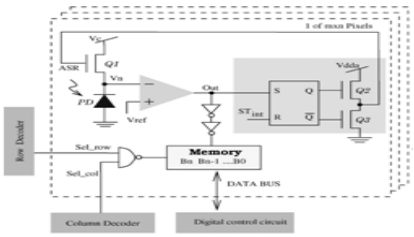

Fig.6 DPS with self resetting asynchronous scheme

Fig. 6 shows the architecture of the self-resetting asynchronous DPS and its timing diagram, respectively. The architecture is similar in configuration to a single slope ADC, and also to the DPS array. **Zhang Chi ,Yao Suying et al (2011)** proposed that DPS array differs significantly from the other two architectures in its mode of operation. The image acquisition starts by sending a global start integration signal ST , to the array and to the control circuit. The control circuit generates timing data, which is distributed in parallel to all the pixels of the array. Upon receiving the start integration signal, each pixel operates asynchronously, where the output voltage of the photodiode is compared to a fixed reference voltage. When the two voltages become equal, the comparator switches, and the data value, which records the switching time, is stored in the pixel memory. The integration time is therefore not dictated by a global timing circuit but is set by each pixel independently. Due to the asynchronous nature of the pixel operation, it is necessary to distribute the timing data as Gray code, to eliminate any errors that may have been caused by the pixel comparator switching during data transition.

VIII. CONCLUSION

Noise severely constraints the accuracy of the time measurement and the quality of the image. In contrast to noise analysis in CMOS APS, the noise characteristic of DPS based on a PWM scheme has been surveyed in this paper. The comparative study of PPS ,APS and DPS are made and its parameters like noise,power and quantum efficiency (QE) are surveyed.

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