ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 3, March 2015

Minimization of the Complexity of the digital Circuit using Genetic Algorithm

Amit Pandey[1], Sudha Nair[2]

Research Scholar, Electronics & Communication, RKDF IST, Bhopal, India[1]

Professor, Electronics & Communication, RKDF IST, Bhopal, India[2]

Abstract: Digital Equipments are the necessity in the current scenario. Rapid growth of digital world has taken the researchers interest in order to improve the performance of circuit. The Optimization of the digital circuit is done on the basis of Genetic Algorithm (GA) for achieving maximum output of the digital circuit in terms of speed. This algorithm can dynamically perform various tests on the desired hardware testability. The comparative analysis is done on the speed of the digital circuit using the genetic algorithm and sequential search algorithm & was found that GA is more efficient & faster in propagation delay.

Keywords: Combinational Circuit, Sequential Circuit, Genetic Approach

I. INTRODUCTION

Interconnection of sure specific elements like resistors, diodes, capacitors, transistors etc. to create a gate, flip flop or the other building block is termed Circuit style [1]. The moment growth of electronic equipments makes the condition to cut back the complexness. The aim is in a position to satisfy by the genetic rule. Genetic rule is one amongst the simplest ways that to resolve a tangle that very little is thought [2]. Genetic algorithms use the principles of choice and evolution to supply many solutions to a given drawback.

There is a unit many sorts of application that used genetic rule to resolve the matter. In Digital circuits there's an opportunity to seek out the most output of a digital circuit supported flip flop and might minimize time as compare to alternative search algorithms there circuits also are referred to as the logic circuits as a result of a man of science [1].

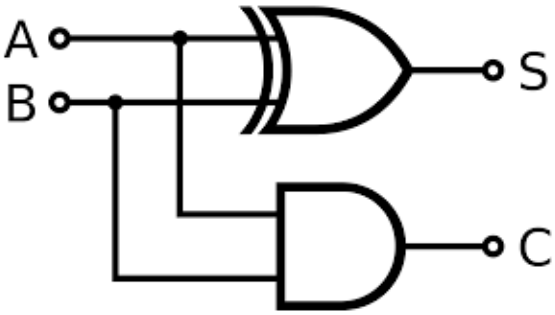

Figure 1.1 Digital Circuits with Gates

Figure 1.1 is a simple architecture for the digital circuit having two Gates. Each has its own property according to logic theory.

In this paper, Optimization of the digital circuit is done on the basis of Genetic Algorithm (GA) for achieving maximum output of the digital circuit in terms of speed. These works have been using some digital circuits and evaluating the maximum output of the circuits using GA.

The results show that the time taken by proposed work is less than the previous work. There is a large difference between numbers of comparator. Finally the proposed work is better than the previous methods.

II. DIGITAL CIRCUIT

A digital circuit could be a circuit whereby the signal is one among two separate levels. every level is one among 2 completely different states taken .Digital circuits use transistors to form logic gates perform Boolean logic. This logic is predicated on digital natural philosophy and pc process. Digital circuit's area unit less sensitive to noise or deterioration of the standard of analog circuits. It's additionally easier to perform detection and error correction of digital signals. To change the method of planning digital circuits, engineers Electronic style Automation (EDA) tools, a kind of package that optimizes the logic in very digital circuit digital systems within the world these days; have an excellent influence on fashionable society. Many, industrial, commercial, scientific progress has been created attainable due to digital systems.

III. GENETIC ALGORITHM

Genetic Algorithm GAs is a methodology that inspired by the procedure of organic progression. Genetic Algorithm follow human evaluation and survival of fittest to generate an optimized solution and it has been used uniform approach to solve the problems [2, 3]. It contains two terms Population and individual, Individual behave like child. Population is permutation of parent's gens like father, grandfather, mother, grandmother etc.

- A genetic representation of solutions to the problem;
- A way to create an initial population of solutions;
- An evaluation function rating solutions in terms of their fitness;
- Genetic operators that alter the genetic composition of children during reproduction;

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 3, March 2015

- Values for the parameters of genetic algorithms.

Genetic algorithms tend to thrive in an environment in which there is a very large set of candidate solutions and in which the search space is uneven and has many hills and valleys. True, genetic algorithms will do well in any environment, but they will be greatly outclassed by more situation specific algorithms in the simpler search spaces. Therefore you must keep in mind that genetic algorithms are not always the best choice. Sometimes they can take quite a while to run and are therefore not always feasible for real time use. They are, however, one of the most powerful methods with which to (relatively) quickly create high quality solutions to a problem. Now, before we start, I'm going to provide you with some key terms so that this article makes sense.

IV. GENETIC ALGORITHM WITH DIGITAL CIRCUIT

Genetic algorithm can apply at many places in the world of digital circuits. It seems to be that the various authors has worked on genetic algorithm over digital circuit. The genetic algorithm has used in order to find Fault Diagnosis of Mixed-signal Circuits. Genetic algorithm can also apply to design of Combinational Digital Circuits. Genetic algorithm has used with hardware evaluation environment in order to improve the time and area constraints with the arithmetic operations. Some major applications are:

- Designing of Digital Circuit
- Optimization of Digital Circuit
- Fault Tolerance of Digital Circuit
- Test Generation of Digital Circuit
- Performance analysis of Digital circuit

V. RELATED WORK

There are many works has been done in this area. Some of work has presented here.

The author explained the genetic algorithm over hardware evaluation environment [5]. They provided results with a number of benchmark arithmetic circuits evolved under different performance driven timing and area constraints.

Genetic algorithm plays an important role to evolve the combinational circuit [6]. This algorithm uses the various techniques like liner chromosomes and dimensional crossover. In this paper the author proposed the two dimensional over two dimensional crossover and mutation techniques. By this approach the speed of GA has increased as compare to traditional approach. This whole work has done in MATLAB.

There are some limitations in conventional fault tolerance diagnosis of mixed-signal circuit algorithm [7]. In this paper the author applied the genetic algorithm in order to diagnosis the faults in mix-signal circuit. They use some characteristics and the optimal fitness function to simulate the work. The results show that this approach can help to reduce the complexity of digital amount and special processing.

Job Scheduling is a important task in the computer system. When it has to done in multiprocessor it will make more complex [8]. In this paper the author has used the genetic approach in order to perform job scheduling in multiprocessor environment. Here fitness function based on aggregation is used. Here Results of three methods has compared in unified condition simulation. The Genetic approach shows better results in experiments and can reduce finishing time and waiting time simultaneously.

The author has proposed [9] a local search based genetic algorithm (GALS) in order to solve the community mining problem. The author has tested the work on both computer-generated and real-world networks, and compared with some competitive community mining algorithms. Experimental results demonstrate that GALS is highly effective as well as efficient at discovering community structure.

Timetabling problems are a process of assigning a given set of events and resources to the limited space and time under hard constraints which are rigidly enforced and soft constraints which are satisfied as nearly as possible [10]. To solve such types of problem the author apply the genetic algorithm. It is demonstrated to be feasible for solving a real-world university course timetabling problem.

VI. PROPOSED METHODOLOGY

Genetic algorithms are inspired by Darwin's theory about evolution. Solution to a problem solved by genetic algorithms is evolved. Algorithm is started with a set of solutions (represented by chromosomes) called population. Solutions from one population are taken and used to form a new population. This is motivated by a hope, that the new population will be better than the old one. Solutions which are selected to form new solutions (offspring) are selected according to their fitness - the more suitable they are the more chances they have to reproduce.

Their performances are used here for finding maximum output of the digital circuit. Flow chart describes the techniques used for finding maximum output of the digital circuit using genetic algorithm. Mainly there are two techniques used for finding maximum output of the digital circuit using genetic algorithm.

1- Multipoint crossover technique.
2- Variable mutation methods.

VII. JONSON COUNTER

Counters have huge number of applications in Digital world. There are many types of counters; here there is a discussion about Johnson counter. Johnson counter is also known as twisted Ring counter or inverse feedbacks counter. It such circuit there is a 2N states where 'N' is the number of flip-flops. A Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first. The register cycles through a sequence of bit-patterns. The MOD of the Johnson counter is 2n if n flip-flops are used. The main advantage of the Johnson counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD.

DOI 10.17148/IJARCCE.2015.4393

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 3, March 2015

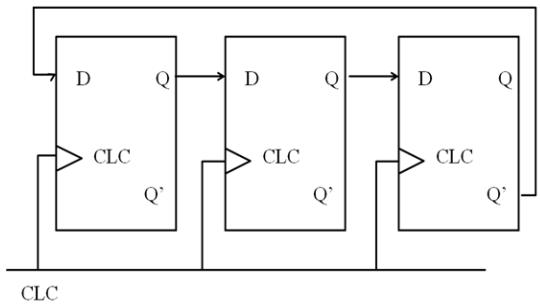

Figure 1.2 Jonson Counter (4 Bit)

D-flip flop

Basically, such type of flip flop is a modification of clocked RS flip flop gates from a basic Latch flip flop and NOR gates modify it in to a clock RS flip flop. The D input goes directly to S input and its complement through NOT gate is applied to the R input.

This kind of flip flop prevents the value of D from reaching the output until a clock pulse occurs. The action of circuit is straight forward as follows.

When the clock is low, both AND gates are disabled, therefore D can change values without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced equal to D when the clock again goes low, Q retains or stores the last value of D. Locks are often referred to as level-sensitive, because their output follows their inputs as long as they are activated.

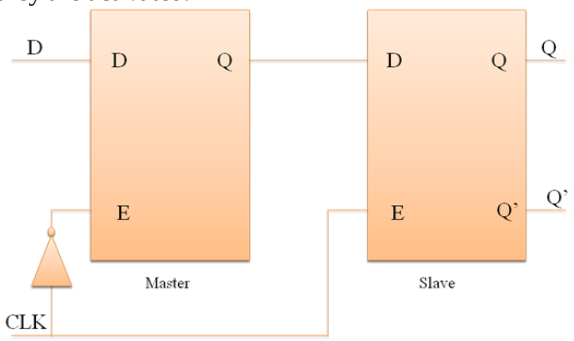

Figure 1.3 D Flip flop

ALGORITHM

According to the GA we use following steps for finding maximum output of the circuit:-

STEP 1: The first step describes about the different parameter of the digital circuit.

STEP 2: This step describes the execution of the digital circuit by providing the clock and stores its output.

STEP3: The output of step 2 undergoes the process of genetic algorithm. The output of step 2 is taken as the search space and initial population is selected from the search space.

STEP 4: This step describes the initialization of mutation rate = 0 and generation = 1.

STEP 5: This step describes the finding value of selected location.

STEP 6: This step describes the selection of two members from initial population which have highest value?

STEP 7: This step describes the iterative condition for the step6. If the condition is found true then mute rate is checked else crossover is done. In the crossover, generate new Childs from the combination of parent's member.

STEP 8: If mute rate found equal to maximum mute rate then process is terminated

And result is generated else the mute rate is increased by 1 and crossover is done.

STEP 9: This step describes the mutation in mutation technique where change in the Properties of the child which generated by the crossover technique.

STEP 10: After the execution of mutation new generation comes.

STEP 11: If generation is found to be equal to maximum defined generation then the

Process is terminated and result is generated else initialize with new Childs.

FLOW GRAPH OF WORK

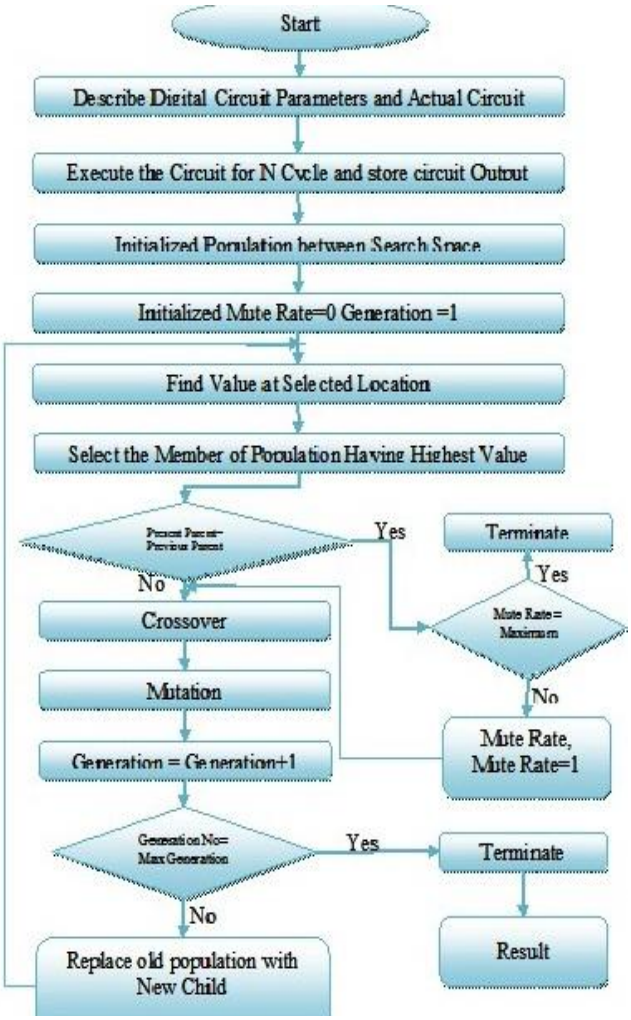

Figure 1.4 Flow Graph of Working Model

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 3, March 2015

VIII SIMULATIONS & SYNTHESIS RESULTS

Here shows the simulation and synthesis results of Digital Circuit in the RTL view of Digital Circuit shows there are two inputs clock and reset and there are two outputs best value and best address best value shows the maximum output of digital circuit and best address shows the address of memory where the maximum output of digital circuit stored

RTL VIEW OF CIRCUIT

RTL view describes there are two inputs clock and reset and there are two outputs best address and best value. In digital circuit design, register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals.

Register-transfer-level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level is typical practice in modern digital design.

IX SIMULATION RESULT

Simulation window shows the output results of hardware simulation which gives the best value of digital circuit and best address of memory in which best value is stored.

In this section we provide the snapshots of our work.

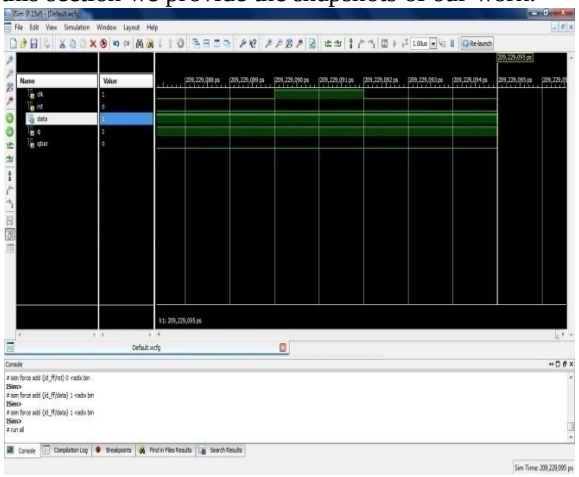

Figure 1.5 Simulation of D flips Flop

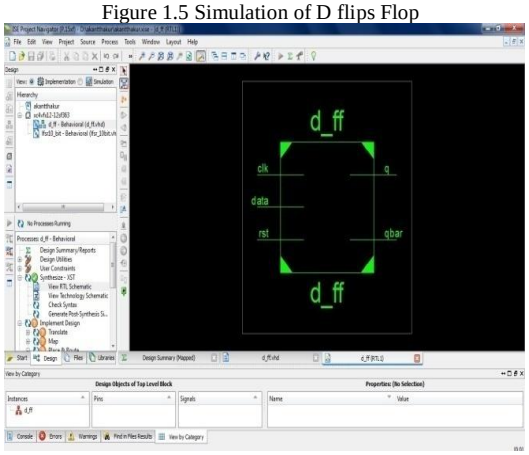

Figure 1.6 RTL view of D Flip Flop

Here the figure 5.2 shows the register transfer level view generated by VHDL for D flip-flop has been shown. The figure 5.3 shows the Technology Schematic of D flip-flop.

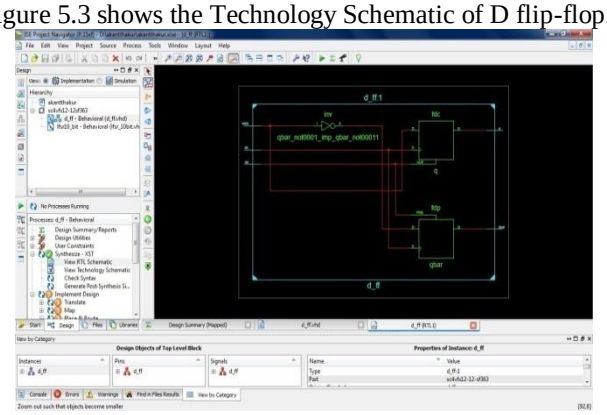

Figure 1.7 Technology Schematic view of D Flip Flop

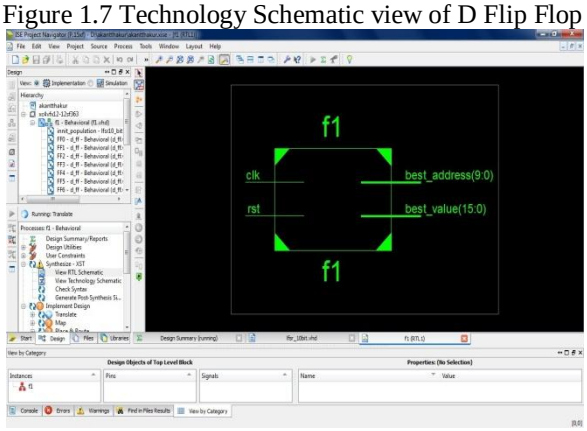

Figure 1.8 RTL for final Work

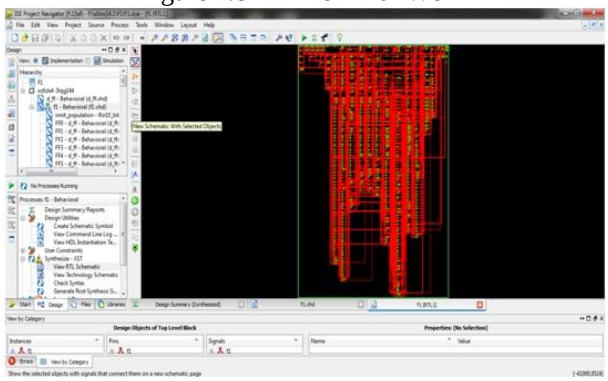

Figure 1.9 Final Technology Schematic

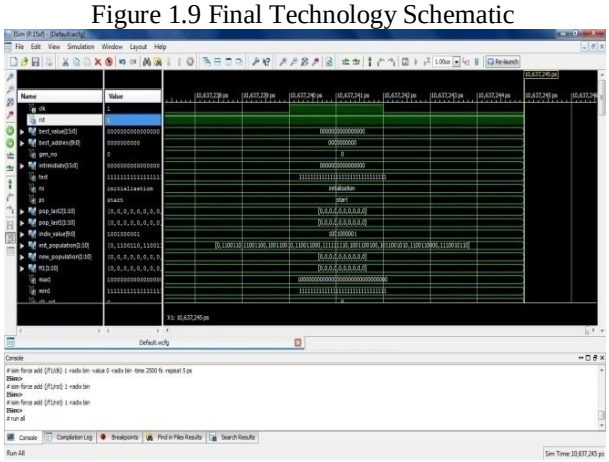

Figure 1.10 Final Simulation of Work

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 3, March 2015

Slice logic utilization	Used	Available	Utilization
Number of Slice Registers	809	4,800	16%
Number used as Flip Flops	808		
Number used as Latches	1		
Number used as Latch- thrus	0		
Number used as AND OR logics	0		
Number of slice LUTs	1,619	2,400	67%
Number used as logic	1,197	2,400	49%
Number using 06 output only	773		
Number using 05 output only	7		
Number using 05 and 06	417		
Number used as ROM	0		
Number used as Memory	413	1,200	34%

Table 1.2 Device utilization summery

COMPARISON TABLE

Maximum Output	Comparator Used in GA	Time Required in GA	Comparator Used in Sequential Search	Time Required in Sequential Search
1111111111111111	230	2.3µS	1023	10.23µS
1111111100011111	250	2.5µS	1023	10.23µS
1111111111100000	210	2.1µS	1023	10.23µS
1011111010110101	230	2.3µS	1023	10.23µS
1111111100000000	210	2.1µS	1023	10.23µS
1111001111000011	210	2.1µS	1023	10.23µS
1100111111110011	210	2.1µS	1023	10.23µS
1111101111110011	250	2.5µS	1023	10.23µS
0001110001111111	210	2.1µS	1023	10.23µS
1111111110000000	220	2.2µS	1023	10.23µS

Table 1.1 Comparison Table

The table 5.1 shows the comparative study of the proposed work with respect to sequential search. Here the number of comparator used for search and time has been shown. The result has been taken for the ten different maximum outputs.

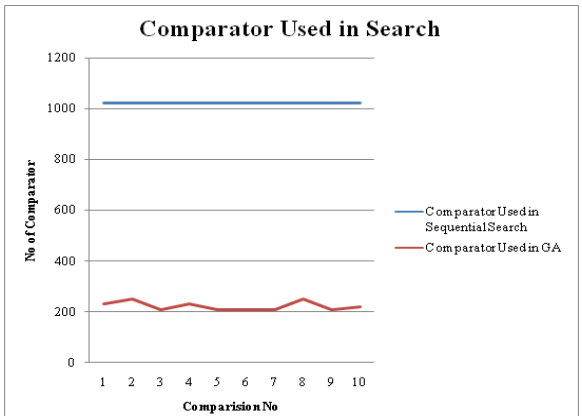

Figure 1.11 Comparison graph

The above graph shows the comparison between the comparator required in the both work. If we search anything the searching element must be compare with the element of the search area. Large number of comparison will not good for any algorithm. As we know the sequential search goes through the each element of the nodes with respect to data sequence and finds the searching element. In this case it seems to be that the there is a large difference between both approaches in required comparison

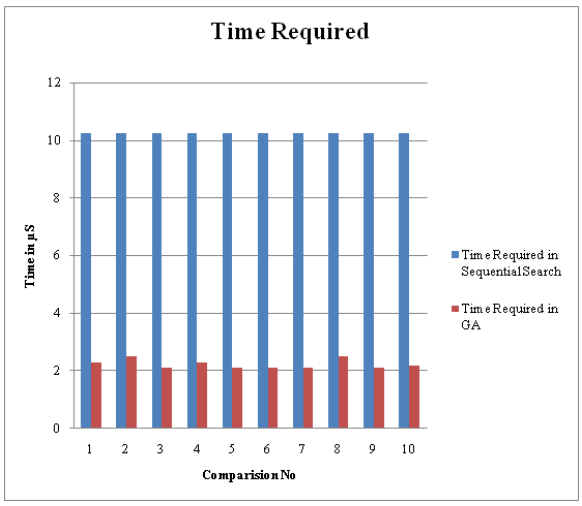

Figure 1.11 Comparison graph with time

We have already observed that the numbers of comparisons are going to be down in the proposed approach. So that the required time should be reduces. The above figure shows this comparative study which shows that the proposed methodology required the less time as compare to sequential search.

X. CONCLUSION

A Digital circuit has a huge number of outputs. Among all these outputs there is a need of selecting one of the best outputs. The proposed work shows that it is possible to find the maximum output of a digital circuit. The work has used genetic algorithm with the help of VHDL implementation.

DOI 10.17148/IJARCCE.2015.4393

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 3, March 2015

Genetic algorithm is one of the Artificial Intelligence approaches to simulate the idea of adaptation to the process of evolution and natural selection of nature through the development of computer work. Genetic algorithm is one used by a number of tools that artificial intelligence in problem such as optimization, planning, processing of data, clustering, trend analysis and path finding.

In this dissertation, Optimization of the digital circuit is done on the basis of Genetic Algorithm (GA) for achieving maximum output of the digital circuit in terms of speed. These works have been using some digital circuits and evaluating the maximum output of the circuits using GA.

The results show that the time taken by proposed work is less than the previous work. There is a large difference between numbers of comparator. Finally the proposed work is better than the previous methods.

FUTURE WORK

GA is the better choice for development in the different areas of communication, medical, mathematics, manufacturing and other fields.

In this work, we have used Roulette wheel and Elitism selection methods for selection. In future, we can use other selection methods like Rank selection, Tournament selection, and Steady state selection. In this work, the length of the population we have used is 10 chromosomes. In future, we can increase the length of the population to improve the performance. In this work, we have used multipoint crossover technique and variable mutation technique. In future we can use different crossover and mutation techniques to improve the performance.

ACKNOWLEDGEMENT

This paper would not have been possible without my guide **Prof. Sudha Nair**. I wish to express my thanks to all the people who helped turn the World-Wide Web into the useful and popular distributed hypertext. I also wish to express thanks the anonymous reviewers for their valuable suggestions.

REFERENCES

[1] "Digitalcircuit"http://users.senet.com.audwsmith/beginners.htm Accessed on 23/06/2013
[2] Goldberg D E., "Genetic Algorithms in Search, Optimization and Machine Learning", Reading: Addison-Wesley Publishing Company, 1989
[3] Coello Coello C A, Lamont G B, Van Veldhuizen D A. 2nd ed., "Evolutionary Algorithms for Solving Multi-Objective Problems", New York: Springer, 2007
[4] A. Rangel-Merino, J. L. López-Bonilla, R. Linares y Miranda, Optimization Method based on Genetic Algorithms, Apeiron, Vol. 12, No. 4, October 2005.
[5] Ben. I Hounsell and Tughrul Arslan "A Novel Genetic Algorithms for the Automated Design of Performance Driven Digital Circuits", IEEE 2000, pp 601-608.
[6] Vijayakumari. C.K and Mythili. P "A Faster 2D Technique for the design of Combinational Digital Circuits Using Genetic Algorithm" IEEE 2012.
[7] Shangcong Feng and Xiaofeng Wang,"Research on Fault Diagnosis of Mixed-signal Circuits Based on Genetic Algorithms", IEEE 2012, pp 12-15.
[8] Elnaz Zafarani Moattar, Amir Masoud Rahmanil and Mohammad Reza Feizi Derakhshi"Job Scheduling in Multi Processor Architecture Using Genetic Algorithm" IEEE 2008, pp 248-251.
[9] Di Jin, Dongxiao He, Dayou Liu and Carlos Baquero "Genetic Algorithm with Local Search for Community Mining in Complex Networks", IEEE 2010, pp 105-112.
[10] Xinyang Deng, Yajuan Zhang, Bingyi Kang, Jiyi Wu, Xiaohong Sun and Yong Deng"An Application of Genetic Algorithm for University Course Timetabling Problem" , IEEE 2011, pp 2119-2122.
[11] M. A. Abido and A. Elazouni, "Improved Crossover and Mutation Operators for Genetic- Algorithm Project Scheduling", IEEE 2009,pp- 1865-1872
[12] Elnaz Zafarani Moattarl, Amir Masoud Rahmanil, Mohammad Reza Feizi Derakhshi, "Job Scheduling in Multi Processor Architecture Using Genetic Algorithm", 2008 IEEE, pp -248-251.
[13] Masanao Aoshima and Akinori Kanasugi, "A Processor for Genetic Algorithm based on Redundant Binary Number", IEEE 2008, pp- 581-586.
[14] H.A. Rahim1, A.A. A. Rahman, R.B. Ahmad1, W. N. F. W. Ariffin1, M.I. Ahmad1, "The Performance Study of Two Genetic Algorithm Approaches for VLSI Macro-Cell Layout Area Optimization", IEEE 2008, pp- 207-212.
[15] Ernesto Mininno, Francesco Cupertino and David Naso, "Real-Valued Compact Genetic Algorithms for Embedded Microcontroller Optimization", IEEE 2008, VOL. 12, NO. 2, APRIL 2008 pp- 203-219
[16] Pei-Yin Chen, Ren-Der Chen, Yu-Pin Chang, Leang-San Shieh, "Hardware Implementation for a Genetic Algorithm", IEEE 2008, VOL. 57, NO. 4, APRIL 2008 pp- 699-705.
[17] Y. Deng, X. Y. Su, D. Wang and Q. Li, Target Recognition Based on Fuzzy Dempster Data Fusion Method, Defence Science Journal,vol. 60, 2010, pp 525-530.
[18] Y. Deng, W. Jiang and R. Sadiq, Modeling contaminant intrusion in water distribution networks: A new similarity-based DST method, Expert Systems with Applications, vol. 38, 2011, pp 571-578.
[19] Y. Deng and F. T. S. Chan, A new fuzzy dempster MCDM method and its application in supplier selection, Expert Systems with Applications, 2010, Article in Press.
[20] P. Avella, B. D'Auria, S. Salerno and I. Vasil'ev, A Computational Study of Local Search Algorithms for Italian High-school Timetabling. Journal of Heuristics, vol. 13, 2007, pp 543-556.
[21] . D. Causmaecker, P. Demeester and G.V. Berghe, A Decomposed Metaheuristic Approach for a Real-world University Timetabling Problem. European Journal of Operational Research, vol. 195, 2009, pp 307-318.
[22] Socha, M. Sampels and M. Manfrin, Ant Algorithms for The University Course Timetabling Problem with Regard to The State- of-the-art. Applications of Evolutionary Computing, vol. 2611, 2003, pp 334-345.
[23] R. Lewis and B. Paechter, Application of The Grouping Genetic Al- gorithm to University Course Timetabling. Evolutionary Computation in Combinatorial Optimization, Proceedings, vol. 3448, 2005, pp 144-153.
[24] P. Wilke, M. Grobner, N. Oster, A Hybrid Genetic Algorithm for School Timetabling. Advances in Artificial Intelligence, vol. 2557, 2002, pp 455-464.
[25] Yingjie Xing "An Improved Genetic Algorithm with Recurrent Search for The Job-shop Scheduling Problem" IEEE 2006 pp 3386-3390.

BIOGRAPHY

Amit Pandey has completed his graduation from Thakral Institute of Technology Bhopal in Electronics and Communication. Now Pursuing M.Tech Program from RKDF IST Bhopl M.P.