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Design and Analysis of Low Power High Performance 32-bit Ripple Carry Adder with Proposed Adder Cell

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Abstract: In this work one bit Full Adder with Ten transistors have been proposed. Reducing Power dissipation, supply voltage, leakage currents, area of chip are the most important parameters in today`s VLSI designs. The system reliability can be increased by reducing the cost, weight and physical size and it is achieved by decreasing the transistor count. Therefore the minimum power consumption target and lower area can be meet by reducing the hardware size. Digital circuits can be minimize in two methods. One is human method and another is Computational method. This paper propose one-bit Full Adder based on human method with ten transistors and simulation for the designed circuits were also performed with 4-bit, 16-bit and 32-bit ripple carry adder. Finally the simulation analysis were compared with conventional and proposed Adder in terms of total power consumption, delay, area and power delay product.

Keywords: CMOS; Conventional Full Adder; Low Power design; 4-bit RCA;16-bit RCA;32-bit RCA.

I. INTRODUCTION

Development of digital Integrated Circuits is challenged by high power consumption and greater threshold leakages. Scaling improves functionality and density of transistors on a chip. Scaling helps to increase operation speed and performance of IC designs. Today leakage power and current has became an important issue in digital system design. The system reliability can be increased by reducing the cost, weight and physical size and it is achieved by decreasing the transistor count. Therefore the minimum power consumption target and lower area can be meet by reducing the hardware size. Digital circuits can be minimize in two methods. One is human method and another is Computational method. Boolean algebra, Karnaugh Map and QuineMcclusky methods come under human method.

Low-power design techniques minimize active leakage power in nano scale CMOS VLSI systems. Developers of battery powered devices facing challenges to offer high levels of functionality, performance and simultaneously increasing life time of the battery. In some cases, battery developers are also challenged to develop next generation products with no battery at all, requiring energy harvesting from environmental sources such as light, heat and vibration. Furthermore, the demand for longer life time and smaller size batteries increases as applications are increases.

To maximize battery lifetime as well as functionality developers of battery powered applications must consider many factors in their system architecture and designs. In current CMOS technologies, the sub threshold leakage current is much larger than the other leakage current components. This current can be calculated by using the following equation.

$I_{DS}=K\,(1-e^{V_{ds}/V_T})\,e\,(V_{GS}-V_T+V_{ds}/V_T)$.

Even in current generation technology, sub threshold leakage power dissipation is comparable to the dynamic power dissipation, and the fraction of the leakage power will increase significantly in the near future. [1], [2].

Leakage current and power is an important issue in Deep Sub Micron Technology. The main contribution of Leakage Power in CMOS circuits is due to dynamic power dissipation which increases with the reduction of threshold voltage, channel length, and thickness of the gate oxide.
The average power consumption of any logic circuit is
$P_{average} = P_{Static} + P_{Dynamic} + P_{Short\ Circuit}$

This paper mainly focuses on reduction of power consumption, area, delay, leakage at higher performance with MTCMOS technique. Section-II describes the design of conventional 1-bit full Subtractor. Section-III describes the design of 1-bit Full Subtractor with different techniques. Section-IV describes proposed one bit full Subtractor. Section-V presents the simulation results of Conventional and Proposed Subtractor with different power reduction techniques. Section-VI concludes this paper.

II. DESIGN OF CONVENTIONAL FULL ADDER

Conventional Full adder is a combinational circuit that performs addition between twobits taking into account that a one may have been added by a lower significant stage.

This circuit has three inputs and two outputs. The three inputs A, B and C denote the minuend, subtrahend and carry respectively.[3],[11].

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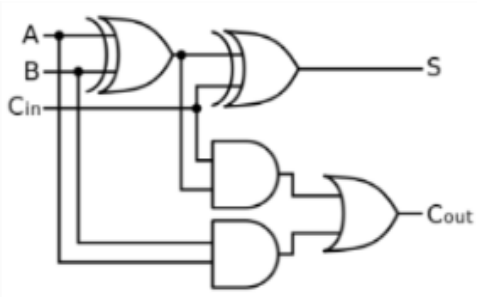

Fig 1. Logic Circuit of Conventional Full adder.

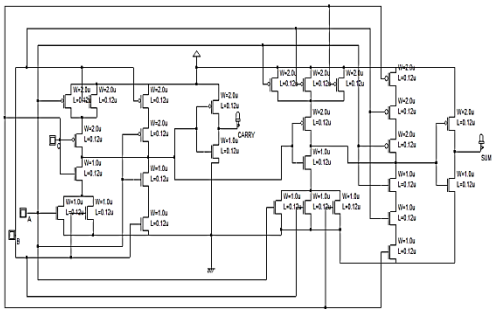

Fig 2. Transistor Level Circuit of Conventional Full adder.

The two outputs S and Cout represent sum and carry, respectively. The logic circuit and transistor level schematic of full adder is shown in Fig.1& Fig 2. and truth table in Table I. [12].

TABLE I: TRUTH TABLE OF FULL ADDER

Inputs			Outputs	
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S = A xor B xor C
Cout = AB + BC + AC
Where A, B, Cin inputs and S, Cout are outputs..

III. DESIGN OF 4-BIT , 16-BIT AND 32-BIT RCA WITH CONVENTIONAL FULL ADDER

Conventional Full Adder with twenty eight transistors is used for designing 4-bit and 16-bit ripple carry adder. As arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR and universal gates like NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).[6].

Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder, since each carry bit "ripples" to the next full adder.[7]. The block diagram of 4-bit Ripple Carry Adder is shown here below.

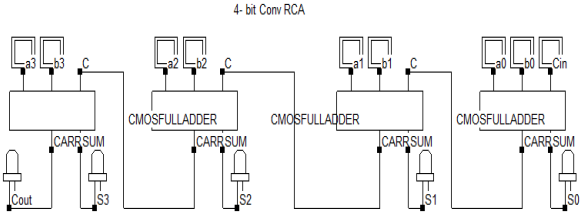

Fig 3. 4-Bit RCA with Conventional Full adder.

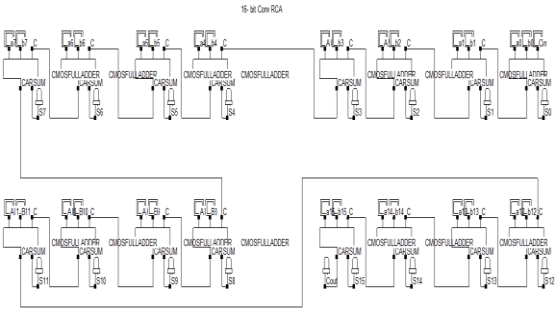

Fig 4. 16-Bit RCA with Conventional Full adder.

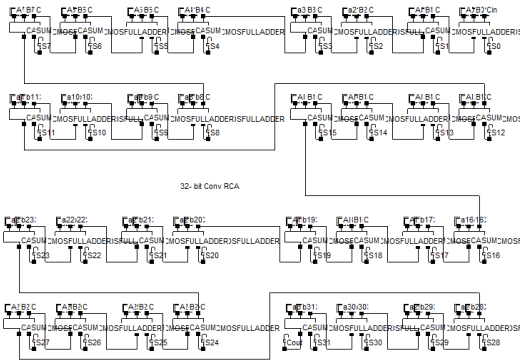

Fig 5.32-Bit RCA with Conventional Full adder.

IV. DESIGN OF PROPOSED FULL ADDER CELL.

The Circuit diagram of proposed Full Adder with ten transistors is shown in Fig 5. and the designed circuit is used for implementing four bit, sixteen bit and thirty two bit ripple carry adders for analyzing the performance of proposed adder cell in terms of delay, power, area and power delay product.[4],[5].

Table II, and III represents performance analysis of conventioanl and Proposed Ripple Carry Adderswith 4, 16 and 32-bits at 90nm and 65nm technologies, Table IV shows no. of transistots required for implementing Conventional and Proposed one bit Full Adder,Table V shows no. of Full Adder cells required for implementing 4, 16, and 32-bit RCA`s, where as Fig 7., Fig 8. and Fig 9. Shows 4-bit, 16-bit and 32-bit RCA`s, and Fig 10., and Fig 11 Represents Layouts of 32-bit Conventional and Proposed RCA`s, Fig 12. & Fig 13. Represents waveform

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of conventional and proposed 32-bit RCA`s (V vsI),where as Fig 14. & Fig 15 represents Graphical analysis of the results tabulated in Tables II, III.

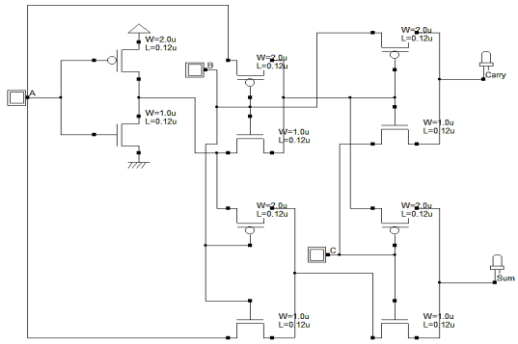

Fig 6. Full adder cell with ten transistors.

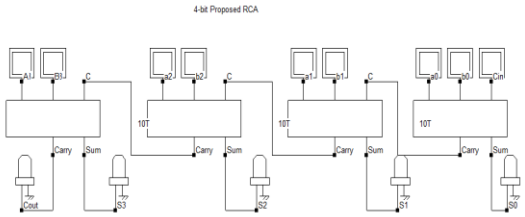

Fig 7. 4-bit Rippple Carry Adder with proposed adder cell.

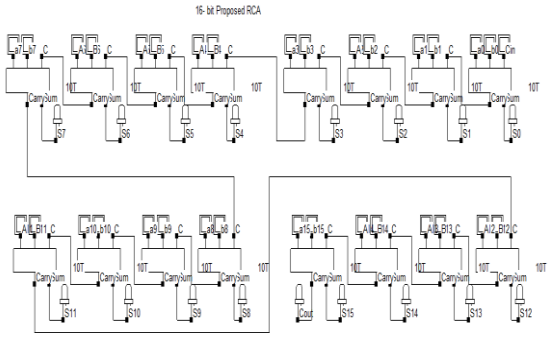

Fig 8.16-bit Rippple Carry Adder cell proposed adder cell.

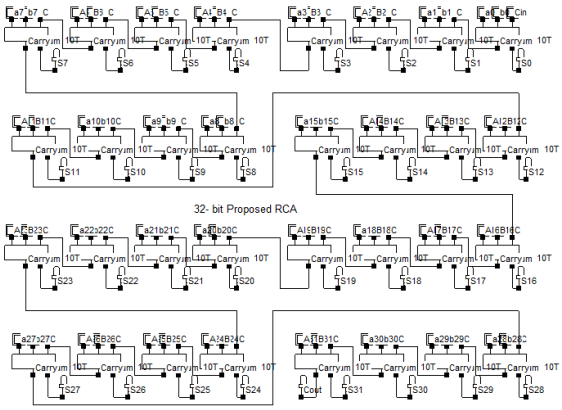

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Fig 9. 32-bit Rippple Carry Adder cell proposed adder cell.

V. SIMULATION RESULTS

Performance analysis of 4-bit, 16-bit and 32-bit Ripple carry Adders with proposed Adder cell is analyzed in Microwind 3.1 CAD tool in 90nm and 65 nm technologies. Comparison is done in terms of power, delay, area and power delay product in 90nm and 65nm technologies at room temperature.[10].

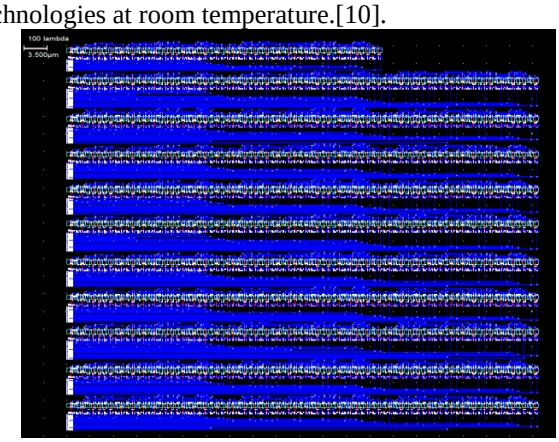

Fig 10. Layout of 32-bit Rippple Carry Adder with Conventional Full adder.

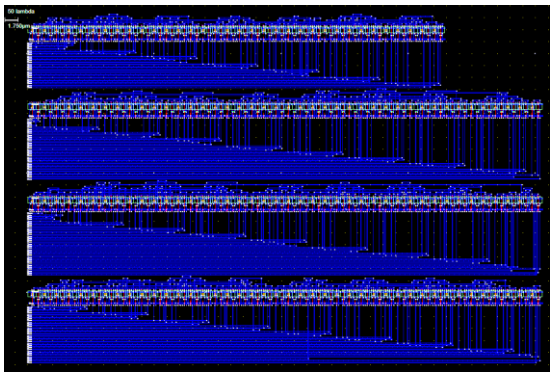

Fig 11. Layout of 32-bit Rippple Carry Adder with Proposed Full adder.

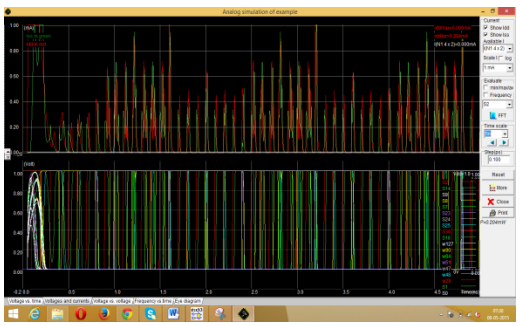

Fig 12. Waveform of 32-bit RCA with Conventional Full adder(V vs I).

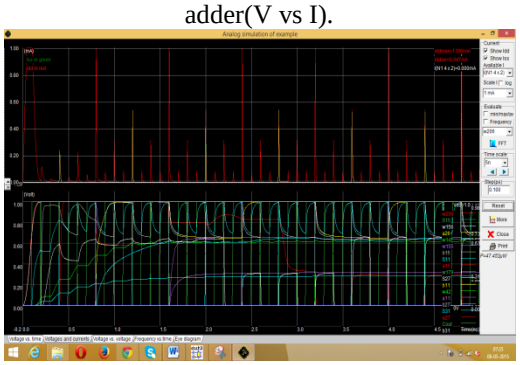

Fig 13. Waveform of 32-bit RCA with Proposed Full adder(V vs I).

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TABLE II. SIMULATION RESULTS OF CONVENTIONAL AND PROPOSED CIRCUITS IN 90NM/27^{0}C

ADDERS	AREA (μm^2)	POWER in (μw)	DELAY in (ns)	PDP VALUE (μw X ns)
CONVENTIONAL FULL ADDER	288	121.00	0515	62.315
4- bit RCA	1472	237.00	1.385	328.24
16- bit RCA	3956	319.00	4.865	1551.9
32- bit RCA	6992	543.00	9.505	5161.2
PROPOSED FULL ADDER	108	18.985	0.365	6.7586
4- bit RCA	450	56.839	0.740	42.060
16- bit RCA	2208	77.374	2.240	173.31
32- bit RCA	3404	110.00	4.240	466.40

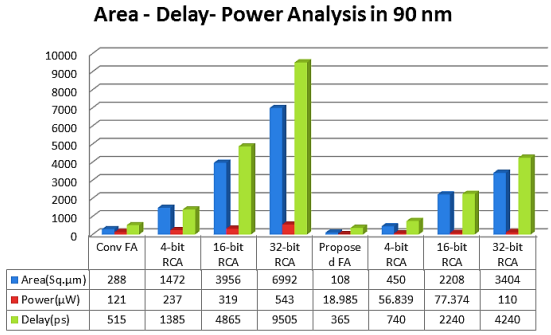

Fig 14. Graphical Analysis of the results tabulated in Table II.

TABLE III. SIMULATION RESULTS OF CONVENTIONAL AND PROPOSED CIRCUITS IN 65NM/27^{0}C

ADDERS	AREA (μm^2)	POWER in (μw)	DELAY in (ns)	PDP VALUE(μw X ns)
CONVENTIONAL FULL ADDER	168	43.393	0.250	10.848
4- bit RCA	936	108.00	0.663	71.604
16- bit RCA	2376	137.00	2.319	317.703
32- bit RCA	4248	248.00	4.527	1122.69
PROPOSED FULL ADDER	63	8.8070	0.178	1.5676
4- bit RCA	280	24.674	0.359	8.8579
16- bit RCA	1296	34.839	1.085	37.8003
32- bit RCA	2016	47.453	2.054	97.468

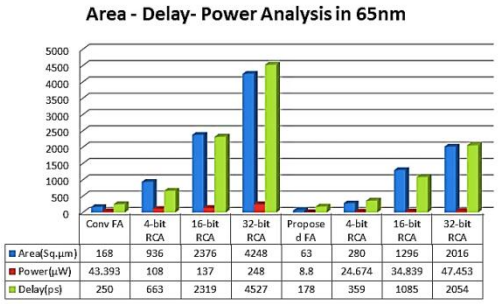

Fig 15. Graphical Analysis of the results tabulated in Table III.

VI. CONCLUSION

Simulation results show reduction in power consumption which leads to reduction in leakage current and power using Microwind/DSCH 3.1 tool in 90nm and 65nm technologies. Finally observed that Proposed 32-bit Ripple Carry Adder with ten transistors is Energy Efficient one as the power delay product value is less compared to other Ripple Carry Adder architectures. Future work is carrying out in designing 64-bit and 128-bit RCA`s with the proposed Adder cell.

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