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# Low Power Array Multiplier using Modified GDI Cell for Full Output Swing

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**Abstract**: One of the mostly used circuits in the digital designs is Multiplier. In digital signal processing multiplication is the most commonly used function. Due to high throughput hardware multiplication is most commonly used. Many designs of multiplier have already been proposed for low power. GDI (Gate Diffusion Input) a new technique for low power Multiplier design has a limitation of low output swing. Here a modified GDI cell based multiplier is designed and used for Low power and full output swing.

**Keywords**: GDI- Gate diffusion Input, Multiplier, Multiplexor, Adder, Low power

## I. INTRODUCTION

As the requirement of portable devices are increasing, the need of high speed, small and low power circuits are triggering a lot of research efforts. The author in [1] has talked about the GDI technology for designing small circuits with small number of transistors for low power design. A GDI cell is proposed which has only two transistors and can generate 8 different outputs.

Many researches are done in the field of low power circuits and many different designs are proposed [2-4]. Based on CMOS technology, popular low power design technique is PTL(Pass Transistor Logic). It is the mostly used design in past few years. The main advantages are High Speed, Low power dissipation, and small area (due to small number of transistors). The main disadvantages are, First at low voltage levels the device operation becomes slow due to threshold drop at transistor, it is very important for low power designs because we operate at lowest possible voltage for low power design. Second since the PMOS devices doesn't fully turned off, there will be a direct path formed between supply and ground when input is high which results in static power dissipation[3].

There are many other methods for low power circuit designs. Transmission gate technique uses complementary transistors to realize complex circuits. Complementary pass-transistor logic (CPL) uses complementary inputs and outputs using NMOS pass transistor logic but has the problem of high static power dissipation. Double pass-transistor logic (DPL) uses complementary transistors to keep full swing operation and reduce the static power consumption but suffers from large area.
GDI technique solves most of the problems discussed above but has the drawback of low output swing. As PMOS passes bad logic 0 and good logic 1, and NMOS is good at logic 0 and bad at logic 1. Due the above characteristics GDI suffer from low output swing. In this paper, we have designed modified GDI based AND and OR gates for full output swing. Using those gates GDI adder is designed. Finally the 4-bit multiplier is designed based on the adder. Finally the results of modified GDI multiplier is compared against CMOS results. The outline of the paper includes Section II contains the description of basic GDI cell, Section III deals with Implementation, Section IV contain implementation of adder and multiplier, section V deals with simulation results and finally Section VI Conclusion - detailing the outcome of this project.

## II. GDI CELL

The basic GDI cell is shown in the Figure 1.

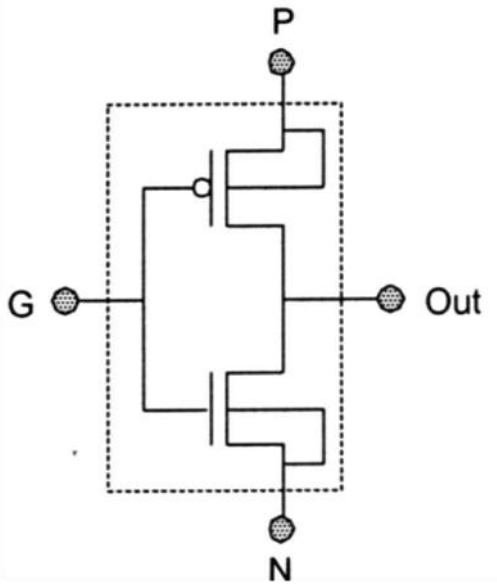


Figure 1. GDI Cell circuit

The basic GDI cell has three Inputs: G (Gate terminal of PMOS and NMOS), P (Input to source of PMOS), N (Input to drain of NMOS). Giving different values at the input results in different Boolean functions at the output. Most of the functions realized by this two transistor circuit are very complex when made using CMOS. Table 1 show the output of the GDI cell for different input combinations.

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| N | P | G | Out | Function |
|---|---|---|---|---|
| '0' | B | A | $\overline{A}B$ | F1 |
| B | '1' | A | $\overline{A}+B$ | F2 |
| '1' | B | A | $A+B$ | OR |
| B | '0' | A | $AB$ | AND |
| C | B | A | $\overline{A}B+AC$ | MUX |

Table 1: Output of GDI cell for different input values.

## III. IMPLEMENTATION

For the multiplication purpose the basic circuits of AND and MUX are modified for full output swing. The AND gate is realized using only 2 transistors using basic GDI cell. An extra transistor is added to it for getting full swing. The modified AND gate circuit is shown in figure 2.

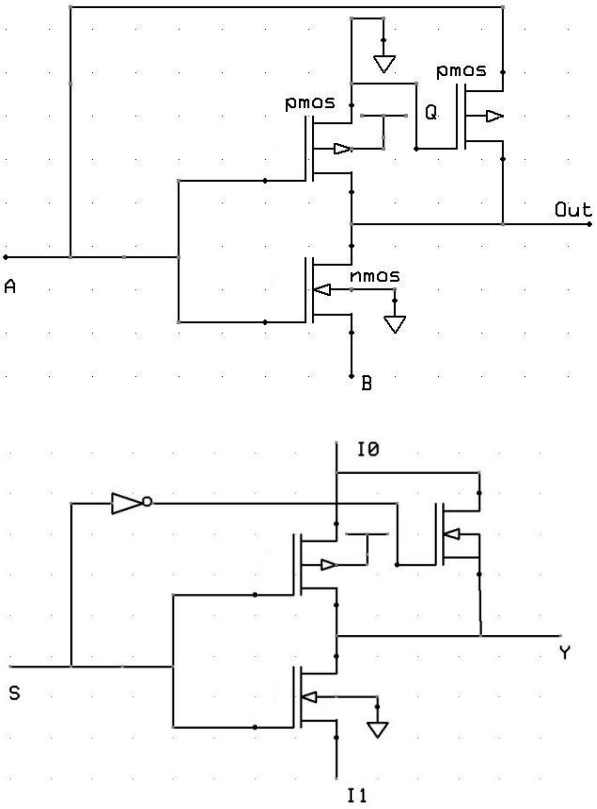


Figure 2: Modified Adder for Proper Output Swing
Figure 3: Modified MUX for Proper Output Swing

The MUX circuit is also modified for full output swing. An extra pmos is added to get full output swing. . This new design shown in Figure 3 give a better output swing as compared to normal GDI cell.

## IV. IMPLEMENTATION OF ADDER AND MULTIPLIER

In the design of conventional array multipliers a full adder made using GDI mux is being used. Figure 4 Shown below is a full adder made using MUX. It is made up of three 2:1 MUX. A number of designs of adder are proposed, but the adder made using MUX consume less power and area compared to others. Table 2 show the output of Full adder.

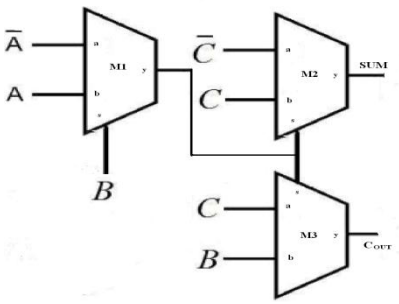


Figure 3: Full Adder Circuit using three 2:1 MUX

| A | B | C | SUM | CARRY |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Table 2: Full adder operation

Conventional array multiplier here is designed using full adder in which multiplication is obtained by partial product method. In a digital system an array multiplier involves the parallel multiplication, which is done in the following three steps:

1. Generation of partial product (PP) bits.
2. The accumulation of partial product (PP) bits into two rows.
3. The computation of final product generally using a carry propagate adder (CPA).

Figure 5 show the diagram of conventional array Multiplier.

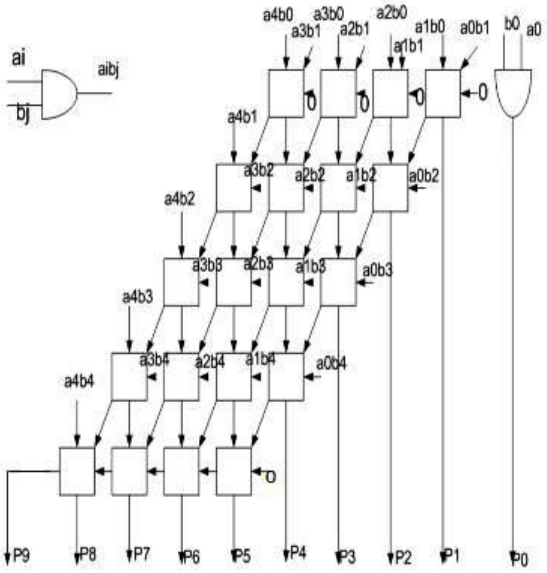


Figure 5: Array Multiplier

## V. SIMULATION RESULTS

The implementation is done using Cadence Spectre with standard UMC 180nm CMOS technology. The results

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obtained were compared with the results of its CMOS implementation. Table 3 shows the result of GDI based multiplier implementation and table 4 show the result of CMOS implementation.

| Component | Number of Transistors | Static power | Dynamic Power |
|---|---|---|---|
| **AND Gate** | 3 | 23.4fW | 62.3pW |
| **MUX** | 5 | 28nW | 839nW |
| **ADDER** | 23 | 25nW | 4.9uW |
| **Multiplier** | 484 | 4.5nW | 43.1uW |

Table 3: Power Consumption Using GDI Logic

| Component | Number of Transistors | Static power | Dynamic Power |
|---|---|---|---|
| **AND Gate** | 6 | 1.46nW | 783nW |
| **MUX** | 20 | .47nW | 2.6uW |
| **ADDER** | 64 | 1.1nW | 6.4uW |
| **Multiplier** | 864 | .13nW | 48.6uW |

Table 4: Power Consumption Using CMOS Logic

## VI. CONCLUSION

By using the proposed GDI multiplier high performance can be achieved. Following conclusions have been made:

- The Proposed GDI multiplier consume 11.2% Less power as compared to CMOS.
- The Static Power Consumption of GDI Logic is more than CMOS but the Overall power consumption is less when compared to CMOS
- The Transistor count in GDI logic is very much lesser than CMOS. Using GDI multiplier we can save the area by 43%.

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