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Adiabatic Vedic Multipler Design Using Chinese Abacus Approach

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Abstract: In this paper, we discuss the implementation of Vedic multiplier with Chinese Abacus adder design, using Reversible Logic Gates. The power consumption of the Vedic multiplier is low as it generates all partial products and their sum in one step. Since high radix of Chinese Abacus adder reduces the carry propagation delay, it is observed here that the proposed design increases the speed of operation manifold. The proposed work is implemented on the Xilinx FPGA device, Spartan-3E. The results show that multiplier implemented using Chinese Abacus approach is quite efficient in terms of area, time and speed

Keywords: Vedic Multiplier, Chinese Abacus Adder, propagation delay, Reversible Logic.

I. INTRODUCTION

Multiplier is one of the important blocks in almost all the arithmetic logic units. These multipliers are mostly used in the fields of Digital Signal Processing (DSP), Fast Fourier Transforms, convolution, filtering and microprocessor applications. A system's performance is generally determined by the performance of the multiplier, because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. A high speed and area efficient multiplier can be achieved by using Vedic mathematics. In this work, we have implemented the Vedic multiplier using Chinese Abacus Adder with and without using Reversible logic gates.

Reversible logic is one of the promising fields for future low power design technologies. Since one of the requirements of all DSP processors and other embedded devices is to minimize power dissipation, multipliers with high speed and lower dissipation are critical. This paper proposes an implementation of Reversible *Urdhva Tiryakbhayam* (UT) Multiplier which consists of two cardinal features. One is the fast multiplication feature derived from Vedic algorithm *Urdhva Tiryakbhayam* and another is the reduced heat dissipation by the virtue of implementing the circuit using reversible logic gates. The paper is partitioned into six sections. Section II gives introduction on reversible logic. Section III explains the *Urdhva Tiryakbhayam* (UT) algorithm. Section IV explains the Chinese Abacus Adder algorithm, Section V elaborates on the design aspects of Reversible UT Multiplier. Section VI gives the simulation results. Conc1usions and references follow

II. REVERSIBLE LOGIC

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in proximity. The basic principle of reversible computing is that an objective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation. A reversible logic gate is an N-input, N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

The following are the important design constraints for reversible logic circuits:

1. Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantum cost.
3. The design can be optimized so as to produce minimum number of garbage outputs.
4. The reversible logic circuits must use minimum number of constant inputs.
5. The reversible logic circuits must use a minimum logic depth or gate levels.

The basic reversible logic gates encountered during the design are listed below:

1. Feynman Gate [1]:

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.

2. Peres Gate [2]:

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.

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3. Fredkin Gate [3]:

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost five. It can be used to implement a Multiplexer.

4. HNG Gate[4]:

It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost six. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus
minimizing the garbage and gate counts.

5. NFT Gate[5]:

The 3*3 New Fault Tolerant gate (NFT) with quantum cost of 5 has worst case delay of 3 and it has better correction capability. The output states map to the inputs in this manner.

A = A XOR B,
B = AC' XOR B'C, and
C = AC' XORB C

6. F2G Gate[5]

The 3*3 Feynman double gate gate with quantum cost of 2 has worst case delay of 3 and it has better correction capability

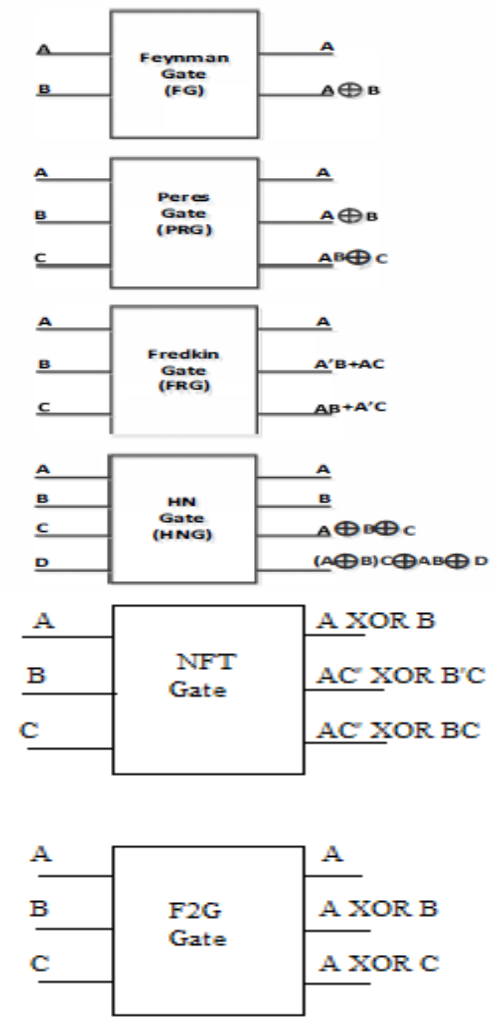

Figure1: Reversible Logic Gates[1][2][3][4][5]

III. URDHAVA – TIRYAGBHYAM

The multiplier is based on an algorithm *Urdhva Tiryakbhyam* (Vertical & Crosswise) of ancient Indian Vedic Mathematics. *Urdhva Tiryakbhyam* Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products.

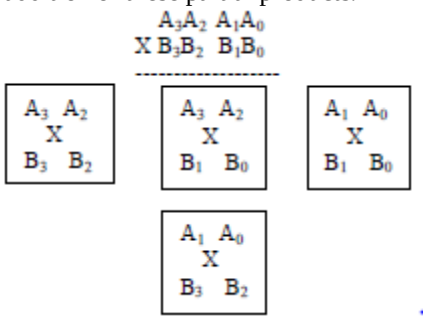

Figure 2: Block diagram of 4x4 vedic multiplication.

For NXN multiplication unit, we require four N/2 bit multipliers and three N bit full adders. 4x4 bit multiplication has been shown in Fig.3. High speed of multiplier depends mainly upon speed of the adder units used.

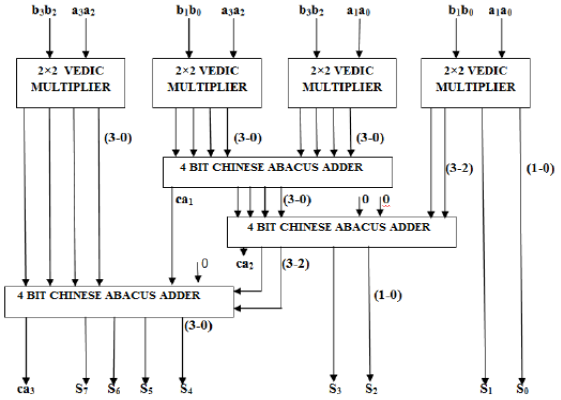

Figure3: Block diagram of proposed 4x4 Vedic multiplier using Chinese Abacus Adder

IV. CHINESE ABACUS

Chinese Abacus is the ancient approach used for performing mathematical calculation in many parts of the world, especially in China. It is still used by many small enterprises for their day to day work. Due to its high speed of operation, it give high competition to electronic pocket calculator. Similar efficiency can be attained in electronic version.

The first digital arithmetic circuit employing the Chinese abacus approach were proposed by Maloberti et al. [6-8]. The architecture of radix-4 abacus adder is presented in [6]. The architecture of radix-2 abacus adder is presented in [7] and [8]. The most severe drawback of Maloberti's adder in radix-4 design is the serial addition of each bead by the Shift-Up module. The serial addition of each bead by the Shift-Up module can be improved by the parallel addition

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module of the proposed architecture. The serial addition of each bead by the Shift-Up module will moreover induce more than nine pass transistor chains, due to its counting method. The delay time of the signal waveform becomes long.

Radix-4 adder helps in reducing the excessive delay by reducing the number of carries [9]. A basic column element of the Chinese abacus is depicted in figure 4(a). The configuration showed in figure 4(a) represents the number six. Each column element has one higher bead with a weight, of five and four lower beads with a weight of one. The key feature of the Chinese abacus is the use of one bead with weight five. This allows the operator to minimize the transmission of rests.

In this paper, we use abacus adder in each column having three beads higher and three beads lower, each having weight of four and one each, respectively. The basic element is able to represent decimal number in the range 0 to 15. Figure 4(b) depicts the abacus representation of decimal number 9. In this methodology, the 4-bit adder only contributes two ripple carries. One is internal carry from lower beads to higher beads, the other is external carry from this column element to a next neighbour column element.

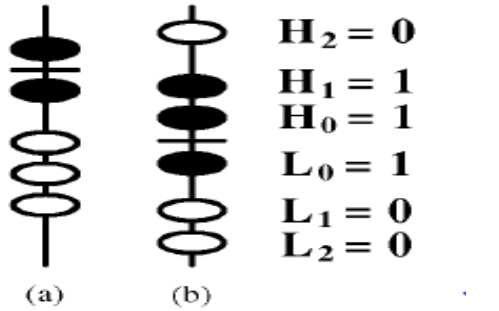

Figure 4. (a) Chinese abacus coding with base 10 of the decimal number 6, (b) the proposed Chinese abacus adder coding with base 16 of the decimal number 9 [7].

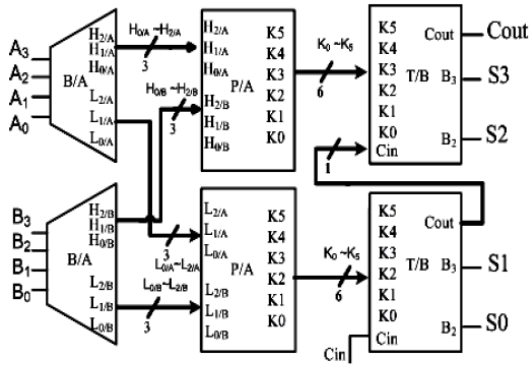

Figure 5. Block diagram of the 4-bit abacus adder[10].

Block diagram of radix-4 abacus adder is depicted in figure 5. As shown in figure 5, the function of radix-4 abacus adder is completed in four phases. In first phase binary input is converted into abacus output known as B/A(binary to abacus) module. In second phase, parallel additon takes place known as P/A(parallel addition module). In the last (third) phase thermometric input converted into binary output known as T/B(thermometric to binary) transformation module.

V. IMPLEMENTATION OF PROPOSED DESIGN AND SIMULATION RESULTS

The 4x4 Vedic multiplier is design using the Chinese abacus methodology. It may simply use three 4-bit abacus adders, shown in figure 3. We design all component of multiplier using reversible logic gates.

The digital logic implementation of the 2X2 Urdhva Tiryakbhayam multiplier using the conventional logic gates [11] is as shown in figure 6. The expressions for the four output bits are given below figure 6. The block diagram of reversible logic gate implementation of 2x2 UT multiplier is as shown in figure 7. This design does not consider the fanouts.

The circuit requires a total of six reversible logic gates out of which five are Peres gates and remaining one is the Feynman Gate. The quantum cost of the 2X2 Urdhva Tiryakbhayam Multiplier is enumerated to be 21. The number of garbage outputs is 9 and number of constant inputs is 4.

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 3. It consists of four 2X2 multipliers, each of which processes four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the four bit abacus adder.

The other four input bits for the abacus adder are obtained from the second 2X2 multiplier. Likewise, the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit abacus adder. The outputs of these four bit adders are in turn 5 bits each, which need to be summed up. This is done by a five bit abacus adder which generates a six bit output. These six bits form the upper bits of the final result.

The Chinese abacus adder is consummated (realized) using the NFT and F2G Gate. Single NFT Full Adder (SNFA**)** is a Fault Tolerant full adder circuit which consists of one New Fault Tolerant (NFT) gate and three Feynman Double (F2G) gates where the quantum cost is 11 and the total number of garbage outputs is 3.

This design also does not take into consideration the fanouts of the gates. For this design the quantum cost is computed to be 162, the total number of gates used will be 36, the number of garbage outputs will be 62 and the number of constant inputs will be 29.

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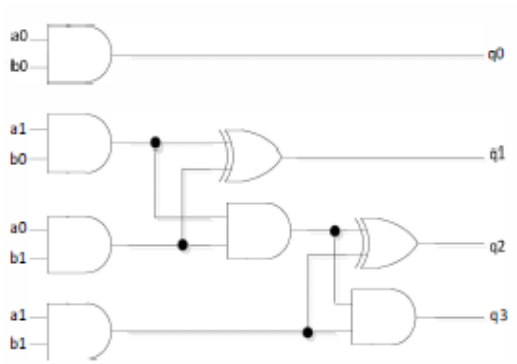

Figure 6: Conventinal Logic Implementation of 2x2 UT multiplier

q0 = a0.b0
ql= (a1.b0) xor (a0.bl)
q2= (a0.al.b0.bl) xor (al.bl)
q3= a0.al.b0.bl

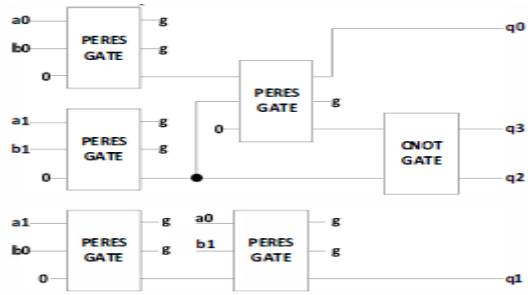

Figure 7: Reversible logic gate implementation of 2x2 UT multiplier.

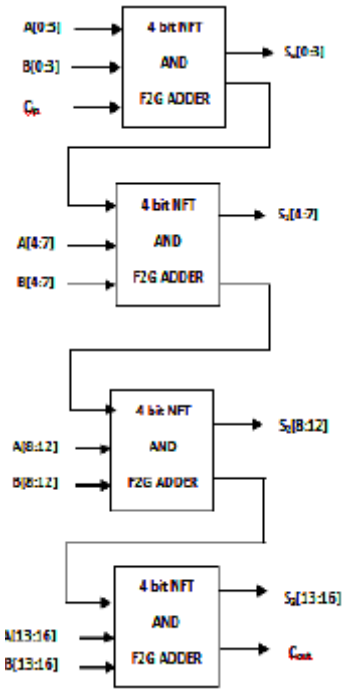

Figure 8: Reversible logic gate implementation of Chinese Abacus Adder.

Simulation of the proposed work is done using Modelsim SE 6.5. Synthesis and Implementation is done using Xilinx Spartan-3E FPGA Board of device family xc3s50-4-tq144. The subsequent figures show the simulation, RTL and Technical Schematic of the multiplier. Results show that 4x4 UT vedic multiplier designed in this work using reversible logic gates, consumes less area and has high speed as compared to 4x4 UT vedic multiplier designed using conventional logic gates. Results also show that 4x4 UT vedic multiplier designed using reversible logic gates is 23% faster and takes less area than 4x4 UT vedic multiplier design without using reversible logic gates

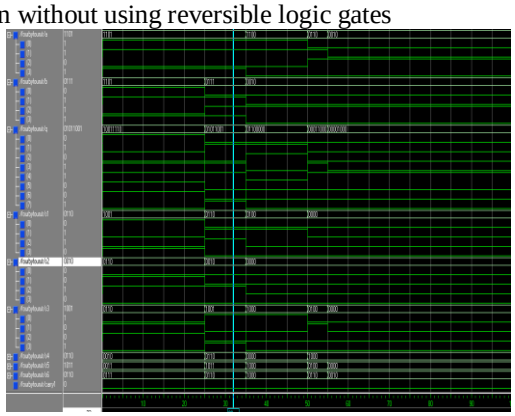

Figure 9: Simulation result for 4x4 bit Vedic multiplier designed using reversible Logic gates

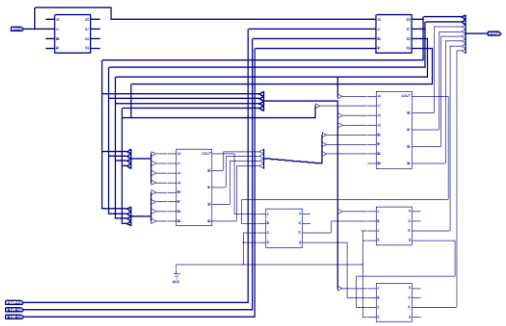

Figure 10: RTL view of 4x4 bit UT Vedic multiplier designed using reversible logic gates.

TABLE I: SIMULTAION RESULTS OF DEVICE UTILIZATION

Methods	**UT Vedic multiplier without reversible logic gates**	**UT Vedic multiplier with reversible logic gates**
Number of slices	36 out of 768 (4%)	28 out of 768 (3%)
Number of 4 input LUTs	65 out of 1536 (4%)	49 out 1536 (3%)
Number of bonded IOBs	17 out of 97 (17%)	16 out of 97 (17%)
Net propagation delay	20.705 ns	15.830 ns
Frequency	48.297MHz	63.17MHz

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VI. CONCLUSION

The use of Vedic multiplier approach results in a competitive technique as compared respect to conventional fast multiplier. The simulation results show that this approach of Vedic multiplier using Chinese Abacus adder is very efficient for low-power, high-speed applications. This architecture is also easy for pipeline implementation. Another advantage is that the methodology may reduce the number of ripple carries and partial product generation in many steps. It can be inferred that Vedic multiplier using Chinese Abacus adder is quite efficient as compared to the conventional multiplier, for multiplication operation.

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