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Impact of Scaling Digital Circuit Design Technology on Solid State Logic Style Selection

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Abstract: As technology scales into deep submicron regime, secondary effects became increasingly important. Sub threshold current, interconnect capacitance and Vth variation due to process variation can easily dominate the performance. In this work we study these effects and how much they affect performance of different logic styles as technology scales. We laid-out a 16-bit carry-bypass adder in CMOS, LEAP and XGATE (transmission gate) logic styles, simulated it in various technologies and we present our results and conclusions.

I. INTRODUCTION

As technology scales into the deep submicron regime, many secondary effects that were not an issue in long-channel devices become increasingly important. This is a result of both shrinking of the feature size and the continuous lowering of supply and threshold voltages. The causes and effects of these emerging secondary effects are widely discussed in the literature [1, 2, 3].

However, most of these researches focused on the effect of technology scaling on the device level, ignoring many of the issues involved in practical digital circuit design. This paper will examine the impact of the technology scaling from a circuit designer's perspective, and evaluate the implication of technology scaling on logic style selection. In particular, we will consider three effects that become very important as technology scales into deep submicron, and how they affect performance in different logic styles. These effects are:

1) The increasing subthreshold current caused by decreasing Vth.
2) The interconnect capacitance that starts to dominate performance due to the poor scalability of the fringing capacitance.
3) The Vth (threshold voltage) variation caused by poor process control at deep submicron.

The rest of this report is organized as follows. Section 2 will describe the simulation environment under which we did our simulations. Section 3 will show how the power consumption, circuit delay, and power-delay-product of each logic style scales as technology scales, and will also present some comparative results among the different logic styles.

Section 4 will examine the effect of interconnect capacitance and its implication on performance degradation. Section 5 will examine the effect of threshold voltage variation on circuit performance. Finally, section 6 will present our main conclusions.

II. SIMULATION ENVIRONMENT

We laid-out a 16-bit carry bypass adder in three different logic styles: 1. Static CMOS [7], 2. LEAP standard cell as proposed in [5], and 3. A design style based on transmission gates which will be referred to as XGATE for the rest of this report. We used the magic layout editor to design the layouts and its extraction tool to extract the corresponding spice decks which were simulated using hspice.

Each simulation consisted of giving sequentially 8 inputs to the adder, one every 60ns, i.e. a total of 480ns. The inputs were selected in an appropriate way to generate glitches and worst-case propagation delays.

Across different technologies, it is assumed that the thickness of insulating oxide between different metal layers is kept constant. As a result, coupling plate capacitance per unit area between different metal layers is also kept constant.

It is further assumed that, to avoid quadratic increase in metal resistance, the height of a metal layer remains constant. As a result, if the minimum feature size of a technology scales by S, the coupling capacitance between wires of the same layer scales by 1/S as pitch size of metals decreases with S. Finally, the fringing capacitance per unit length from the sidewall of a metal to an adjacent plane is estimated by $\frac{2\pi\varepsilon}{\log(d/h)}$, where d is the distance between metal layer and h is the height of a wire [4]. Using the same assumption as above, both d and h are independent of scaling. As a result, the value for fringing capacitance per unit length is kept constant.

To account for feature size decrease and technology scaling in our simulations we had to modify the magic technology file and the SPICE transistor models (original versions of models were obtained from www.mosis.org).

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2.1 Magic technology file

Magic' extraction tool uses a technology file to specify the values of the different kinds of capacitance. Since this information depends on the feature size we had to modify the technology file and essentially parameterize it across the feature size.

2.2 SPICE transistor models

To account for secondary effect presents in sub-micron technology, a BSIM3V3 model [8] is used. Special attention was paid to the modeling of threshold voltage as it will be shown that threshold voltage is one of the most important parameters that determine a circuit's performance and reliability.

Since many of the parameters in a BSIM3V3 model are curve-fitting constants from experimental results, it is difficult to predict their values for a future technology. As a result, to model the effect of scaling, only those that have a significant impact on the simulation results were modified. By observing their effects on the transfer characteristic of a MOSFET, we concluded that the following three parameters are the most important to model scaling of deep-submicron technologies: TOX, VTH0 and K1. TOX is scaled with the same factor as the minimum feature size. VTH0 is a simulation parameter specified by a particular test case. VTH0 corresponds to the values of "Vth (threshold voltage)" in subsequent sections, which is the nominal threshold voltage value at long channel. K1 is the first order body-bias dependency of γ in long channel devices. The value of K1 is back calculated from the value of VTH0 given, assuming VFB stays constant across technology. Although this estimation does not follow the physical derivation of its value, it does serve as an easy-to-obtain estimation for future technology that we don't have information about.

Based on these modifications to accommodate for technology scaling, we simulated all the combinations of the following parameters: logic style (one of CMOS, LEAP, XGATE), feature size Lmin (one of 0.04µ, 0.08µ, 0.1µ, 0.2µ, 0.3µ, 0.4µ), Vdd (one of 0.2V, 0.4V, 0.6V, …, 2.0V), threshold voltage Vth (one of 0.2V, 0.3V, 0.4V, 0.5V, Vdd/3, Vdd/4) and interconnect capacitance (included or not included in the spice decks). For every such simulation we measured the following parameters for the 16-bit carry-bypass adder: Delay, Power, Energy, PDP (Power-Delay-Product) and EDP (Energy-Delay-Product).

III. POWER, DELAY AND POWER DELAY PRODUCT

For high performance circuits, worst case delay is the primary metric for evaluating a circuit. On the other hand, for low-power circuits, power-delay-product, or in the case of portable devices, energy-delay-product is a more important metric. Under our simulation procedure, in which a fixed input sequence is fed into the circuits at fixed frequency, regardless of the actual speed of the circuit, energy consumption and power consumption are correlated. As a result, for simplicity sake, we will only consider power consumption and power-delay-product in our analysis.

In the following 3 subsections, we will analyze the effect of technology scaling on worst-case delay, power, and power-delay-product (PDP) of different logic styles. All the graphs that will be presented measure one of these 3 performance criteria across all values of Vdd and Lmin that we simulated. For each specific pair of values for Vdd and Lmin the value shown is the minimum one obtained over all the values of Vth that we simulated. These graphs can be seen in Figures 1 through 9.

3.1. Delay

Figures 1 to 3 show the delay of the 3 logic styles for all Vdd's and Lmin's simulated (as we said before, the values shown correspond to the minimum ones obtained over all the values of Vth that we simulated). For larger values of Vdd not much influence is apparent, and delay remains approximately constant. A sharp increase in delay can be observed below Vdd=0.4V. We can also observe that decreasing feature size leads to decreased Vth which in turn leads to more current and decreased delay.

As seen from the graphs, regardless of logic style, the minimum delay of a circuit can always be achieved at the highest Vdd (with the lowest possible Vth). This rule still holds at deep submicron technology. That means, for high performance scaling, the lowest possible Vth should be chosen before sub-threshold current becomes dominant. On the other hand, Vdd should be chosen to be as high as possible so that the circuit still meets the power consumption requirement. Most importantly, Vdd should be upper-limited by the reliability margin to prevent the circuit from suffering from the channel hot-carrier effect. These conclusions confirm the suggestions in [1].

Figure 4 shows how the minimum delay (across all Vdd's and Vth's) for each logic style scales. Since we are interested in the scaling and not in the absolute value, all the minimum delays are normalized to the minimum delay that corresponds to a feature size of 0.4µ. We can see that delay for all 3 logic styles scales pretty well. CMOS shows the best scaling in delay with XGATE being very close at least down to a feature of 0.1µ. LEAP starts deviating from the other 2 styles at a bigger feature size. This is mainly due to the fact that subthreshold current, together with the non-uniform scaling of PMOS and NMOS upsets the circuit balance and thus the performance of the level-restoring PMOS transistor at the output of each LEAP cell.

3.2 Power

Figures 5 to 7 show the power consumption of the 3 logic styles for all Vdd's and Lmin's simulated (the minimum values across all simulated Vth's). Power consumption for CMOS has a minimum for Vdd=0.4 V. Below that, subthreshold current dominates power consumption when compared with dynamic switching power consumption.
In the case of LEAP, high degree of fluctuation occurs for Lmin=0.04µ. This may be due to the circuit's high

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sensitivity to threshold voltage variation as will be shown in section 5. Despite the fluctuation, power consumption at Lmin=0.04μ is higher than at Lmin=0.08μ. This indicates the significant direct path current flowing through the level-restoring PMOS.

Finally, the power consumption of XGATE almost stays constant over different feature sizes. This is probably due to the fact that interconnect capacitance dominates in this style due to the very long polys used.

3.3. Power-Delay-Product (PDP)

Figures 8 to 10 show the PDP of the 3 logic styles for all Vdd's and Lmin's simulated (the minimum values across all simulated Vth's). The PDP of CMOS exhibits the classic U-shape characteristic with minimum value around Vdd=0.4V. LEAP has a similar behavior. On the other hand, XGATE shows a monotonic decreasing PDP. It is probably the case that it has a minimum for a Vdd less than 0.2V.

Figure 11 shows how the PDP (its minimum value across all Vdd's and Vth's) for each logic style scales. As was the case for the delay, here too we have normalized the PDPs to the PDP that corresponds to a feature size of 0.4μ. Again CMOS exhibits the best scalability. XGATE has the worst scalability. The poor scaling of XGATE follows directly from the fact that power consumption of XGATE stays about constant as feature size changes (as explained in 3.2), i.e. power doesn't scale well. The scaling of LEAP's PDP follow that of CMOS closely, until Lmin=0.04μ.

An observation that we made is that the values of Vdd and Vth where the minimum PDPs occurred (these values are not shown in the graphs) exhibit an interesting relation. For CMOS, the optimal PDP occurs when Vdd / Vth is around 2.1. For LEAP, this ratio is about 2.6, and for XGATE, it is about 1.5.

IV. EFFECT OF INTERCONNECT

The parasitic effects introduced by interconnect wires become more important as device dimensions are reduced and tend to dominate the performance in submicron technologies. In the designs that we laid-out and simulated, these effects consist only of the capacitive parasitics. The resistive and inductive parasitics are negligible since the wires are very short. The scaling behavior of these effects is different from the one of active devices, which makes them even more pronounced for deep-submicron technologies.

In this work we tried to measure how much the Delay, Power and PDP of the 16-bit carry-bypass adder designed in the 3 logic styles, are affected by the capacitance introduced by interconnect. To do so, we generated 2 spice decks for every design style and every feature size that we simulated; one with the interconnect capacitance (as extracted from within magic), and one without (by deleting all caps from the first one). Then, we run all our simulations for both kinds of spice decks.

The capacitance of the interconnect is usually extracted from the layout of the circuit. This means that the spice decks without the interconnect capacitances also correspond to the ones that a designer would make to have a pre-layout simulation of his/her design and estimate its performance, before actually going into laying it out. Therefore, the effects of the interconnect capacitance on circuit performance can also be thought of as the error in pre-layout performance estimation.

Figure 12 show the effect of interconnect capacitance for the cases of Delay, Power and PDP respectively. We see that CMOS is the logic style least affected by interconnect capacitance. Its delay shows a 20-30% increase due to interconnect capacitance. We can attribute this to its compact layout that uses very short wires. LEAP delay shows an increase of about 30% to more than 50% for deep submicron technology. We should note that even though LEAP layout has a lot of long wires, it is also a standard cell approach using oversized transistors which partly alleviates the problems caused by the long wires. XGATE is the design style most affected by the interconnect capacitance. Its delay increase ranges from 35% up to 55% for deep-submicron technologies. That is because its layout uses a lot of long wires while transistors are not really oversized.

V. THRESHOLD VARIATION

Despite the advancement in fabrication process to produce transistors of smaller and smaller feature sizes, threshold control of fabrication process has not been advanced at the same pace. Up to 0.15V of threshold variation is not uncommon[6]. This process variation becomes very significant when the threshold voltage of the circuit is pushed towards lower and lower values. At deep submicron technology, running at sub-1V supply voltage, threshold voltage is pushed to around 0.3V. Therefore, a 0.1V variation in threshold voltage implies a change of more than thirty percent. Figure 13 illustrates the effect of threshold variation on circuit delay for different logic styles. At a nominal Vth of 0.2V, a variation of ±0.05V is applied. At a supply voltage of 1V, this translates into almost 20% increase in delay for CMOS and XGATE, and 25% increase for LEAP. At Vdd=0.6V, this increases dramatically to almost 40% increase in delay for CMOS and XGATE, and more than 50% for LEAP.

From the figure, it can be concluded that as the ratio between Vdd and Vth becomes smaller, the effect of threshold variation becomes more significant. The effect is even more noticeable at very low Vth when the circuit is sitting at the edge of subthreshold current conduction. Note that we have only applied a variation of 0.05V to the threshold, which is a relative small value when compared with nowadays process technology. As a result, to ensure reliability and predictability of a circuit at deep-submicron technology with sub-1V supply voltage, a much tighter threshold voltage control is desired. It can either be achieve by quantum advancement in process control, or by innovative circuit styles that dynamically adjust threshold voltage.

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VI. CONCLUSIONS

As technology scales second order effects become very important to the performance and reliability of a circuit. In this work we studied these effects and how they can influence the performance and reliability of a circuit in different logic styles. We saw that CMOS is the logic style that scales best compared to LEEP or XGATE. We also saw that interconnect capacitance and threshold voltage variation due to process variation can become very important issues in deep submicron that may cause a performance degradation ranging from 20% up to more than 50%. CMOS is again the logic style least affected by these effects. So, our main conclusion is that among the logic styles that we considered, CMOS is the logic style of choice to cope with scalability and reliability issues in deep submicron technologies.

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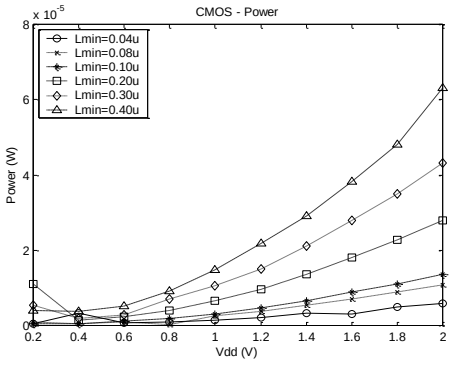

Fig:1

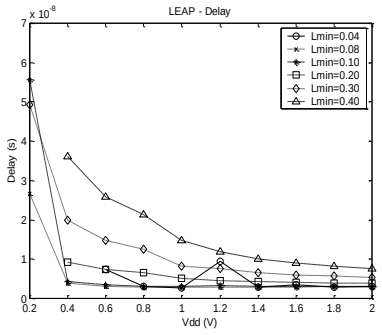

Fig:2

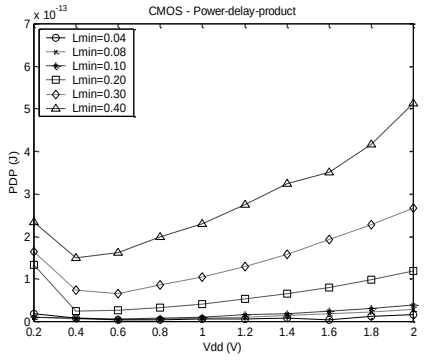

Fig:3

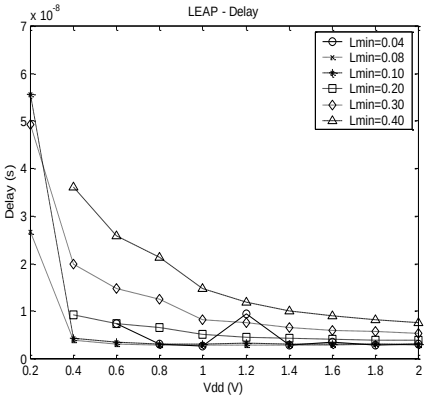

Figure 4: Note that the values of the x axis are half than what they are supposed to be!

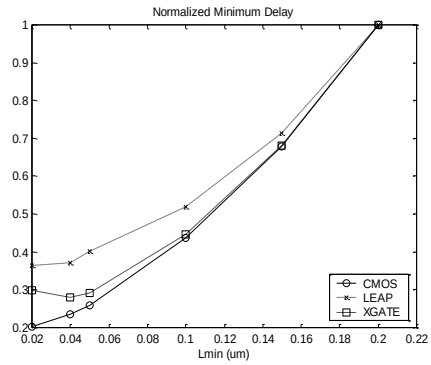

Fig: 5

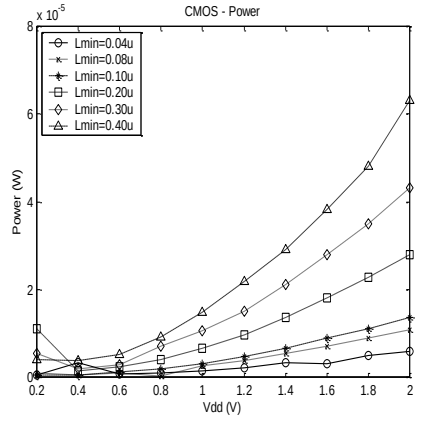

Fig:6

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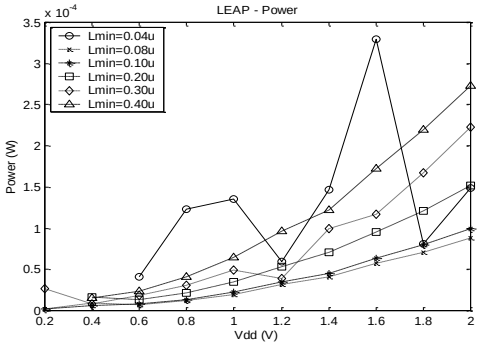


Fig:7

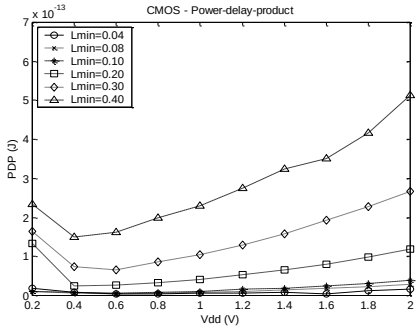


Fig:8

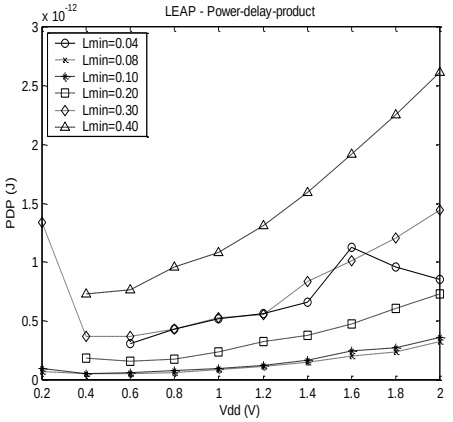


Fig:9

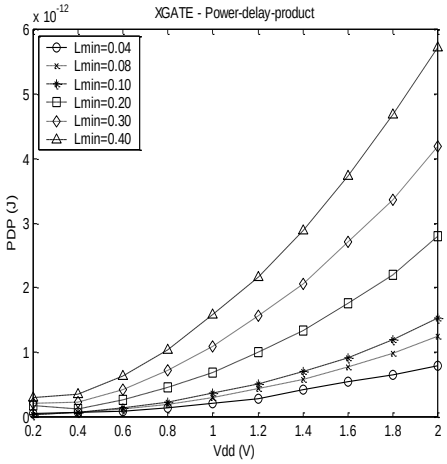
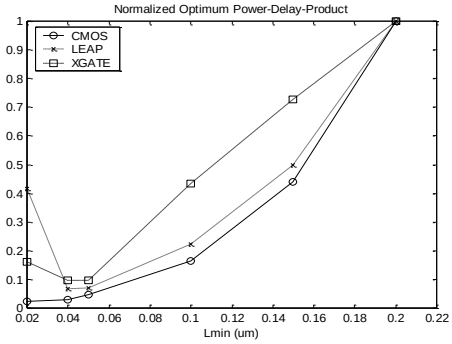


Fig:10



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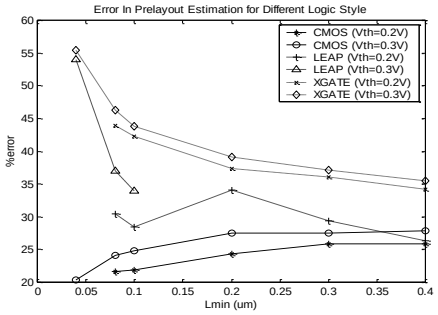

Figure 12: This is the % increase in delay due to interconnect capacitance.

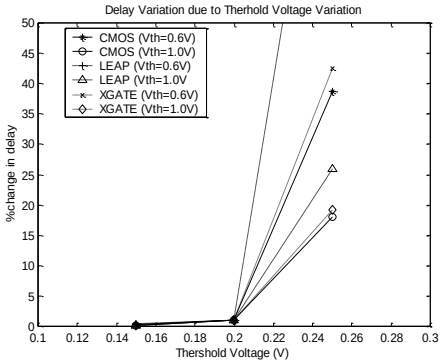

Figure 13: Note that Vdd is 0.6V or 1.0V and not Vth as shown in the parentheses!

BIOGRAPHY

Sachin Tyagi received, B. Tech degree in Electronics and Communication Engineering from ICFAI Institute of Science and Technology, Hyderabad and M.Tech in Electronics and Communication Engineering from MBU, Solan. ***In addition to working as faculty (Assistant Professor) he is pursuing*** research work in Roorkee College of Engineering, Roorkee. His area of interest include VLSI designing, signal processing, MIMO systems and Wireless mobile communications.