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Design and Implementation of SPI with Built-In-Self-Test Capability over SPARTAN 2

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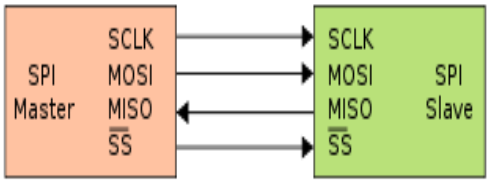
Abstract: The Serial-Peripheral Interface (SPI) protocol is a very essential protocol for connecting between the peripherial devices and microprocessors. As the number of devices in the circuit increased as the advancement of IC technology. So, in order to lessen the product failure self-testability in hardware is demanded a lot in recent times. For the testing of devies we can use self-testability which is called as Built-in-self-test (BIST). BIST is an effective solution to reduce the huge circuit testing cost. This paper represents designing and implementation of SPI protocol with BIST capability over FPGA. An EEPROM and FPGA Spartan 2 are used for the communication testing where the FPGA is master and EEPROM is a Slave. The need of programming for setting up a network with two devices is no longer needed in this proposed system. To accomplish compact, stable and reliable data transmission, the SPI is designed with VHDL language and synthesized on Spartan 2 FPGA.

Keywords: Serial-Peripheral Interface; Embedded built-in-self-test architecture; Verilog HDL; FPGA

I. INTRODUCTION

SERIAL PHERIPERAL INTERFACE BUS:

The spi bus used n a short distance communication, primarly in embedded systems.spi bus is a synchronous serial communication. This interface was developed by motorola. It is used in sensors,liquid crystal displays,secure digital cards.



SPI devices communicate in full duplex mode using a master slave architecture with a single master. The master device originates the frame for reading and writing. Multiple slave devices are supported through selection with individual slave select (SS) lines.

Sometimes SPI is called a four-wire serial bus, contrasting with three-two and one-wire serial buses. The SPI may be accurately described as a synchronous serial interface,[1] but it is different from the synchoronous serial interface (SSI) protocol, which is also a four-wire synchronous serial communication protocol, but employs differiential signalling and provides only a single simplex communication channel.

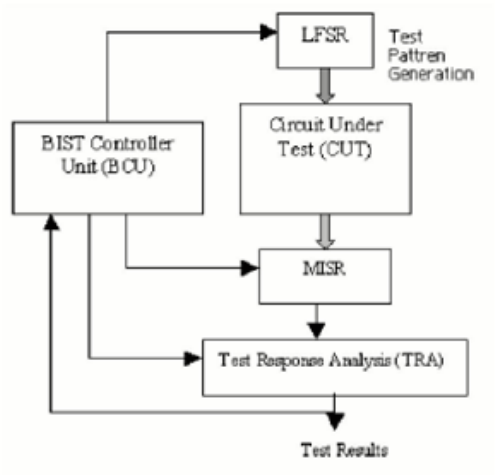
II. BUILT-IN-SELF-TEST-CAPABILITY[BIST]

A Built in-self-test or built in test is a mechanism to permits to test itself engineers meeets the basic requirements

- high reliability
- lower repair cycletimes
- or constraints such as:
- limited technician accessibility
- cost of testing during manufacture

The main purpose[citation needed] of BIST is to reduce the complexity, and thereby decrease the cost and reduce reliance upon external (pattern-programmed) test equipment. BIST reduces cost in two ways:

1) reduces test-cycle duration
2) reduces the complexity of the test/probe setup, by reducing the number of I/O signals that must be driven/examined under tester control.



Bist structure

1) Random Pattern Generators (RPG): Random Pattern Generator (RPG) generates random patterns which can beused for the verification of device like SPI. The RPG is a part of the BIST in the verification of the circuits. Many methods have been proposed for the BIST equipment design [6], [9]. To produce bytes to test the circuit the method of a random pattern generator (RPG) is used.

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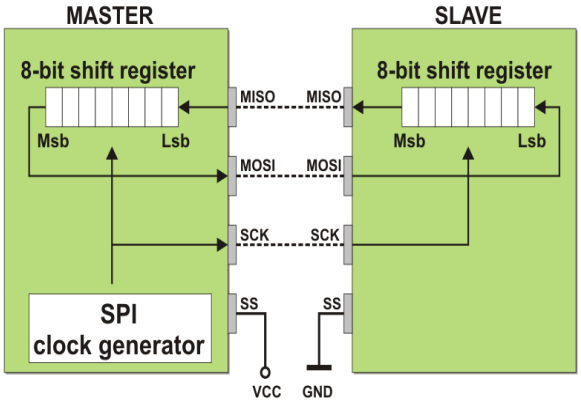
2) Comparator: This is the device which is used to compare two signals i.e received and transmitted bit pattern and then it gives the value of errors.

B. Spi Structure:



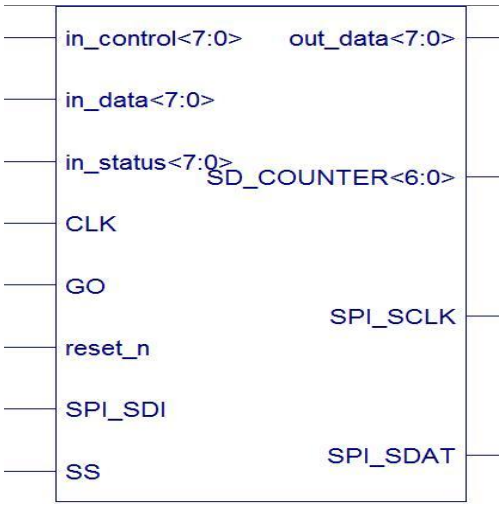
To begin communication, the bus master configures the clock, using a frequency supported by the slave device, typically up to a few MHz. The master then selects the slave device with a logic level 0 on the select line. If a waiting period is required, such as for analog-to-digital conversion, the master must wait for at least that period of time before issuing clock cycles.

During each SPI clock cycle, a full duplex data transmission occurs. The master sends a bit on the MOSI line and the slave reads it, while the slave sends a bit on the MISO line and the master reads it. This sequence is maintained even when only one-directional data transfer is intended.

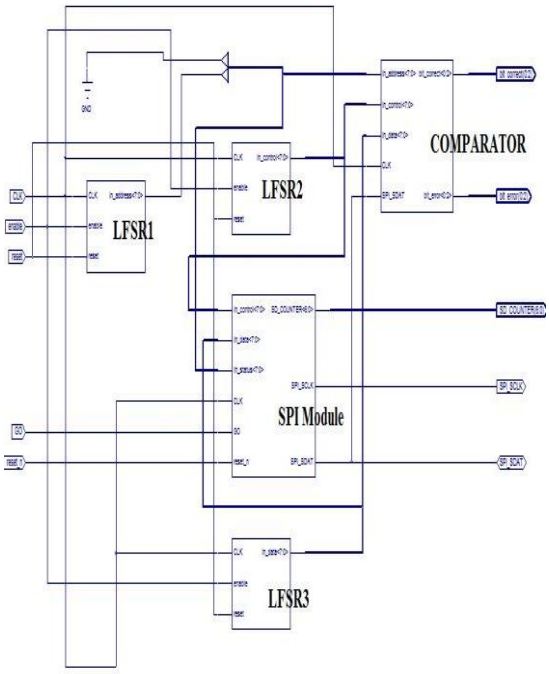
Every slave on the bus that has not been activated using its chip select line must disregard the input clock and MOSI signals, and must not drive MISO. The master must select only one slave at a time.

III. SYSTEM SYNTHE SIZE & IMPLEMENTATION

A. Circuit Schemantic



pin diagram of spi



top level schemantics of spi with bist module

Pin	In/out	description
Clk	In	Clock generator
reset_n	In	Control bit for normal& bist mode
Go	In	Control bit of the spi
in_data	In	Input data byte of the spi
in_control	In	Input control byte of the spi
in_address	In	Input status address of the spi
out_data	out	Output data byte of the master
sd_counter	out	Clock pulse counter for bist mode
spi_sclk	out	Output pin for spi clock
spi_sdata	out	Output data bus
spi_sdi	in	Input data bus

Main spi pin description

B.Simulation Results:

The timing diagrams are achieved from Testbencher (VeriLogger Pro 6.5). The design is tested in the Xilinx FPGA where it also gave the correct output. In the timing diagram, the 8 bits of outputs are converted here into 2-digits Hexadecimal numbers.

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1)Simulation results for BIST module:

a)LFSR 8BIT random pattern generator:

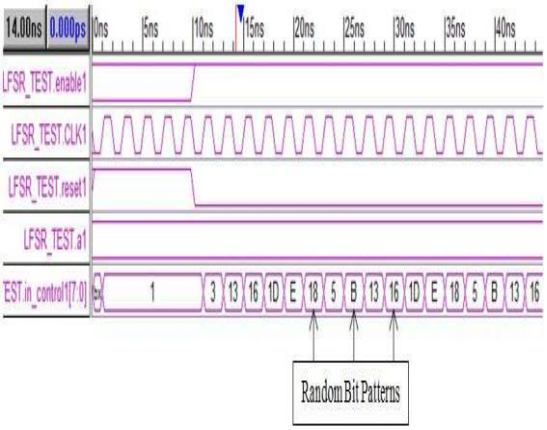
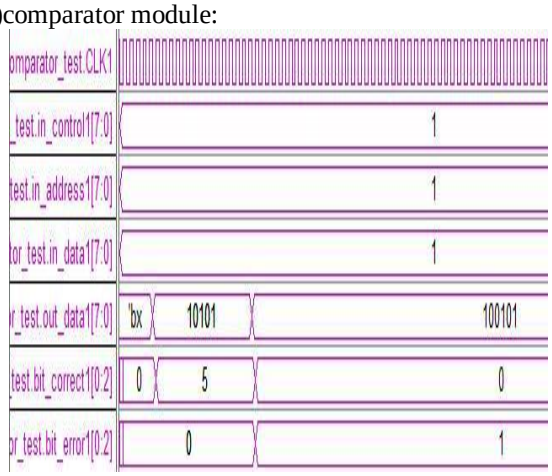


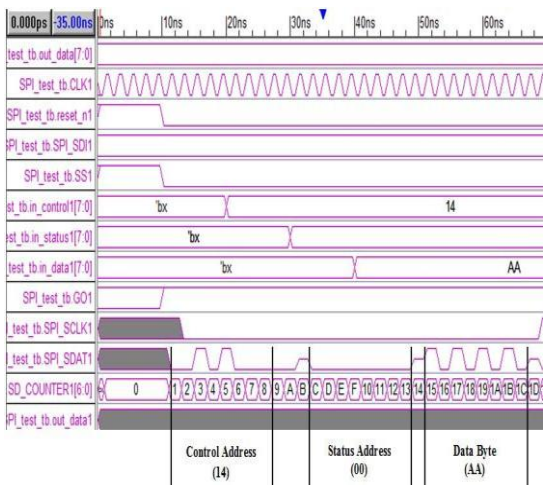
Fig3(a) : Return loss for Design3

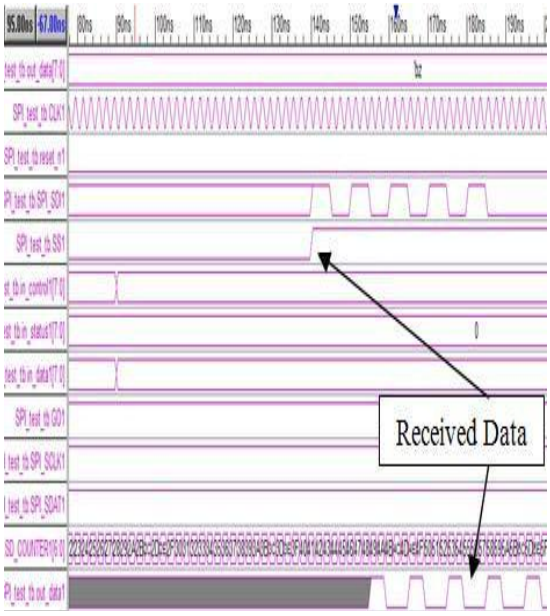
b)comparator module:



2) Simulation Results NORMAL Mode

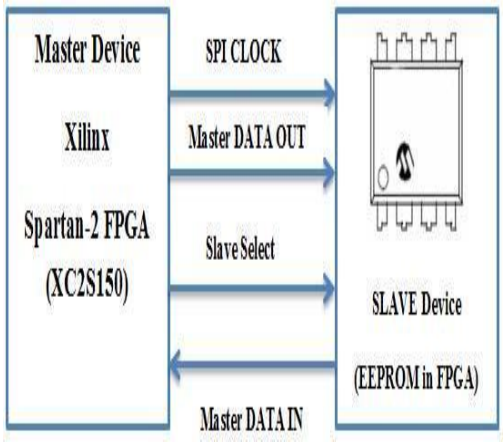
Input type	Binary	Hexadecimal
Control byte	00010100	14
Status address	00000000	00
Data	10101010	AA





C. FPGA Implementation:

Any logical function can be implemented by the Field Programmable Gate Array (FPGA) and it should also be noted that FPGA design is more cost-effective than that of ASIC Design. They have lots of advantages over microcontrollers, such as greater speed, number of I/O ports and performance.



Name	Main SPI Module		SPI with BIST	
	Used Blocks	Percentages (%)	Used Blocks	Percentages (%)
Number of Slices	18 out of 192	9	26 out of 192	13
Number of Slice Flip Flops	19 out of 384 (FDRE:7 FDSE: 12)	4	34 out of 384 (FDR: 3 FDRE:28 FDSE :3)	8
Number of 4 input LUTs	33 out of 384	8	20 out of 384	5
Number of bonded IOBs	24 out of 90 (IBUF :7 OBUF : 16 OBUFT: 1)	26	18 out of 90 (IBUF : 4 OBUF : 14)	20
Number of GCLKs	1 out of 4	25	1 out of 4	25

Table VI. TIMING SUMMARY FOR MAIN SPI MODULE

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Parameters	Main SPI Module	SPI with BIST
	Seconds	Seconds
Minimum period	7.491ns	7.782ns
Minimum input arrival time before clock	6.981ns	4.722ns
Maximum output required time after clock	7.913ns	6.959ns
Maximum delay	7.491ns	7.782ns

V. CONCLUSION

In this paper, an FPGA based implementation of SPI with BIST capability is presented. Here all the modules are designed and simulated with Verilog HDL. Then the system is downloaded in the Xilinx Spartan-2 FPGA (XC2S150). This SPI is much more flexible, speedy, low cost, and stable with respect to conventional one. This SPI control bus architecture can enable the industrial fabrication of chip in a way where only a pressing of one switch can test itself. So that, it would save valuable time and cost of testing circuits significantly.

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