ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

*International Journal of Advanced Research in Computer and Communication Engineering*
*Vol. 4, Issue 5, May 2015*

# Serial Adder using Reversible Gates

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**Abstract:** Reversible logic gates produce zero power dissipation under ideal conditions. Hence these are preferred for low-power design applications such as Quantum computing and Nanotechnology.Adders, Subtractors and Multipliers are basic building blocks of Digital Circuits. This paper proposes design of serial adder using reversible gates. The important reversible gates used for serial adder are Peres gate, Fredkin gate and Feynman gate. The quantum cost of a reversible logic circuit can be minimized by reducing the number of reversible logic gates**.**

**Keywords**: Reversible logic circuits,Quantum computing, Nanotechnology

## I. INTRODUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are constructed using reversible logic circuits. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware result in energy dissipation due to information loss [1]. According to Landauer's principle, the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. In 1973, Bennett, showed that one can avoid KTln2 joules of energy dissipation constructing circuits using reversible logic gates [2].

This paper is organized as follows: Section II gives the brief introduction of the reversible logic gates. Section III describes the design of serial adder using existing reversible gates. Section IV gives the results and discussions of the proposed design. Finally Section V concludes with a scope for further research.

## II. REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits [3, 4].

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.
- Gate levels (GL): This refers to the number of levels in the circuit which are required to realize the given logic functions.

Design and implementation of digital circuits using reversible logic has attracted popularity to gain entry into the future computing technology. In this paper, Serial adder using the existing reversible logic gates is proposed.

### *A. Basic reversible logic gates*

*1) Feynman Gate*

Fig.1 shows a 2*2 Feynman gate [6]. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

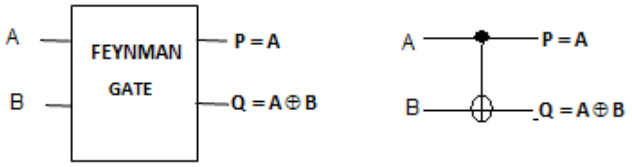


Fig 1: Feynman gate

*2) Double Feynman Gate (F2G)*

Fig.2 shows a 3*3 Double Feynman gate [7]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost of double Feynman gate is 2.

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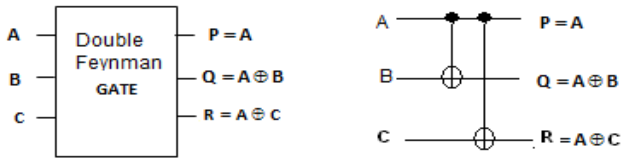


Fig 2: Double Feynman gate

*3) Toffoli Gate*

Fig 3 shows a 3*3 Toffoli gate [3]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

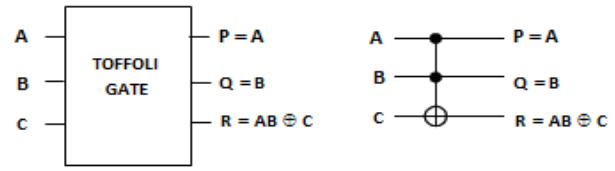


Fig 3: Toffoli gate

*4) Fredkin Gate*

Fig 4 shows a 3*3 Fredkin gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

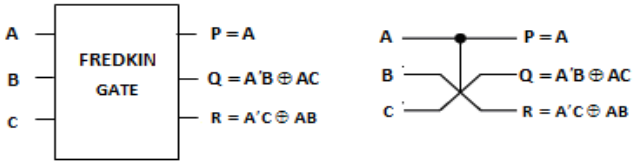


Fig 4: 3*3 Fredkin gate

*5) Peres Gate*

Fig 5 shows a 3*3 Peres gate [10]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

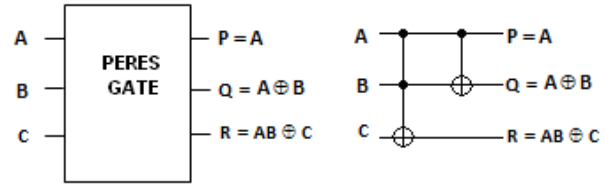


Fig 5: Peres gate

## III. SERIAL ADDER

Here we proposed a 1bit serial adder using Peres gate, Fredkin and Feynman gates.The conventional block diagram is shown in fig6. The reversible serial adder is shown in fig 7. The full adder is designed using 2 peres gates [10] are shown in fig 8. A Flip Flop is a bi-stable element that can be used as a one-bit memory device. Here a simple D Flip-Flop is used to store the carry generated by the Full Adder in the proposed Serial adder circuit. The D-FF is designed using Fredkin and Feynman gates [12] are shown in fig 9. This design reduces the number of existing serial adder circuits [13]. The number of gates used in the proposed serial adder is shown in table 1.

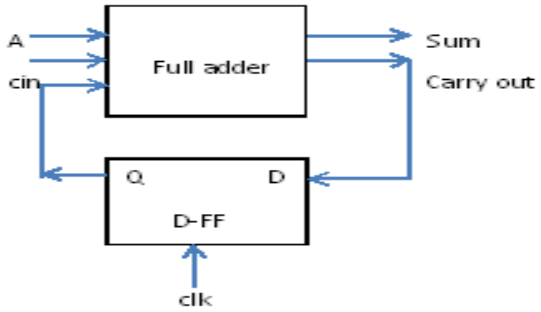


Fig 6: 1-bit serial adder

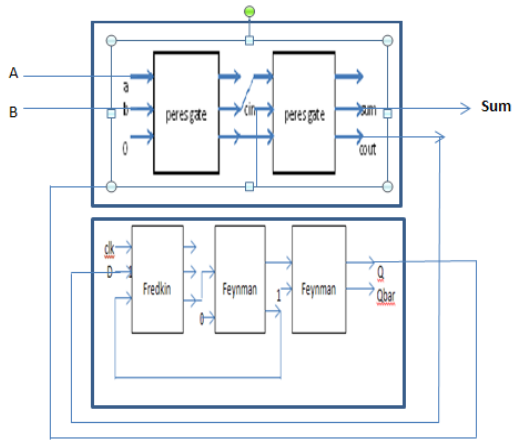


Fig 7:Reversible serial adder

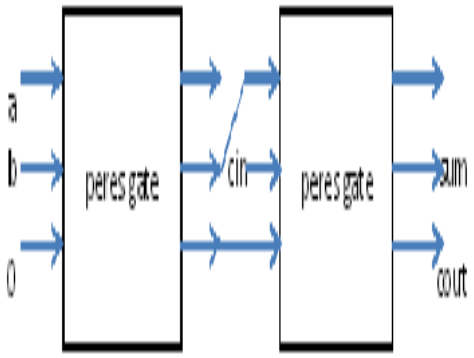


Fig 8: full adder using Peres gate

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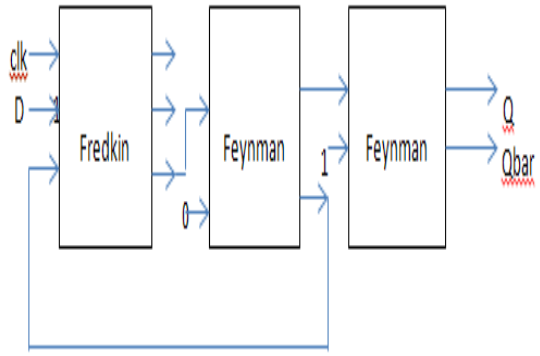


Fig9: D-FF

| Reversible circuit/gate | No. of gates | No of constant inputs | No. of garbage outputs |
|---|---|---|---|
| Full adder | 2 | 1 | 2 |
| D-FF | 3 | 2 | 2 |
| Serial Adder | 5 | 3 | 4 |

Table 1: Utilization summary

## IV. SIMULATION RESULTS

The behavior of the proposed Serial adder, full adder and D-FF are verified using Xilinx ISE. The HDL codes are written in VERILOG HDL and simulated using ISim simulator. The simulated resultsare shown in figs: 10-14.

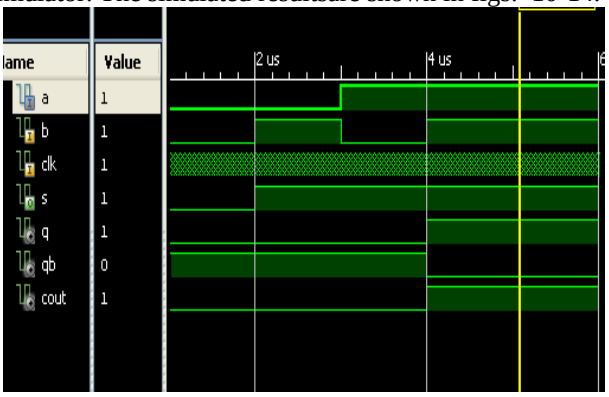


Fig10:simulation result of Serial adder

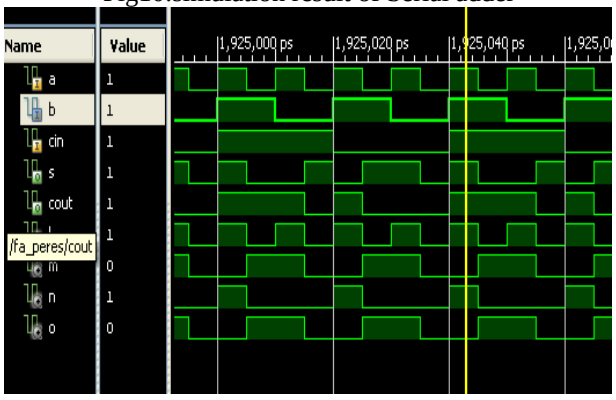


Fig 11: simulation result of full adder

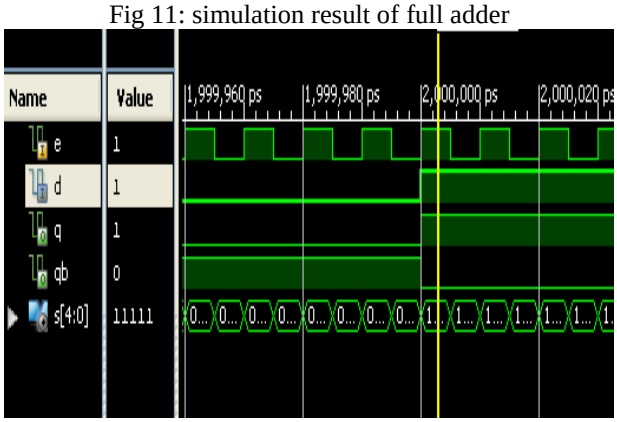


Fig 12: simulation result of D-FF

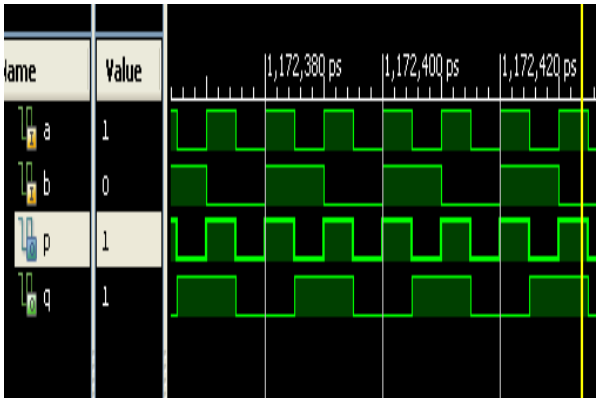


Fig 13:simulation result of Feynman gate

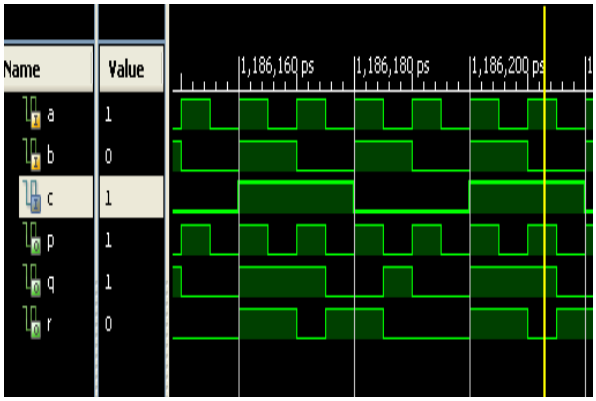


Fig 14: simulation result of Fredkin gate

## V. CONCLUSION

Serial adder is designed using Feynman Gate, Fredkin Gate, and Peres gate. The designed serial adder is highly optimized in terms of number of reversible gates and garbage outputs. Fan out problem is avoided by using Feynman gate for copying the output. The design can be extended to more number of bits. The other work related this is designing Serial adder with accumulator.

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ISSN (Print) 2319-5940

*International Journal of Advanced Research in Computer and Communication Engineering*
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