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Analysis of Threshold Voltage in Nano-Channel Length MOSFETs

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Abstract: This paper presents the simulation results of threshold voltage for Si-based nano channel length MosFet. Simulation results will in between of 180 to 30 nm length of Si-based n-channel MosFet according to constant theory of voltage scaling. The structure of this MosFet is lightly doped drain which reduces to electric field magnitude and effect on short channel at drain region. In this paper, we analyzed the threshold voltage of these type devices and this analysis will provide some applicable limitations inside at ICs and used for basis data at VLSI Circuit design methodology.

Keywords: VLSI, MOSFE, LDD.

1. INTRODUCTION

In tradition feature of MOS devices is easy to be scaled down to lower dimension. Since various devices are consider into the nano-dimension world, it is important to research on the scaling theory applied into various devices. This scaling theory is used for remaining the current-voltage (*I-V*) characteristics of device, with reducing the channel length and width at fast rate of conduction. As reducing the physical size of devices, we can integrate more devices on the chip per the unit area and make its speed faster.

In this paper, we have investigated on the relation between the reduction of the threshold voltage and the scaling theory.[1-3]. If reducing the size of devices, we will encounter unpredictable parasitic effects we do not want to occur in the devices. These effects are referred to short channel effects. Its effects are separated with two effects, electrostatic and electro-dynamic effects. They are the threshold voltage reduction effect occurred by electric field in the electrostatic effects and speed saturation effect by carrier energy increase along to electric field magnitude and reduction of drain reverse bias voltage.

If the drain voltage is constant and the drain current begins to flow at the channel, the gate voltage is defined as the threshold voltage (refered to V_{th}), and as scaling down the devices the V_{th} reduced. As the set of devices become a large unit, the amount of the power dissipation is increased due to large scale of the integration of these devices. Thus we may need the devices with less power dissipation and it is important to develop these devices.

We used Si-based devices owing to lower price and plenty of Si in the semiconductor materials. So we simulated Si-based n-channel MOSFET of all material devices according to the gate lengths from 180 to 30nm with the constant voltage scaling.

The enhanced model device used in this paper is Si-based N-channel MOSFET with 180nm gate length. Scaling down from 180nm gate length to 30nm by step of 10nm is achieved with the constant voltage scaling theory on the basis of the model device. We investigated and studied the operational voltage, that is, the threshold voltage of MOSFET for each gate length.

2. METHODOLOGY: THRESHOLD VOLTAGE OF THE DEVICES

The physical structure of devices applied in this paper is LDD(Lightly Doped Drain) structure, which has lower doped drain. As a matter of fabrication a lower doped region in source region sets on the beginning point of the channel. Recently, this LDD structure is used as the industrial and custom standard of fabrication due to the reduced short channel effects such as the punch-through effect of MOSFET.[2]

As becoming devices of a smaller size, these have high electric field and increasing hot carrier. Thus, this structure with not n^+ doping butn$^-$ reduces punch-through effect in the junction of source and drain region.

Generally, threshold voltage equation in long channel is as follows.

$$V_{th} = V_{FB} + 2|\phi_F| + \frac{|Q_d|}{C_{ox}} \quad (1)$$

Here, V_{FB} isthe flat band voltage, ϕ_F is the fermi potential, Q_d is the charge in the depletion region, and C_{ox} is the oxide capacitance. Since the Eq. (1) is presented on the one-dimensional analysis without accounting of the length of the depletion layers, it has to be corrected as follows.

$$V_{th} = V_{FB} + 2|\phi_F| + V_S + \frac{f \cdot Q_d}{C_{ox}}$$

$$= V_{FB} + 2|\phi_F| + V_S + \frac{f}{Cox}\sqrt{2\varepsilon_s qNa(2|\phi_F| + V_S - V_B)} \quad (2)$$

Here, V_S, V_B, ε_S, q, and N_a are the source voltage, the substrate voltage, the permittivity of the semiconductor, the charge of an electron, and the concentration of the acceptors, respectively. f is as follows.

$$f = \frac{Q_{d1}}{Q_d} = 1 - \frac{r_j}{L}\left(\sqrt{\frac{1 + 2 \cdot x_{d\max}}{r_j}} - 1\right) \quad (3)$$

Here, Q_{d1}, r_j, $x_{d\max}$ are the charge induced to surface inversion in the gate region, radius of junction region, and the width of the depletion layer. The Eq. (3) is known to be suitable to MOSFET with the $1\mu m$ gate length.

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But in this paper, we simulated with the MOSFET under the $1\mu m$ gate length, that is, in the submicron domain. Thus, we try to induce the threshold voltage equation applicable under the $1\mu m$ gate length.

3. SIMULATIONS AND DISCUSSION

As mentioned before, we simulated using the LDD structure of MOSFET, this structure is shown in Fig. 1 and simultaneously this figure shows the doping concentration of 180nm gate length device and the mesh structure. In this mesh structure, cross points are used in calculation of current, voltage, impact ionization, and so on for the whole region.

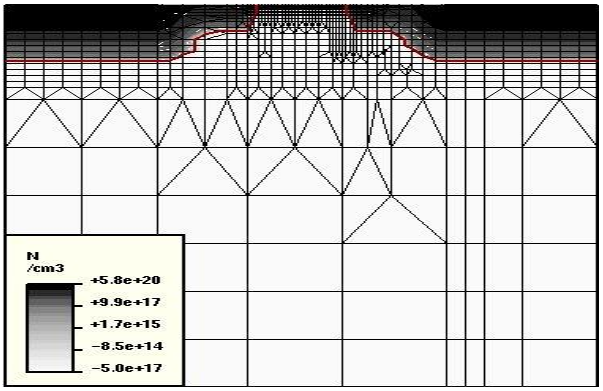

Fig 1. Mesh structure and doping concentration in MOSFET with 180nm gate length.

We scaled the MOSFET on the basis of 180nm gate length device as to the constant field scaling theory, and simulated its threshold voltage in ISE-TCAD, which is a linux-based semiconductor simulating program. The doping concentrations of each region and gate oxide thickness for each gate length are shown in the Table 1.

And the simulation has undergone in two sides. One is the simulation applied the constant scaling theory and the other is the simulation applied not the scaling theory but the gate length reduction. The doping condition of second simulation is the same as that of 180nm gate length.

The doping method of the each region is defined as the Gaussian function. The doping method of the source and drain region is applied with the lateral factor of a half of its region diffusion.

Table 1. Maximum and minimum concentrations of each region and gate oxide thickness in LDD MOSFET.

L_g (nm)	Source & Drain region (cm^{-3})		LDD region (cm^{-3})	Substrate region (cm^{-3})	T_{ox} (nm)
180	MAX	5.00×10^{20}	8.00×10^{19}	3.00×10^{17}	4.00
	MIN	3.00×10^{17}	5.00×10^{17}		
170	MAX	5.61×10^{20}	8.97×10^{19}	3.36×10^{17}	3.78
	MIN	3.36×10^{17}	5.61×10^{17}		
160	MAX	6.33×10^{20}	1.01×10^{20}	3.80×10^{17}	3.56
	MIN	3.80×10^{17}	6.33×10^{17}		
150	MAX	7.20×10^{20}	1.15×10^{20}	4.32×10^{17}	3.33
	MIN	4.32×10^{17}	7.20×10^{17}		
140	MAX	8.27×10^{20}	1.32×10^{20}	4.96×10^{17}	3.11
	MIN	4.96×10^{17}	8.27×10^{17}		
130	MAX	9.59×10^{20}	1.53×10^{20}	5.75×10^{17}	2.89
	MIN	5.75×10^{17}	7.58×10^{17}		
120	MAX	1.13×10^{21}	1.80×10^{20}	6.75×10^{17}	2.67
	MIN	6.75×10^{17}	1.13×10^{18}		
110	MAX	1.34×10^{21}	2.14×10^{20}	8.03×10^{17}	2.44
	MIN	8.03×10^{17}	1.34×10^{18}		
100	MAX	1.62×10^{21}	2.59×10^{20}	9.72×10^{17}	2.22
	MIN	9.72×10^{17}	1.62×10^{18}		
90	MAX	2.00×10^{21}	3.20×10^{20}	1.20×10^{18}	2.00
	MIN	1.20×10^{18}	2.00×10^{18}		
80	MAX	2.53×10^{21}	4.05×10^{20}	1.52×10^{18}	1.78
	MIN	1.52×10^{18}	2.53×10^{18}		
70	MAX	3.31×10^{21}	5.29×10^{20}	1.98×10^{18}	1.56
	MIN	1.98×10^{18}	3.31×10^{18}		
60	MAX	4.50×10^{21}	7.20×10^{20}	2.70×10^{18}	1.33
	MIN	2.70×10^{18}	4.50×10^{18}		
50	MAX	6.48×10^{21}	1.04×10^{21}	3.89×10^{18}	1.11
	MIN	3.89×10^{18}	6.48×10^{18}		
40	MAX	1.01×10^{22}	1.62×10^{21}	6.08×10^{18}	0.89
	MIN	6.08×10^{18}	1.01×10^{19}		
30	MAX	1.25×10^{22}	2.88×10^{21}	1.08×10^{18}	0.67
	MIN	7.50×10^{18}	1.80×10^{19}		

Several extraction techniques can be used to compute the threshold voltage.[4] The common methods are; 1) the regression method which consists in determining the intersection point between the V_{gs} axis and the tangent to the $I_{ds}(V_{gs})$ curve defined at the maximum slope point, 2) the method extracting V_{gs} at $I_{ds} = 0.1\mu A/m$ (typical current level) and 3) extracting the intersection between the two tangents to the $I_{ds}(V_{gs})$ curve in log scale, respectively defined at the maximum and minimum slope points.

In this paper, two methods, as mentioned are used. Second method is used in finding the threshold voltages accounting of DIBL effect, and first method finding ones accounting of VDQC model(is referenced to Van Dort Quantum Correction model)[5] and body effect.

1. The deviation of V_{th} taking account of DIBL effect

Figure 2 shows V_{th} with and without DIBL effect when the drain voltage is 0.1V, 1.0V and 2.0V under the condition of the constant voltage scaling. As gate length is reducing, we know V_{th} is higher and is affected with drain voltage. But the deviation of the curve accounting of the DIBL effect is in the range of maximum0.03V.

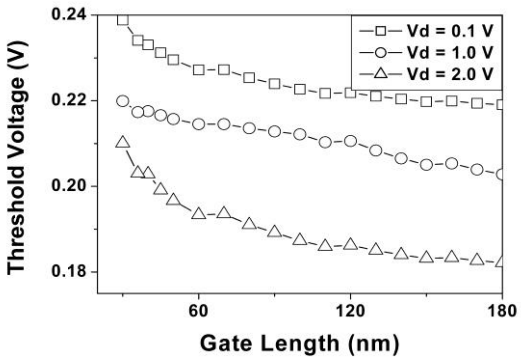

Fig. 2. Deviation of V_{th} taking account of DIBL effect.

Fig. 3 shows the V_{th} simulation graphs with and without DIBL effect under the condition of the gate length reduction. This result shows that as the channel length

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reducing DIBL effect remarkably affected the V_{th}while as the drain voltage it do not affected largely. But we investigated the drain voltage effects increase under the about $0.5\mu m$ gate length.

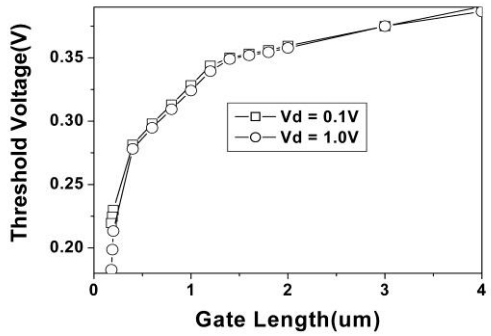

Fig. 3. Deviation of V_{th} taking account of DIBL effect with reducing only the gate length.

2. The deviation of V_{th} taking account of VDQC model

The scaling procedure for modern submicron devices requires both thinner oxide and higher level of channel doping. But the combination of thin oxide and high doping level results in transverse electric fields at the silicon/oxide interface, which are sufficiently large to quantize electron motion in the direction perpendicular to the interface. Taken account of this phenomenology-cal effect the van Dort model can be considered as an effective band gap widening because of confinement of minority carriers in the inversion layer. The value of this widening is given by the following expression

$$\Delta E_g = \frac{13}{9}\cdot k_{fit}\cdot F(\vec{d})\cdot\left(\frac{\varepsilon\cdot\varepsilon_0}{4kT}\right)^{1/3}\cdot\left|\left(E_n - E_{crit}\right)\right|^{2/3} \quad (4)$$

where E_n is the electric field normal to the Si/SiO_2 interface, k_{fit} and E_{crit} are fitting parameters. The function $F(\vec{d})$ is defined as

$$F(\vec{d}) = \frac{2\exp(-a^2(\vec{r}))}{1+\exp(-2a^2(\vec{r}))} \quad (5)$$

where $a(\vec{r}) = l(\vec{r})/\lambda_{ref}$ and $l(\vec{r})$ is a distance from the point $\vec{r}$ to the interface. The parameter λ_{ref} effectively defines the region near the interface, where quantum correction takes place. Depending on the sign of the normal electric field, band gap widening is applied to the conduction band or to the valence band. Let us suppose that E_n is positive if the electric field points outside the semiconductor. Then the band gap widening is applied to the holes (valence band correction) if $E_n > 0$, or to the electrons (conduction band correction) if $E_n < 0$.[6-9]

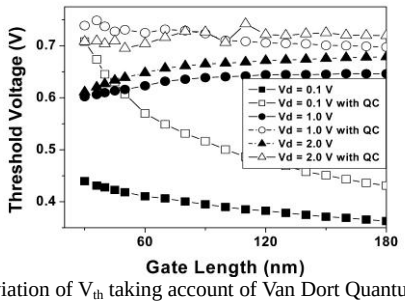

Fig. 4. Deviation of V_{th} taking account of Van Dort Quantum Correction model and do not taking.

Devices was simulated with computing method applied this QC model with scaling. As shown in the Fig. 4, the results applied this model is a little different with one not applied. That is, when the gate voltage is 1V or 2V, we investigated, the difference between V_{th}'sextracting results applied this model and those not applied is negligible, while the difference of them is not trivial when the gate voltage is 0.1V. As shown in Fig. 4(two graphs when $V_d = 0.1V$), we know V_{th} values extracted by the existing calculation method may be estimated wrong values as compared with experimental values measured in the submicron devices.

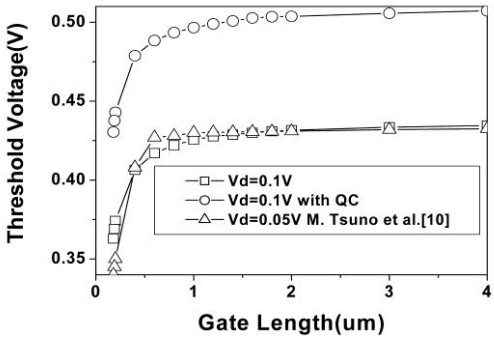

Fig. 5. Deviation of V_{th} takingaccount of Van Dort Quantum correction model and not accounting.

In the Fig. 5, the results, included QC model and not, are illustrated for the gate length. The trace of the bold line is similar to the result of previous scientific paper presented [10-11]. We knowV_{th} is constant in the micron gate length but in the submicron region decreases very seriously as to the channel length reduction. The dashed line in Fig. 5 shows the simulation results applied QC model. This line is 0.07V higher than the graph included QC model.

3. The deviation of V_{th} taking account of the substrate voltage

Fig. 6 shows V_{th} extracting results taking account of the body effect when the drain voltage is 0.1V in the constant scaling theory. As shown in Fig. 6, V_{th} values are about 0.2V higher in $V_{sub} = -2V$ than in $V_{sub} = 0V$. The deviation of V_{th} as to the change of the channel length is very low and the deviation as to the substrate voltage is bigger than one to channel length.

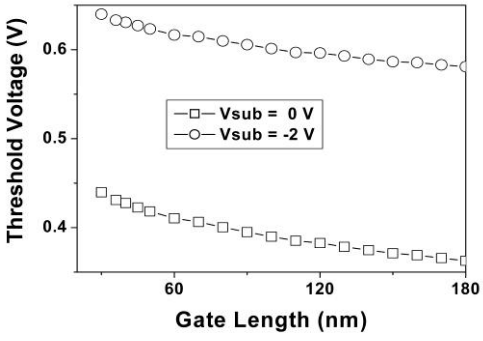

Fig. 6. Deviation of V_{th} as to the substrate voltage.

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Fig. 7 is presented the results of V_{th} extracting as to only the gate length reduction. As shown in this figure, we know the variation of V_{th} as to the substrate voltage affects larger than other effects simulated in this paper. Its trend is resembled in that of Fig. 5.

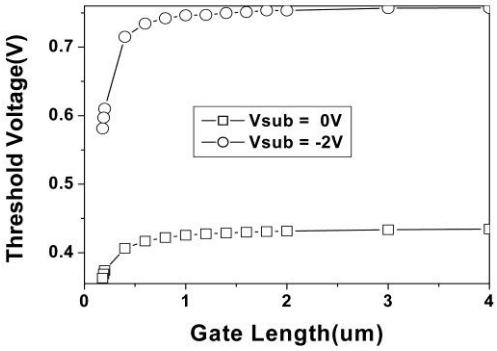

Fig. 7. Deviation of V_{th} as to the substrate voltage.

4. CONCLUSIONS

In strong inversion, one of the most important MOS parameter is the threshold voltage, which determines especially the gate voltage limit over which the device will be turned on. In the design of devices, this condition may be able to be inserted if the V_{th} is changed. In this paper, we inspected the deviation of the V_{th} of only nano-channel MOSFET. The results simulated in this paper show the deviation of the V_{th} for the physical size of the devices is not high. The V_{th} variation applied the DIBL effect, the VDQC model and the body effect is about 0.03V, 0.28V and 0.08V, respectively. Thus we know VDQC model is most affected in V_{th} variation, and the V_{th} variation as to DIBL effect is not very high.

There are the narrow width effect, the DIBL effect, the subthreshold characteristics, the electron-hole multiplication effect and so on in the device features with short channel. The characteristics investigated in this paper is a very small part of those effects. So we will try to study and investigate other characteristics of MOSFET with short channel. Finally, the simulated results in this paper, we think, can be used for the basis data of other ICs or VLSI fabrication.

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BIOGRAPHIES

Sachin Tyagi received a Bachelor of Technology degree in Electronics and Communication Engineering from ICFAI Institute of Science and Technology, ICFAI University, Dehradun and Master of Technology in Electronics and Communication Engineering from MBU, Solan. In addition to working as faculty (Assistant Professor) he is pursuing research work in Roorkee College of Engineering, Roorkee. His areas of interest include VLSI Technology and Circuit designing, Signal Processing, MIMO systems and Wireless mobile communication.

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