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A Sepic Converter with Linear Transformer and Ripple Free Output for Wide Range Input Applications

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Abstract: A linear transformer based SEPIC converter with ripple free output is proposed in this paper. The topology utilizes a linear transformer in order to obtain optimized magnetics The conventional power factor correction(PFC) single ended primary inductor converter(SEPIC) topologies proposed so far have achieved low conduction losses and reduced input ripple current but they have failed to achieve optimized magnetics.. In addition input current ripple and the voltage stresses across the switches is reduced by utilizing a clamping capacitor across the switch. A detailed analysis is carried out on MATLAB/SIMULINK platform and the various results are tabulated and analyzed. The hardware prototype model of proposed topology is designed and implemented for the input voltage of 24/55 v DC for which the expected output voltage 150v DC with the circuit efficiency of 94% is achieved**.**

Keywords: power electronics, power factor correction (PFC), bridgeless converter, single ended primary inductor converter (SEPIC)

I. INTRODUCTION

There has been an increasing demand for high power factor and low total harmonic distortion (THD) in the current drawn from the utility. With the precise requirement of the power quality, power factor correction significant efforts have been made in the development of PFC converters. These kinds of converters generally have full bridge diode rectifier on an input side so the conduction losses occur at the input side where the full bridge diode is present. In order to overcome this problem the full bridge diode is eliminated and bridgeless converters are introduced. The boost converter topology has been widely used as a PFC converter because of its simplicity and high power capability. It can be used with the universal input voltage range. The boost converter always uses three semiconductor voltage drops in the current flow path. To increase the converter efficiency bridgeless boos rectifiers were introduced. The conduction losses are reduced by reducing the number of semiconductor devices that conduct current from the source to the load. However, the output diode operated in high voltage has severe reverse recovery problems due to high diode forward current and high output voltage. As the switching frequency increases,, the large reverse recovery currents of the output diodes effect the switches in the form of additional turn on losses and also produce electromagnetic interference (EMI) noises. The major disadvantage of using boost converter is that its output voltage should be higher than its peak input voltage.

Relatively low output voltage of PFC converter is required in many applications such as switched mode power supplies.
Therefore in order to overcome the disadvantages of the PFC boost converter, PFC buck converters are introduced. These converters are more suitable for many applications due to their low output voltage range. Moreover buck converters perform better at light load owing to a wide range of choices of lower voltage rated semiconductor devices and reduction of losses and sizes of isolation transformers. However, since the input current of the PFC buck converter has dead angles during the time intervals when the input voltage, there is a strong tradeoff between the power factor and output voltage selection.
Therefore in order to overcome the disadvantage of the PFC boost and buck converter, SEPIC converters is proposed in this paper. It is used to obtain high power factor regardless of its output voltage which can be stepped down or up accordingly. SEPIC converters have been adopted for many applications such as high power factor correction, photovoltaic system and LED lightening. However it has several drawbacks such as

- High voltage stresses of power semiconductor devices
- Low efficiency due to hard switching operation of the power switches
- Electromagnetic interference noises are significant in high-frequency operation
- A bulk inductor should be used to minimize the current ripple.

In order to overcome the above mentioned drawbacks a “Linear transformer based SEPIC converter with ripple free output for variable input application” is developed in this project. It mainly consists of a linear transformer which will overcome the disadvantage of using three magnetic components in order to reduce the current ripple and the high voltage stresses of the switches can be reduced by using a clamping capacitor across the switch.

Therefore due to the reduced ripple and voltage stresses of the power semiconductor devices the efficiency is improved.

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II. PROPOSED TOPOLOGY

The proposed linear transformer based SEPIC converter topology consists of a linear transformer; it is another excellent technique applied in high voltage step up applications by adjusting the turns ratio of the transformer. The capacitor C_2 is added across the switch to reduce the switching losses. Diodes D_1 and D_2 are the input rectifiers and operate like a conventional SEPIC PFC converter. The other components C_1 ,L_1 ,D_o and C_o are similar to those of conventional SEPIC converter. It is assumed that the converter operates in discontinuous conduction mode (DCM). The converter operation is analyzed during one switching period in the positive half line cycle of the input voltage. The circuit arrangement is shown in fig 1.

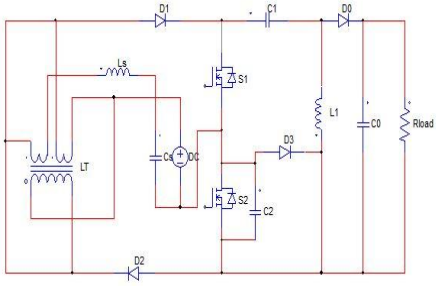


Figure 1: A linear transformer based SEPIC converter

The advantages of using this topology are-

1) Closest to UPF is achieved.
2) Conversion efficiency is better compared to others.
3) Low voltage stress across the main switch is achieved by using effective clamping technique.
4) The ripple is further reduced due to ZVS operation

The proposed linear transformer based SEPIC converter operates in three modes, in one switching period. Before t_o, the switch $S_1$and diode D_o are turned off and the switch S_2 is conducting. The theoretical waveform of the proposed converter is shown in fig 2.

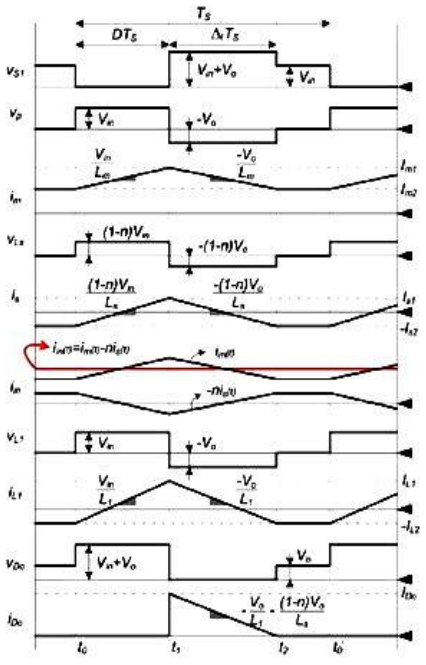


Fig. 2. Key waveforms of the proposed converter

III. OPERATION OF A PROPOSED CIRCUIT

A. Region of operation

The converter operates in three modes namely,

1) Mode 1(t_0, t_1):

During this mode the switch S_1 is turned ON, the tertiary winding of the transformer is charged and the current is induced in the primary and the secondary winding of the transformer.

Therefore the diode D_1 is forward biased and the capacitor C_1 and the inductor L_1 is charged. Hence the inductor L_1 is fully charged. The capacitor C_o supplies to the load. The current i_s increases from its minimum value $-I_{s2}$ linearly as follows.

$$i_s(t) = -I_{s2} + \frac{(1-n)V_{in}}{L_s}(t - t_0) \quad \text{..... (1)}$$

2) Mode 2(t_1, t_2):

During this mode the switch S_1 is turned OFF and the switch S_2 is turned on. The inductor L_1 which was charged previously in mode 1 will now start to discharge thus forward biasing the diode D_o.

The capacitor C_o is fully charged and supplies the load. The capacitor C_2 and diode D_3 are connected across the switch S_2 in order to reduce the stress across the switch S_2 by performing ZVS operation.

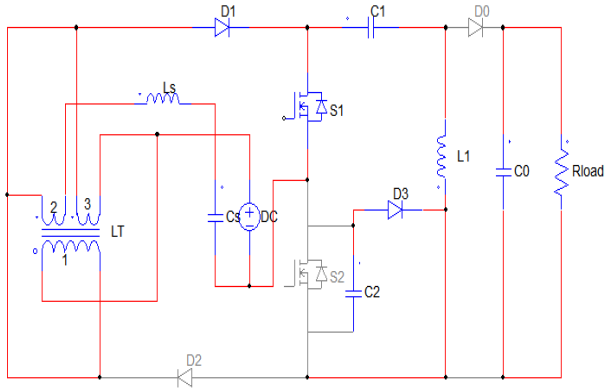
The capacitor C_2 also opposes the change in voltage. Therefore a ripple free current is fed into the inductor L_1. The current i_s decreases from its maximum value linearly as follows

$$i_s(t) = I_{s1} - \frac{(1-n)V_{in}}{L_s}(t - t_1) \quad \text{.....(2)}$$

3) Mode 3 (t_2, t_0'):

This is a transition mode where switch S_2 is about to turn off and switch S_1 to turn on. By the end of this mode the switch S_2 will be turned off and switch S_1 will be turned on. The output capacitor C_o supplies to the load.

In all the modes of operation the diode D_2 is reverse biased in order to ensure a continuous flow of current into the linear transformer and also to avoid the reverse flow of current into the switch S_2 which may cause damage to the switch



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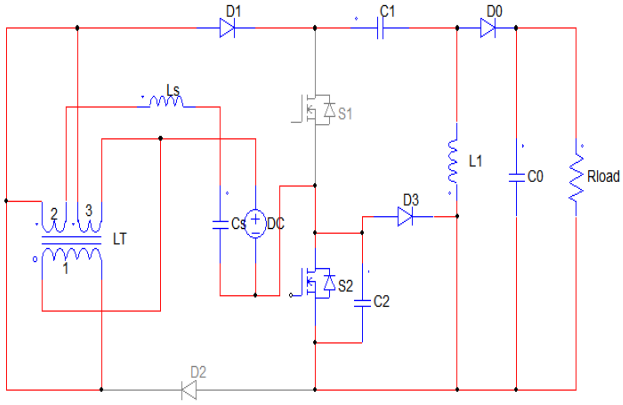

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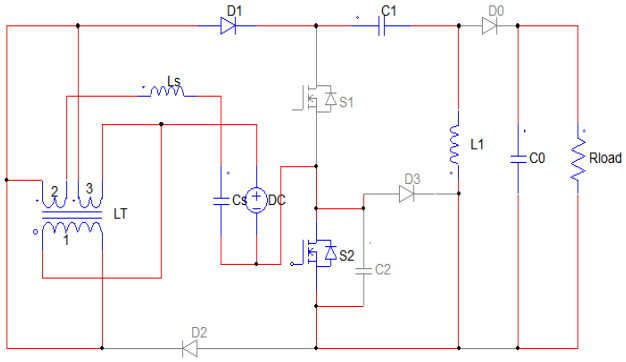

3(c)

Figure 3: shows the mode of operation of proposed circuit
(a) Mode1, (b) Mode 2, (c) Mode 3

VI. DESIGN PROCEDURE

A. Design Specification:

Design specifications of the proposed converter are as follows:

1) Main voltage V_{in} = 55V_{dc};
2) DC output voltage: V_o = 150V
3) Maximum output power: P_{out} = 250W
4) Switching frequency: f_{SW} = 100KHz

B. Rating of switching devices

In this proposed circuit, the voltage stresses of all the switching devices are equal to the sum of the maximum input voltage and output voltage as follows

$$V_{D,max} = V_{SW,max} = V_{in,peak} + V_o \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

The current stresses across the diode is given as follows

$$I_{D,max} = I_{D1} = I_{D2} = \left[\frac{2-n}{l_s}\right]\sqrt{\frac{4P_o l_s}{f_{sw}}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

C. Clamping capacitor

As the switches conduct, they develop voltage stresses across them, thus a clamping capacitor is used across the main switch in order to reduce the stress across the switch and is given as follows.

$$C_2 = \frac{D}{R\left(\frac{\Delta V_o}{V_o}\right)f} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

The voltage across the switch S_1 is same as that of the diode voltage but the voltage across the S_2 should be less when compared switch S_1 because of the clamping effect, the voltage stress across the switch S_1 is reduced

D .Conditions to operate in DCM

In order to guarantee that the proposed converter operate in DCM mode the inequality of $\Delta_1 < 1 - D$ must be satisfied. The voltage gain can be extended greatly without an extreme duty cycle as turns ratio of the transformer increase which makes the converter suitable for high step up and high power conversion. Duty cycle is obtained as following inequality.

$$V_o = \frac{1}{(1-D)} V_{in} \quad \ldots\ldots\ldots\ldots\ldots\ldots (6)$$

E. Average inductor current

The average current flowing through the inductor is given as follows

$$I_{L1} = \frac{V_O^2}{V_{in} R} \quad \ldots\ldots\ldots\ldots\ldots\ldots (7)$$

$$\Delta i_{L1} = \frac{V_{in} D}{L_1 f} \quad \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

F. Output capacitor

As the output ripple voltage is two times the input line frequency the output capacitor C_o should be large enough to minimize the output voltage ripple ΔV_o. Therefore, C_o can be obtained from the following equation

$$C_o = \frac{P_O}{4 f V_O \Delta V_o} \quad \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

IV. SIMULATION

A. Circuit Arrangement:

The main aim of this project is to improve the voltage gain and efficiency and to reduce the ripple by using a linear transformer. Active clamp technique is adopted to reduce the voltage stresses. The simulation work is done in MATALB SIMULINK. The output voltage of 150v is obtained and simulation diagram is shown in fig 4

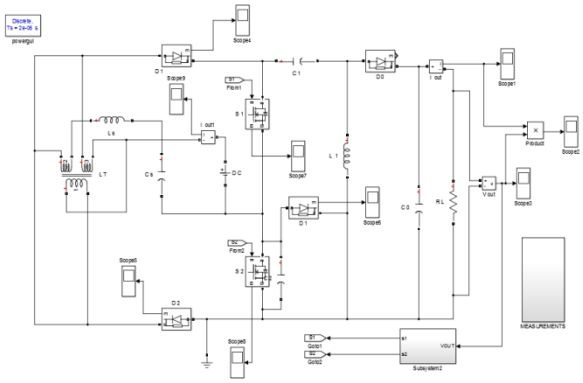

Figure 4: Circuit Arrangement in MATLAB Simulation Package

1. The fig 5 shows the proposed linear transformer based SEPIC converter for ripple free input current for a wide input range.
2. A clamping capacitor and a diode are used a cross switch S_2 for ZVS operation in order to reduce the stress
3. The value of output capacitor is reduced further so that the hardware is no more bulky
4. The waveforms of output voltage, output current and output power are shown below

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C. Simulation Results:

The figure 5 shows the simulation results of input voltage, output current, output power for the proposed linear transformer based SEPIC converter respectively as shown below.

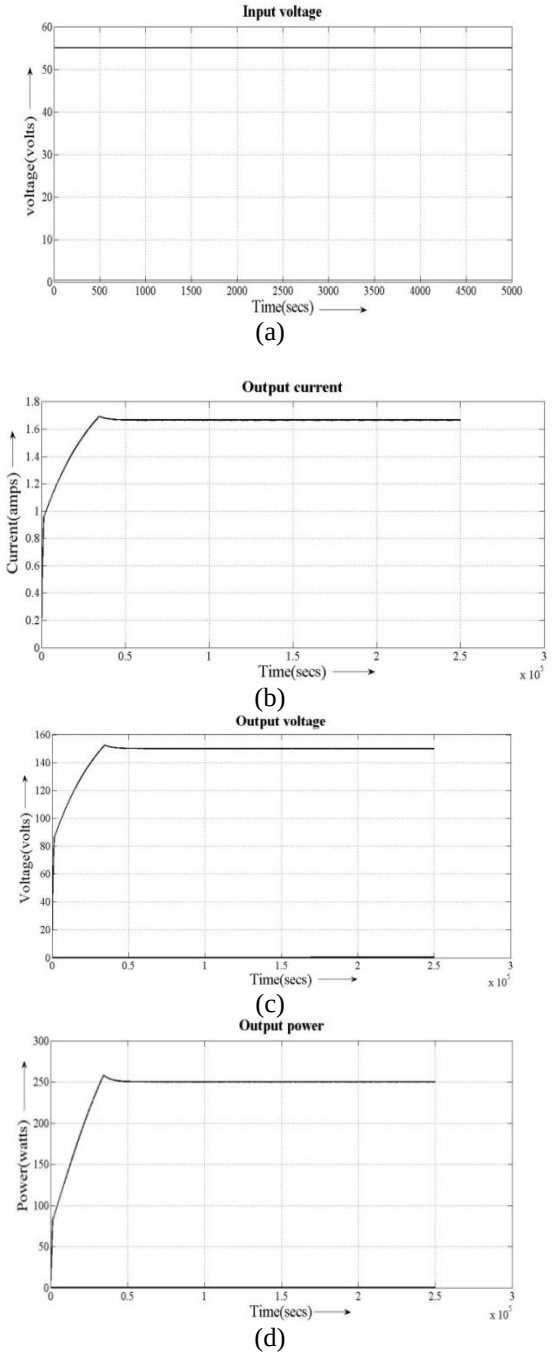

Fig 5: waveform of output voltage and output current of proposed converter.

(a) Waveform for 55V input (b) Waveform for output current (c) Waveform for 150V output voltage (d) Waveform for 250W output power

Figure 5(a) shows the simulation results obtained for a input voltage of 55v.And the figure 5(b) shows the simulation results for output current of 1.6amps.And figure 5(c) shows the simulation results for output voltage 150V and figure 5(d) shows the simulation results for output power of 250W which is greater than the conventional converter respectively

V. MEASUREMENT RESULTS

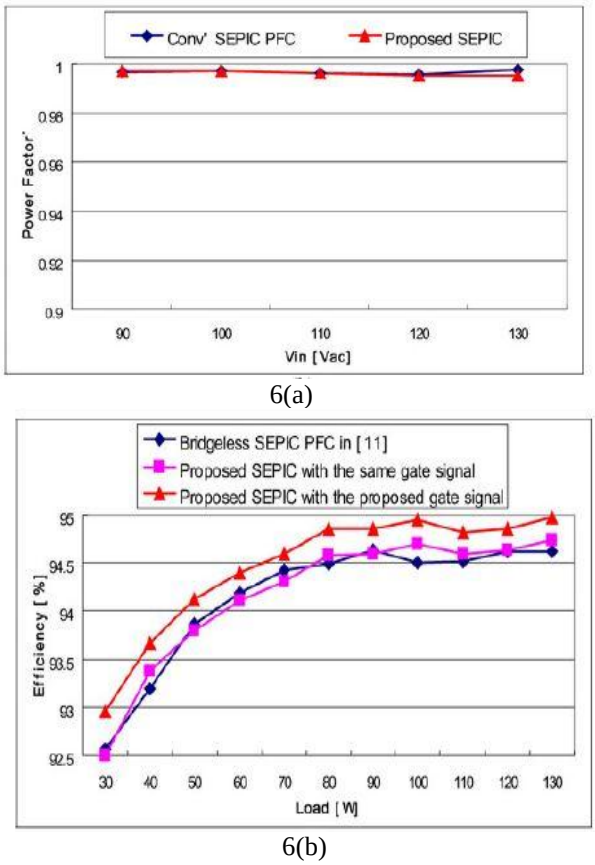

Figure 6: Shows the measurement results of proposed circuit (a) Power Factor, (b) Efficiency

In fig 6 (a), the power factor is measured more than 0.995 in the converter as shown in Fig.6(a). In addition, Fig.6(b) shows the measured efficiency of the bridgeless SEPIC PFC in and the proposed converter. When the same gate signals in are applied to the switches, the efficiency of the proposed converter is similar to that of the conventional converter. When the proposed gate signals a are applied to the switches, the efficiency is improved compared with the conventional converter

VI. CONCLUSION

A linear transformer based SEPIC with ripple free output for variable input application is presented in this project.ZVS soft switching is achieved for the switches during the whole switching transition. The linear transformer reduces the reverse recovery losses. By employing linear transformer the voltage gain can be greatly extended and the switch voltage stresses are far lower than the output voltage and high performance MOSFETS available to reduce the conduction losses in high input application. Finally the converter is designed to show the converter performance and experimental result. The advantage of the proposed topology

It produces considerably more current and voltage. High weighted efficiency than conventional converter. Wide input voltage range. In future more advanced control techniques can be used to improve the performance and efficiency of the system.

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