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Design and Implementation of UART

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Abstract: The proposed paper illustrate of UART using technique for implementation of UART using FIFO with the help of VHDL description language. The UART is protocol which is transmitted the information or data in serial form i.e. in serial communication mode. A special computer chip known as a universal asynchronous receiver transmitter acts as the interface between the parallel transmission of the computer bus and the serial transmission of the serial port.

Keywords: UART, RS-232, FIFO, VHDL IMPLEMENTATION ISE SIMULATOR 13.1.

I. INTRODUCTION

Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol. In serial transmission can be either synchronous or asynchronous .In synchronous transmission groups of bit are combined into frame and frame are send continuously with or without data to be transmitted. In asynchronous transmission groups of bits are sent as independent unit with start/stop flags and no data link synchronization to allow for arbitrary size gap between frames.

The UART (universal asynchronous receiver transmitter) are connected to the input of RS232 and the output if RS232 are connected to the FIFO (first in first out). The UART consist of three main components namely transmitter, receiver, baud rate generator.RS-232 are serial transmission via RS-232 is officially limited to 20kbps for a distance of 15 meter or 50 feet. Depending of the type of media used and the amount of external interference present RS-232 can be transmitted at higher speed or over greater distance or both.

Baud rate of a data communication system is the number of symbols per second transferred. A symbol may have more than two states, so it may represent more than one binary bit. Therefore the baud rate is not equal to the bit rat. FIFO stand for first in first out meaning that the oldest inventory items are recorded as sold first but do not necessarily mean that the exact oldest physical object has been tracked and sold.

II. SYSTEM MODEL

A. UART

The UART used asynchronous transmission. The asynchronous transmission means group of bit are sent as independent unit with start/stop flag and no data link synchronization. The UART controller is the key component of the serial communication subsystem of a computer. The UART takes bytes of data and transmits the individual bits in a sequential fashion. At the destination a second UART reassembles the bit into complete bytes.
In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two pin functions have been changed to allow signalling of DMA transfers. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU.

The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt). The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (216b1), and producing a 16 c clock for driving the internal transmitter logic. Provisions are also included to use this 16 c clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor- interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

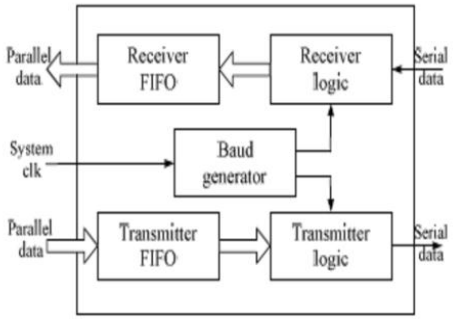

Fig. 1. Basic configuration if UART with FIFO

III. PROPOSED MODEL

A. UART FRAME FORMAT

Below is the timing diagram for the transmission of a single bytes. Uses a single wire for transmission. Each block represents a bit that can be a mark (logic '1' high) or

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space (logic '0'low). Each bit has a fixed time duration determined by transmission rate. The start bit marks the beginning of a new word. When detected the receiver synchronizes with the new data strum. Next follows the data bit (7 or 8). The least significant bit is sent first.

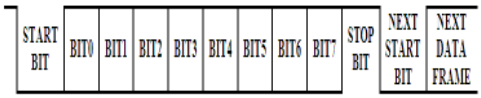

Fig. 2.

In the above frame format the above frame start the bit start bit . After start bit transmitted the 8 bit data and stop bit. In this type the one complete 8 bit data are transmitted. This 10 bit is transmitted then again the next start bit is transmitted and after 8 bit and stop bit and so on.

B. BAUD RATE

Bit rate is a measure of the number of data bit (that's 0's and 1's) transmitted in one second. Baud rate by definition means the number of times a signal in a communications channel changes state. Baud means state changes of the line per second. Baud rate refers to the number of signal or symbols changes that occur per second.

A symbol is one of several voltage, frequency or phase changes. NRZ binary has two symbols represent voltage level.

Baud Rate represents the number of bits that are actually being sent over the media, not the amount of data that is actually moved from one UART device to the other. The Baud count includes the overhead bits Start, Stop and Parity that are generated by the sending UART and removed by the receiving UART.

This means that seven-bit words of data actually take 10 bits to be completely transmitted.

BAUD RATE = NO OF BITS TRANSMITTED/ RECEIVER PER SECOND

Baud rate generator is used to generate the baud rate for both the transmitter and receiver. Not required for any other function including reads and writes. Crystal or external clock 16 bit divisor programmed in DLM/DLL registers. IN transmitter FIFO mode to write data to transmit holding register.

Transmit data is queued in TXFIFO. Data in TXFIFO is transferred to transmit shift register (TSR) when TSR is empty. TSR shift data out on TX output pin. The receiver FIFO incoming data is received in the receiver shift register (RSR) received data is queued in the RX FIFO.

C. RS-232

A popular way to transfer commands and data between a personal computer and a Microcontroller is the use of standard interface, like the one described by protocols RS232 (older) or USB (newer). The protocol RS232 defines the signals used in communication, and the hardware to transfer signals between devices.

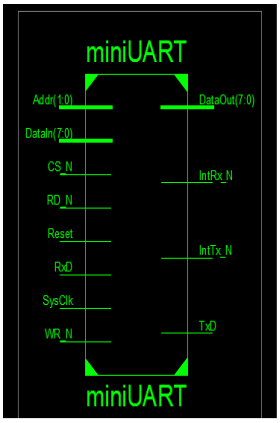

Fig. 3.

The standard defines voltage levels V(0) to be at least +5V at the transmitting end of the line TX, and can be degraded along the line to become at least +3V at the receiving and of the line. Similarly voltage level V (1) must be at least -5V at TX, and at least -3V at RX. The standard also defined the upper limit for these voltages to be up to ±15V. Logic high is transferred as V (0). The microcontroller cannot handle such voltage levels, so typically a voltage level translator is inserted between the microcontroller and the connector where the RS232 signals are available connectors are typically so-called D9 connectors, and the electric wiring in between two connectors at devices A and B is shown in Fig. for two female type connectors at both devices.

TABLE I: DEVICE UTILIZATION SUMMARY

Logic utilization	Used	Available	Utilization
No of slice register	74	19200	0%
No of slice LUT's	118	19200	0%
No of fully used bit	71	121	58%
No of bouded IOB's	27	220	12%
No of BUFG/BUFGCTRL	1	32	3%

The whole design is functionally simulated using the Mentor Graphics company's Model Sim under 40MHz system clock and 9600Hz baud rate. As shown in Fig. the 8-bit data "11111111" is input from the transmitter port 'sbuf_t', while "10010101" is serially output from the output port 'txd'; the data "11111111" is serially input from the receiver port 'rxd', while "1111111" is output from output port rf_data out'. The results show that the function of the proposed design is right

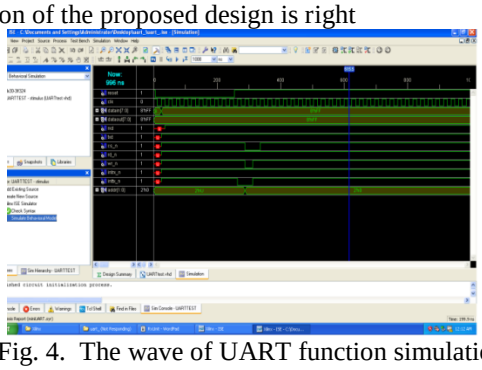

Fig. 4. The wave of UART function simulation

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IV. CONCLUSION

In this paper, we proposed a design of multi channel UART. It internally consists of baud rate generators, Asynchronous FIFO along with transmitters and receivers. The design is successfully simulated using xilinx ise 13.1 software and synthesized using Xilinx software. The results are stable and reliable which shows the correct functionality. Hope this multi channel design meet the modern communication needs. The design has great flexibility, high integration. Because of using FIFO data loss is avoid.

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