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Measurement of Interface Trapped Charge Densities(D_{it}) in 6H-SiC MOS Capacitors

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Abstract: At High oxidation temperature of SiC shows a tendency of carbide formation at the interface which results in poor MOSFET transfer characteristics. Thus we developed oxidation processes in order to get low interface charge densities. N-type 6H-SiC MOS capacitors were fabricated by different oxidation processes: dry, wet, and dry-reoxidation. Gate oxidation and Ar anneal temperature was 1150 ℃. Ar annealing was performed after gate oxidation for 30 minutes. Dry-reoxidation condition was 950 ℃, H2O ambient for 2 hours. Gate oxide thickness of dry, wet and dry-reoxidation samples were 38.0 nm, 38.7 nm, 38.5 nm, respectively. Mo was adopted for gate electrode. To investigate quality of these gate oxide films, high frequency C-V measurement, gate oxide leakage current, and interface trapped charge densities (Dit) were measured. The interface trapped charge densities (Dit) measured by conductance method was about 4×10^{10} [$cm^{-1}eV^{-1}$] for dry and wet oxidation, the lowest ever reported, and 1×10^{11} [$cm^{-1}eV^{-1}$] for dry-reoxidation

Keywords: SiC, MOS capacitor, oxidation, high-freqency C-V, D_{it} , conductance method, gate oxide leakage current densities.

1. INTRODUCTION

Silicon carbide has been shown to be an attractive material for high power, high voltage and high temperature applications. Compared to Si, the 6H-SiC has 3 times larger energy band gap, 7 to 8 times higher breakdown field, 10 times lower power consumption, 3 times higher saturated electron drift velocity, and 3 times higher thermal conductivity with excellent thermal stability and radiation tolerance [1], [2].

However, these tremendous theoretical advantages have yet to be realized in experimental SiC devices. Fabricated SiC devices have following problems: SiC's relatively immature crystal growth, yield decrease by micropipe evolution in SiC, uncertain threshold voltage shifts caused by interface surface states, decrease of driving current and switching speed caused by electron/hole mobility reduction in SiC-SiO_2 interface and reliability of SiC-metal ohmic contacts [3].

The reason of above mentioned problems, interface trapped charges that affect the threshold voltage, transconductance(gm), subthreshold swing, and channel mobility can be studied using MOS capacitors fabricated by oxidizing SiC n-epilayer. We developed oxidation processes in order to get low interface trapped charge densities. To investigate quality of SiC gate oxide films, high frequency C-V characteristics, gate oxide leakage current, and D_{it} were measured.

This paper is organized as follows. Section 2 discusses various oxidation methods and overall process flow of SiC MOS capacitors. Section 3 presents experimental results and discussions. Finally, comparison between different oxidation methods and conclusions are given in Section 4.

2. EXPERIMENTAL PROCEDURE

To appraise quality and reliability of SiC gate oxide layers, N-type SiC MOS capacitors were fabricated by different oxidation processes: dry, wet, dry-reoxidation [4], [5] as shown in table 1.

Si-faced, n-type 6H-SiC wafer with 5um thick epi-layer (doping level of 5×10^{16} cm^{-3}) was used to fabricate the MOS capacitors. Prior to oxidation, samples were cleaned using an RCA cleaning process by a dip in a HF solution. After the cleaning, the samples were immediately loaded into the oxidation furnace in a hydrogen atmosphere at 800 ℃.

Table 1. Experimental conditions of SiC oxidations.

	Oxidation Conditions	Annealing Condition	Reoxidation Condition
Dry	1150℃, O_2	1150℃, Ar	None
Wet	1150℃, Bubbler, O_2		None
Dry-reoxidation	1150℃, O_2		950℃, Bubbler, O_2

Fig. 1 shows dry, wet oxidation process conditions used in growing gate oxide layers.

Gate oxidation and Ar anneal temperature were 1150 ℃ as shown in Fig. 1. Ar annealing was performed after gate oxidation for 30 minutes.

Gate oxide thickness of dry, wet oxidation samples were 38.0 ㎚, 38.7 ㎚, respectively.

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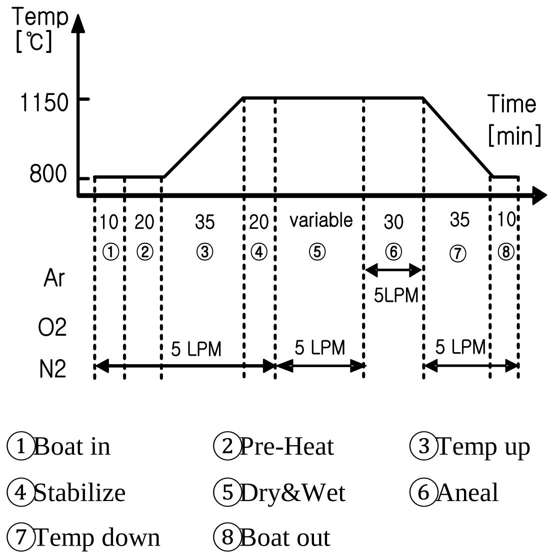

Fig. 1. Dry, wet oxidation process conditions.

Fig. 2 shows the dry-reoxiation process conditions. Gate oxidation and Ar anneal temperature were 1150 ℃. Reoxidation was performed at 950 ℃ after Ar annealing for 2.5 hours. Gate oxide thickness of dry-oxidation sample was 38.5 ㎚ measured by spectroscopy [6], [7].

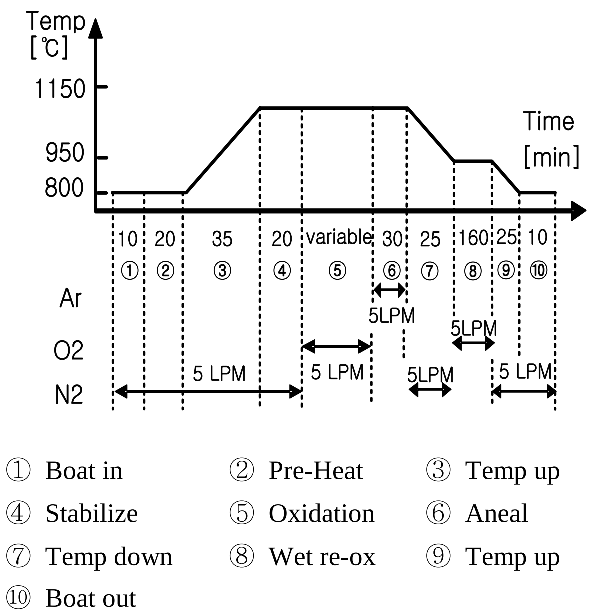

Fig. 2. Dry-reoxidation process conditions.

Overall process flow of SiC MOS capacitors is shown in Fig. 3. Gate electrode (~250 ㎚) was deposited on the oxide layers using sputtered Mo.

The gate electrode was patterned using photolithography techniques and defined by wet etching. Sputtered Al was deposited 1000 Å for backside contact [8].

Fabricated SiC MOS capacitors were 200×200, 300×300 ㎛ squares.

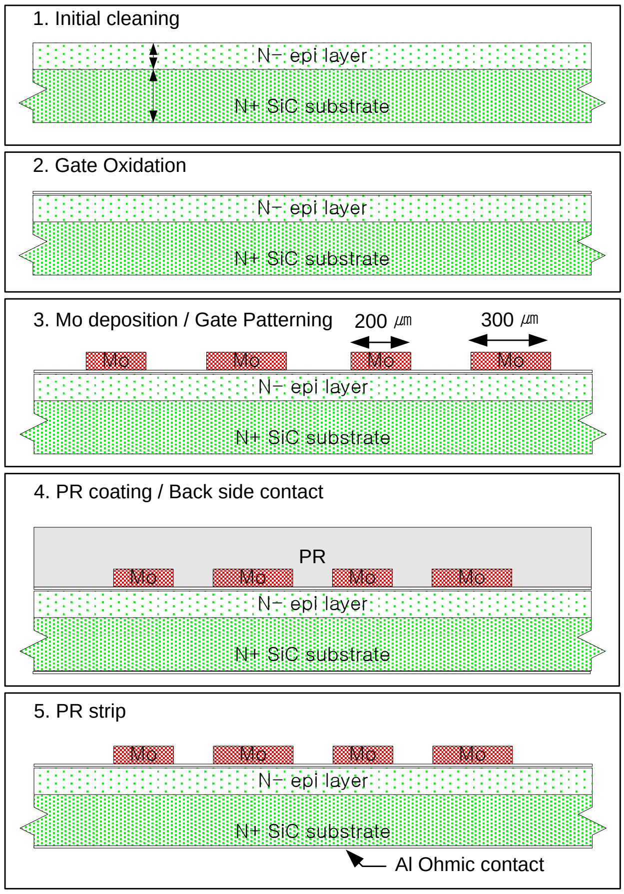

Fig. 3. Overall process flow of SiC MOS capacitors.

3. RESULTS

A variety of methods can be used to measure the electrical characteristics of SiC MOS capacitors. To investigate quality of these gate oxide films, high frequency C-V curves, gate oxide leakage current densities and D_{it} were measured by using HP4284A LCR meter and HP 4156A Semiconductor Parameter Analyzer.

Fig. 4 shows the high frequency C-V curves of the SiC MOS capacitors for different oxidation conditions. The high frequency C-V characteristics were measured by sweeping the gate voltages (5 V => -5 V => 5 V). The MOS capacitors change from accumulation mode to inversion mode (when gate voltage decreases from 5 V to –5 V) at the –2 V ~ 2 V. The slope of the transition region of high frequency C-V characteristics represents the interface state densities: the sharper transition, the less interface state densities. Wet and dry oxidations have less interface state densities compared to dry-reoxidation contray to our expectations. As the gate voltage sweeps from 5 V to –5 V and back to 5 V, C-V curves shows a slight hysterisis to negative direction.

Fig. 5 shows the leakage current densities for gate oxide layers. The measurements show that leakage current densities are about 10^{-9} [A/cm^2] ~ 10^{-12} [A/cm^2]. The leakage current densities for wet and dry oxidation were about same and lower than those of dry-reoxidation about 1 order of magnitude.

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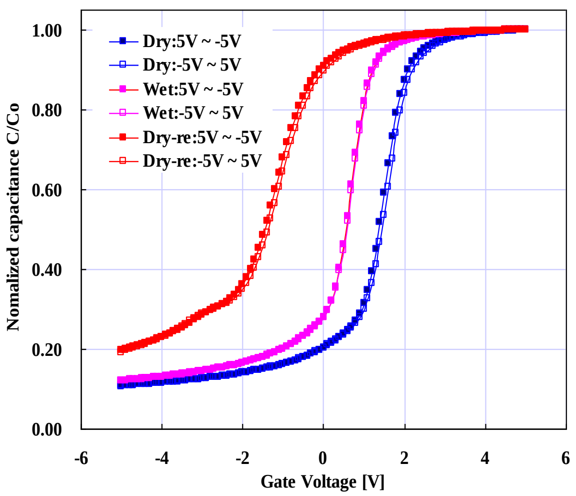

Fig. 4. High frequency C-V curves for different oxidation conditions.

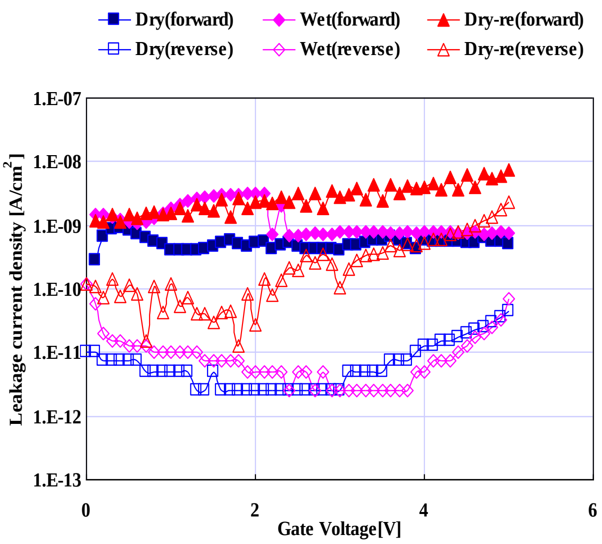

Fig. 5. Leakage current densities for different oxidation conditions.

Next, the conductance method was used for measurement of D_{it} [9] in 6H-SiC MOS capacitors. It is based on the measurement of the equivalent parallel conductance G_P of an MOS-capacitor as a function of bias and frequency. The simplified equivalent circuit of an MOS-capacitor appropriate for the conductance method is shown in Fig. 6. (a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_S, and the interface trap capacitance C_{it}. The capture of carriers by D_{it} and emission of carriers from from D_{it} is a lossy process, represented by the resistance R_{it}. For interface trap analysis it is convenient to replace the circuit of Fig. 6(a) by that in Fig. 6(b), where C_p and G_p are from a simple circuit conversion.

$$C_P = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2} \qquad (1)$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \qquad (2)$$

where $C_{it}=qD_{it}$, $\omega=2$ $\varpi = 2\pi f$, and $\tau_{it} = R_{it}C_{it}$ the interface trap time constant, is given by $\tau_{it} = [v_{th}\sigma_p N_A \exp(-q\phi_s / kT]^{-1}$. G_p is divided by ω to make Eq. (2) symmetrical in $\varpi\tau_{it}$. Eq. (1) and (2) are for interface traps with a single energy level in the band gap. Interface traps at the SiO_2-Si interface, however, are continuously distributed in energy throughout the semiconductor band gap. Capture and emission occurs primarily by traps located within a few kT/Q above and below the Fermi level for such a continuum of interface traps. This results in a time constant dispersion and gives the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln(1+\omega^2\tau_{it}^2) \qquad (3)$$

The units of conductance are S/cm^2 in these equations.
Eq. (1) and (2) show that the conductance is easier to interpret than the capacitance because Cs is not required in Eq. (2). The conductance is measured as a function of frequency and plotted as G_p / ω versus ω or f. The function G_p / ω has a maximum at $\omega=2/\tau_{it}$, and at that maximum $D_{it}=2G_p/q\omega$. For Eq. (3) we find $\omega=2/\tau_{it}$ and $D_{it}=2.5G_p / q\omega$ at the maximum. Hence we determine D_{it} from the maximum G_p / ω and determine τ_{it} from ω at the peak conductance location on the ω-axis. Capacitance meters and bridges generally assume the device to consist of the parallel C_m-G_m combination in Fig. 6(c). A simple circuit comparison of Fig 6(b) to 6(c) gives G_p / ω in terms of the measured capacitance C_m the oxide capacitance, and the measured conductance G_m as Eq. (4).

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \qquad (4)$$

The series resistance is assumed negligible.
An approximate expression giving the interface trap densities in terms of the measured maximum conductance is Eq. (5).

$$D_{it} \approx \frac{2.5}{q}\left[\frac{G_p}{\omega}\right]_{MAX} \qquad (5)$$

The table 2, 3, 4 show SiC MOS capacitor C_m, G_m, C_i for dry, wet and dry-reoxidation as function of bias and frequency [9].

Table 2. SiC MOS capacitor C_m, G_m, C_i for dry oxidation.

Voltage [V]	Freq [KHz]	C_m [S/Cm^2]	G_m [F/Cm^2]	C_i [F/Cm^2]
1.8	300	1.2E-06	1.67E-11	2.49E-11
1.4	100	3.00E-07	1.16E-11	2.47E-11

1.3	50	1.35E-07	1.00E-11	2.47E-11
1.2	10	3.15E-08	9.91E-12	2.47E-11
1.2	5	1.71E-08	9.42E-12	2.47E-11
1.1	1	2.94E-09	9.36E-12	2.34E-11
1.1	0.7	2.68E-09	9.21E-12	2.52E-11

Table 3. SiC MOS capacitor C_m, G_m, C_i for wet oxidation.

Voltage [V]	Freq [KHz]	C_m [S/Cm^2]	G_m [F/Cm^2]	C_i [F/Cm^2]
0.8	300K	7.45E-07	1.33E-11	2.31E-11
0.6	100K	1.79E-07	1.09E-11	2.26E-11
0.5	50K	9.39E-08	9.71E-12	2.27E-11
0.5	10K	2.47E-08	9.64E-12	2.27E-11
0.5	5K	1.36E-06	9.50E-12	2.29E-11
0.4	1K	2.51E-09	9.09E-12	2.31E-11

Table 4. SiC MOS capacitor C_m, G_m, C_i for dry-reoxidation.

Voltage [V]	Freq [KHz]	C_m [S/Cm^2]	G_m [F/Cm^2]	C_i [F/Cm^2]
-0.9	1000	4.37E-06	1.08E-11	1.84E-11
-1	500	3.88E-06	1.30E-11	1.84E-11
-1.3	100	4.47E-07	1.01E-11	1.90E-11
-1.4	50	2.34E-07	9.95E-12	1.91E-11
-1.5	10	5.24E-08	9.13E-12	1.91E-11
-1.6	5	2.61E-08	9.55E-12	1.91E-11
-1.8	1	5.06E-09	9.50E-12	1.91E-11

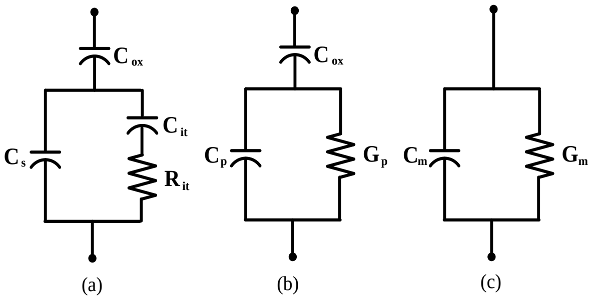

Fig. 6. Equivalent circuits for conductance measurements. (a) MOS capacitor with interface state time constant, (b) simplified circuit of (a), (c) measured circuit

Fig. 7 shows D_{it} as a function of energy determined from the conductance method. It is based on the measurement of the C_m-G_m of an MOS capacitor as a function of bias and frequency. Fig. 7 shows measured interface states located in the band gap from 0.6 eV to 1.2 eV from the conduction band edge. The extracted D_{it} for wet and dry oxidation were lower than those for dry-reoxidation about 1 order of magnitude [10].

4. CONCLUSION

N-type 6H-SiC MOS capacitors were fabricated by different oxidation processes: dry, wet, and dry-reoxidation. Mo was deposited for gate electrode. Al was deposited for backside contact. Fabricated 6-H SiC MOS capacitors were 200×200, 300um×300um squares. To investigate electrical characteristics of these gate oxide films, the high frequency C-V response, gate oxide leakage current, and interface trapped charge densities of the 6H-SiC MOS capacitors for different oxidation conditions were measured. The measurements show that leakage current densities is from 10^{-9} [A/cm^2] to 10^{-12} [A/cm^2]. D_{it} measured by conductance method were about 4×10^{10} [cm^{-1}eV^{-1}] for dry and wet oxidation, the lowest ever reported, and 1×10^{11} [cm^{-1}eV^{-1}] for dry-reoxidation

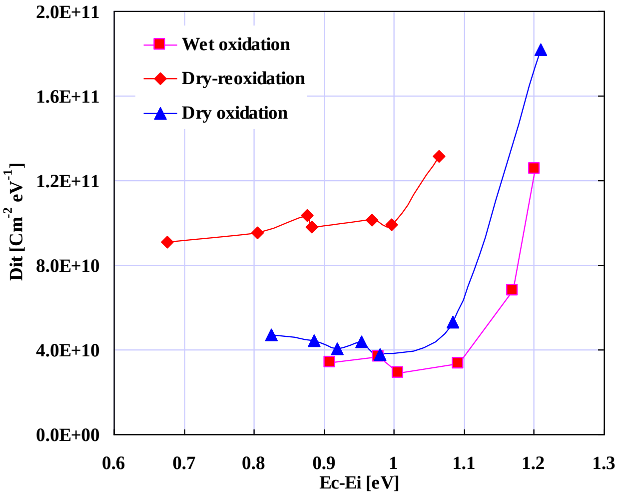

Fig. 7. Interface trapped charge densities as a function of energy for various oxidation conditions.

REFERENCES

[1] D. M. Brown et al., "High temperature silicon carbide planar IC technology and first monolithic SiC operational amplifier IC" *Trans . 2nd International High Temp. Elec. Conf,* pp. XI-17, June, 1994.

[2] J. N. Shenoy et al., " High voltage double implanted powe MOSFETs in 6H-SiC" *54th Annual Device Research Conference*, late news, June 24-26, Santa Barbara, CA.

[3] Philip G. Neudeck "Recent Progress in Silicon Carbide Semiconductor Electronics Technology" NASA Lewis Research Center, M.S. 77-1, 21000 Brookpark Road, Cleveland, OH 44135, USA

[4] Jae S. Choi, Jang H. Lee, Boo H. Lee, Gun Y. Lee, Yeong S. Kim, and Keun H. Park, "Characterization of the SiC MOSFET" The Korean Physical Society, vol. 47, no. 2., pp. 108, 2003.

[5] Jae S. Choi, "SiC CMOS Devices for High Temperature Applications" A thesis for the degree of Ph. D , Department of Semiconductor Engineering Graduate School, Chungbuk National University, Cheongju, Korea, 2004

[6] Chung W. Oh, Jae S. Choi, Ji H. Song, Jang H. Lee, Hyung G. Lee, Keun H. Park, and Yeong S. Kim, "Fabrication of 6H-SiC MOSFET and Digital IC" J. Korean Institute of Electrical and Electronic Material Engineers, vol. 16, no.7., pp. 584, July 2003.

[7] J. S. Choi, W. S. Lee, D. H. Shin, H. G. Lee, Y. S. Kim, and K. H. Park, "Abnormal hysteresis property of SiC oxide C-V Characteristics", *Tech. Dig. Of Int'l Conf. on SiC and Related Material-ICSCRM 2001*, Tsukuba, Japan, pp. 619, 2001.

[8] C. Y. Lee, J. H. Song, J. S. Choi, J. B. Lee, K. H. Kim, Y. S. Kim, K. H. Park, and H. G. Lee, "Characteristics of Non-alloyed Mo Ohmic Contacts to Laser Activated p-type SiC" J. Korean Institute of Electrical and Electronic Material Engineers, vol. 16. no.7., pp. 577, July 2003.

[9] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, *New York*, wiley, 1982.

[10] D. K. Schroder, *Semiconductor material and device characterization, New York,* John Wiley & Sons, Inc., pp. 267-277, 1990.

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BIOGRAPHIES

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