ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 7, July 2015

Design of Asynchronous Viterbi Decoder using Hybrid Register Exchange Method for Low Power Applications

Pooja M. Chandel[1], Prof.M. N. Thakre[2] , Prof.G. D. Korde[3]

Student M. Tech, VLSI, BDCE, Sewagram, Wardha, India[1]

Assistant Professor, Sel. Grade, VLSI, BDCE, Sewagram, Wardha, India[2]

Assistant Professor, VLSI, BDCE, Sewagram, Wardha, India[3]

Abstract: This paper describes the design of an asynchronous Viterbi decoder having a convolutional encoder with constraint length K=3 and a code rate ½. Viterbi decoders are used to decode convolutional codes. Using Viterbi algorithm Viterbi decoder decodes a bit stream that has been encoded using convolutional encoder. The soft decision output is used for convolutional encoder. In this paper we have used Hybrid Register Exchange Method (HREM) which is the combination of Trace Back Method (TBM) and Register Exchange Method (REM) for decoding the bit stream. HREM is having an advantage over TBM and REM that it reduces the switching activity due to which power can be reduced. The choice of asynchronous design was predicted due to its power advantage. Asynchronous designs are inherently data driven and are active only when doing useful work, enabling considerable savings in power and better reliability. The main aim of proposed method is to reduce power consumption.

Index Terms: Convolutional encoder, Viterbi Algorithm, Viterbi decoder, asynchronous Viterbi decoder, power consumption, hybrid register exchange method, soft output decision.

1. INTRODUCTION

The Viterbi decoding algorithm was proposed and analyzed by Viterbi in 1967 [1], is widely used as a decoding technique for convolutional codes as well as the bit detection method in storage devices. The algorithm works by forming trellis structure, which is traced back for decoding the received information. Convolutional encoding with Viterbi decoding is a powerful method for forward error correction. In more than one billion cell phones Viterbi decoders currently find their use. Viterbi decoders used in digital wireless communications are complex and dissipate large power.

Viterbi decoders [2] are used to decode data which is encoded using convolutional encoders and transmitted over noisy channels. A message encoded using a convolutional encoder follows what is a trellis diagram which shows the different states of the encoder as well as the path taken to encode an arbitrary message. Viterbi's algorithm tries to reconstruct this correct path based on the received stream, despite errors in the received stream. This is done by reconstructing the trellis diagram and allocating a weight to each branch and node (i.e. state) of the reconstructed trellis, at each time slot. By tracing back through the reconstructed trellis, the decoder can detect and correct errors in the received stream.

Two design styles are available for designing the Viterbi decoder i.e synchronous and asynchronous. Synchronous designs are controlled by a global clock, running throughout the entire system. Asynchronous designs, on the other hand, are locally rather than globally synchronized and use handshaking signals between their components in order to perform the necessary synchronization and sequencing of events. There are many advantages to be gained from migrating to asynchronous designs such as negligible power consumption of ideal parts and switching activity is also less.

Asynchronous systems produce less electromagnetic emissions. These signals interfere with cellular phones, television and navigation systems [3]. There are two types of decision outputs, hard output and soft output [5]. In soft decision output, error correcting capability is more as compared to hard output decision. So to increase the accuracy as compared with hard decision outputs, soft output Viterbi algorithm can be used.
There are two types of decoding technique, Register Exchange Method (REM) and Trace Back Method (TBM).

The REM is simple, but it requires large power consumption and large chip area.TBM is used for large constraint length and for high performance. However, the TBM has drawbacks, which requires last-in-first-out (LIFO) buffer and has to use multiple read operations for high speed operation. This multiple operation results in complex control logic. One of the promising solutions to reduce the switching activity can be achieved by combining the REM and TBM techniques. The method is referred to as Hybrid Register Exchange Method (HREM) [5]. In this method, register exchange and trace back methods are combined and therefore the name Hybrid Register Exchange Method which reduces the switching activity and power.

This paper provides the design of convolutional encoder with soft output decision and an asynchronous Viterbi decoder using HREM (hybrid register exchange method) used for low power consumption.

2. CONVOLUTIONAL ENCODER

Fig1 shows the convolutional encoder (2, 1, 3) structure which we have used in our paper. It consist of 2^m (m=2) shift stages, with a constraint length (K = 3) and modulo-2 adders (n=2) giving the output of the encoder.

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 7, July 2015

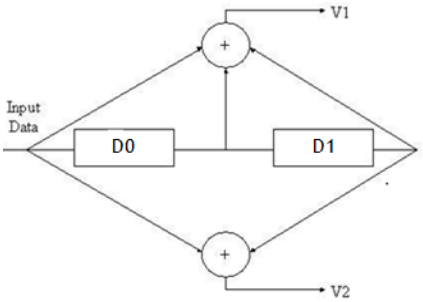

Fig 1. Convolutional Encoder

(r = ½, K=3)

The rate of the code becomes ½. The output of V1 and V2 of the adders are calculated as follows:

V1= input XOR D0 XOR D1
V2= input XOR D1

2.1 Soft Decision Decoding

In this paper soft decoding is used to decode the Viterbi decoder. Soft decoding [4] is used to calculate Euclidean distance of the each branch of each state. In this design the soft decoding technique is fixed in the form of 3 & -3. Zero indicates through -3 & one indicates through +3. If the metric of any state is in negative form then 2's complement of that negative value is taken for further procedure. Likewise, all branch metrics are calculated, and minimum path is taken as survivor path for the trellis. On the other hand hard decoding does not need to define their metrics as +3 or -3. It is just define by 0 or 1 only. Hard decoding is used calculate the hamming distance between the respective metric.

3. VITERBI DECODER

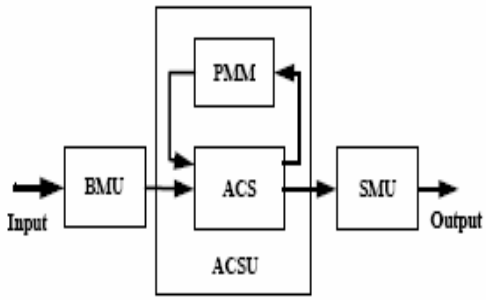

Fig 2.Block Diagram of Viterbi Decoder

Fig2. Shows a block diagram of asynchronous Viterbi decoder. It consists of three main blocks which performs the operation.

3.1 Branch Metric Unit (BMU)

BMU works for calculating the branch metrics according to received sequence. For two 2-bit soft decision input bits (i0, i1) each ranging from -3 to +3, four 5-bit branch metrics are generated. The BMU perform simple add; subtract operations on the input bits to generate the output. For example the branch metric for the state transition which produces the binary output (01) is i0 - i1. The bit serial format of the BMs is then fed into the ACSU.

3.2 Path Metric Unit (PMU):

PMU performs the node plus branch weight calculations and selects the lower weight as the next weight for a node in particular timeslot. The computed node weights are then fed back and become the node weights for next timeslot. On each time slot, this information is passed to the next Unit.

3.3 Survivor Memory Unit (SMU):

The Survivor Memory Unit receives the bit decision from the PMU. This will produces the decoded sequence. Two methods are used in decoding sequence i.e trace back method (TB) and register exchange method (REM). The TB method extracts the decoded bits; beginning from the state with the minimum PM. Beginning at this state and tracing backward in time by following the survivor path, which originally contributed to the current PM, a unique path is identified. While tracing back through the trellis, the decoded output sequence, corresponding to the traced branches, is generated in the reverse order.

In the register exchange, a register assigned to each state contains information bits for the survivor path throughout the trellis. In fact, the register keeps the partially decoded output sequence along the path. But as trace back method decreases speed of operation, register exchange is having frequent switching activity due to which we have used hybrid register exchange method in our paper.

3.4 Hybrid Register Exchange Method (HREM):

One of the promising solutions to reduce the switching activity can be achieved by combining the REM and TB techniques. Corresponding block as shown in Fig 3. The initial state can be first traced through an m cycle, and then transfer the content of initial state to the current state and the next m bits of the register is the m bits of current state itself.

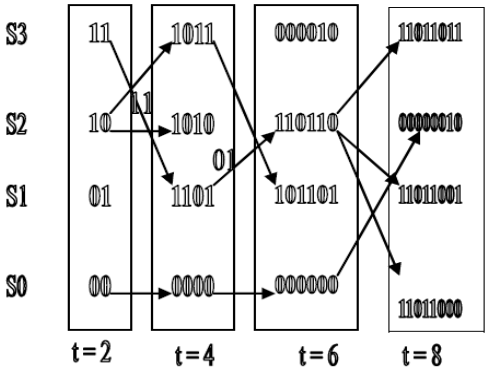

Fig.3: HREM

Here in the Fig.7 pretraceback information at t = 4 is 11 for state S1 therefore the content of S1 state register at t = 4 is the data of S3 at t = 2 and the state S1 itself. And at t = 6 the pretraceback information of state S2 is 01, therefore the content of S2 state register at t = 6 is the data of S1 at t = 4 and the state S1 itself. This process goes continue, the final state register contains the decoded output. The memory operation is not at every cycle therefore it get reduced by a factor of m. also the shifting of data from one register to another is reduced that is the switching activity will reduce.

4. ASYNCHRONOUS VITERBI DECODER

Asynchronous circuits are composed of blocks that communicate to each other by handshaking via asynchronous channels, in order to carry out the required synchronization, communication, and sequencing of operations. Asynchronous communication channel consists of a bundle of wires and a protocol to communicate the data between the blocks. It has two

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 7, July 2015

types of encoding scheme in asynchronous channels. If the encoding scheme uses one wire per bit to transmit the data and a request line to identify when the data is valid is called single-rail encoding. The channel is called a bundled-data channel. Alternatively, in dual-rail encoding the data is sent using two wires for each bit of information. In this paper we have used 4 phase handshaking protocol and single rail bundled data encoding scheme.

4 Phase Bundled Data Protocol

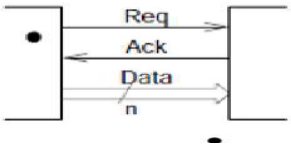

Fig.4 Bundled data channel

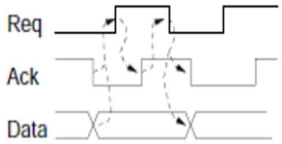

Fig.5. A 4phase Bundled data protocol.

In this type of protocol, the request and acknowledge wires also use normal Boolean levels to encode information. The term 4-phase refers to the communication actions:

- The sender issues data and sets request high,
- The receiver absorbs the data and sets acknowledge high,
- The sender responds by taking request low, at which point the data is no longer guaranteed to be valid, and
- The receiver acknowledges this by taking acknowledge low.

At this point the sender may initiate the next communication cycle. Figure 5 illustrates the communication actions explained above.

5. SIMULATION RESULTS

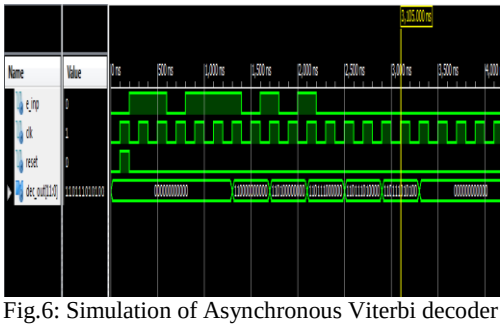

Fig.6: Simulation of Asynchronous Viterbi decoder

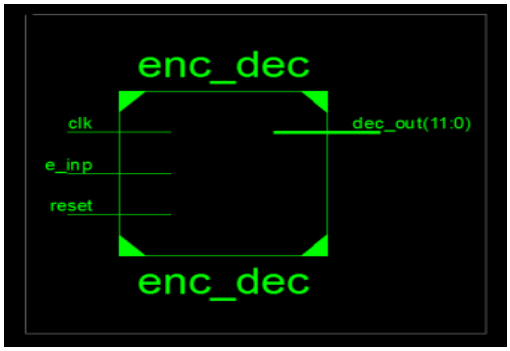

Fig 7: RTL View

This section provides some simulation results for Viterbi decoder on Xilinx Spartan3 FPGA chip. The ISE13.1 is used for synthesizing the VHDL modeling codes. Output of simulation shown in figure6 and RTL schematic for the decoder shown in Figure 7.

Power Consumption Analysis

Feature	Result
Code rate	1/2
Constraint Length(K)	3
Power Consumption	28mW

Comparison of Power Consumption

Parameter	Reference [10]	Proposed
Dynamic Power	1.20mW	1mW

6. CONCLUSION

Viterbi decoders employed in digital mobile communications are complex in its implementation and dissipate large power. This paper describes the convolutional encoder with soft decision output having constraint length K=3 and code rate 1/3. The proposed Viterbi decoder uses HREM technique for decoding and asynchronous design techniques to reduce power consumption. The asynchronous design was based on 4 phase hand shaking protocol for low power consumption .HREM technique reduces the switching activity and results in less memory operations. Total power and dynamic power Consumption is achieved when compared with the previous designs. The design of Asynchronous Viterbi decoder is simulated and Power is analyzed in Xillinx ISE 13.1 successfully.

REFERENCES

[1] A.J.Viterbi, "Error bounds for convolutional coding and an asymptotically optimum decoding algorithm", IEEE Tran. on Inform.Theory, Vol. 2, Pp. 260-269, Apr. 1967.
[2] B. P. Lathi, "Modern Digital and Analog Communication Systems," Oxford University Press, New York, 1998.
[3] Mohamed Kawokgy C. André T. Salama,"Low Power Asynchronous Viterbi Decoder for Wireless Applications," International Symposium on low power Electronics and Design (ISPELD) 2004.
[4] Wing-Kin Chan, "An asynchronous SOVA decoder for wireless communication application", IEEE Proceedings of the 2004 International Symposium on Circuits and Systems, 2004 .
[5] Mrs. D. M. Khatri,S.L. Haridas, Dr. N. K. Choudhari, "Soft Output Viterbi Decoder Using Hybrid Register Exchange", ICWET'11, February 25–26, 2011, Mumbai, Maharashtra, India.
[6] Dr. H. Meliani, A. Gullal "A comparison between Vitrebi algorithm soft and hard output decision decoding".
[7] Priyadharshini Shanmugasundaram, "Synchronization in Asynchronously Communicating Digital Systems.
[8] Kawokgy M., Salama C.A.T, "A low-power CSCD asynchronous Viterbi decoder for wireless applications", ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2007, Portland, OR.
[9] T. kalavati Devi and C Venkatesh, "Design of Low Power Viterbi Decoder using Asynchronous Techniques", International Journal of Advances in Engineering &Technology,Vol 4, Issue 1, pp. 561-570, July 2012.
[10] Rajesh.C and A Sreenivasa Murthy, "VHDL implementation of Fast and Efficient Viterbi Decoder", International Journal of Advanced Computer Research,Vol 3,Issue 12,September 2013.

DOI 10.17148/IJARCCE.2015.4753