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Design Approach of High Performance 32-bit Multiplier Based on Vedic Mathematics using Pipelining

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Abstract: Many processor devotes a considerable amount of processing time in performing arithmetic operations particularly multiplication operations therefore high-speed multiplier is much desired. There are various methods of multiplication in Vedic mathe-matics, Urdhva tiryagbhyam, being a general multiplication formula is equally applicable to all cases of multiplication. This is more efficient in the multiplication of large numbers with respect to speed and area. In that we will see the different types of multiplier that will be generated using a Vedic Mathematics. In that we will proposed a 4-bit binary multiplie using this sutra. A new 4-bit adder is proposed which when used in multiplier, . Also we proposed 8-bit adder, 16 bit adder & 32 bit adder using this adder we proposed an 8-bit multiplier, 16 bit multiplier & 32 bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) for generating the partial products. Also this paper proposed the design of high speed Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics. For Improving our generated result we used the concept of pipelining and design 4-bit, 8-bit, 16-bit & 32-bit pipeline Multiplier.

Keywords: VLSI, Urdhva Tiryagbhyam sutra, Adder, Multiplier.

I.INTRODUCTION

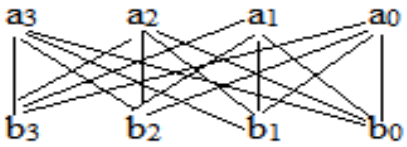
Multipliers are essential in implementation of systems realizing many important functions such as fast fourier transforms and multiply accumulate. Multiplier is one of the key hardware blocks in designing arithmetic operation, signal and image processors. Many transform algorithms like the basic building blocks in Fast Fourier transforms, DCT, DFT etc., make use of multipliers. High performance multipliers using Vedic mathematics are proposed and conclude that it is suitable for high-speed complex arithmetic circuits .

The basic idea behind all these attempts was the fast implementation of the multiplier and addition of the partial products . With advances in technology, many researchers have tried to design multipliers using Vedic sutras, which offer high speed, low power consumption, and regularity of layout and less area or even combination of them in multiplier Multiplier is time-consuming operations in many of the digital signal processing applications and computation can be reduced using the Vedic sutras and the overall processor performance can be improved for many applications.

Therefore, the goal is to create hybrid architectures that is comparable in speed, area and power, but requires less area than a design using a standard multiplier. The motivation behind this work is to explore the Design and implementation of hybrid multiplier architecture. The proposed pipelined Vedic-Array multiplier is based on the Vedic Sutras.

II.VEDIC MATHEMATICS

An illustration of Urdhva Tiryagbhyam sutra is shown in Figure 1



The 4x4 multiplication has been done in a single line in Urdhva Tiryagbhyam sutra [1], whereas in shift and add(conventional) method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier. Now we will see the multiplication of two decimal numbers using the Urdhva Tiryagbhyam sutra which is shown in fig no.2 below.

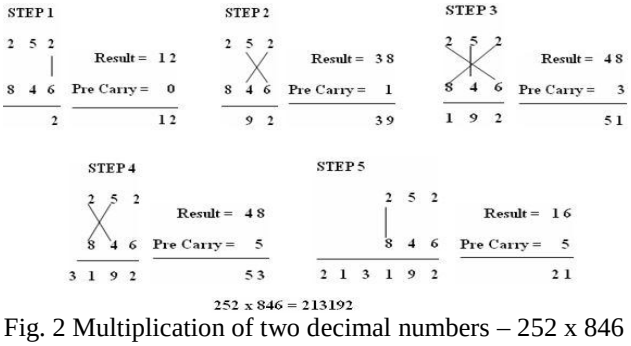


Fig. 2 Multiplication of two decimal numbers – 252 x 846

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III. IMLIMENTED WORK

Pipelining:- Pipelining is one of the popular methods to realize high performance computing platform. Pipelining is a technique where multiple instruction executions are overlapped. It comes from the idea of a water pipe: continue sending water without waiting the water in the pipe to be out.

By pipelining the unit of a system we can produce result in every clock cycle.It leads to a reduction in the critical path. It can either increase the clock speed (or sampling speed) or reduces the power consumption at same speed in a DSP system.

Pipelining is a concept to reduce the delay in the critical path.Pipelining is a set of data processing elements connected in series, where the output of one element is the input of the next one. The elements of a pipeline are often executed in parallel or in time-sliced fashion; in that case, some amount of buffer storage is often inserted between elements.

First we are generating a 1-bit adder having a14-Transister then using this 1-bit adder we generated 4-bit, 8-bit, 16-bit, 32-bit and 64-bit Adder. Using this adder we are generating 4-bit multiplier, 8-bit multiplier, 16-bit multiplier, 32-bit multiplier .

For reducing the delay we used the pipelining concept and using the concept of these pipelining we generate 4-bit pipeline multiplier, 8-bit pipeline multiplier, 16-bit pipeline multiplier, 32-bit pipeline multiplier.

The schematic 4-bit, 8-bit, 16-bit and 32-bit pipeline multiplier is shown in fig.3,5,7,8.

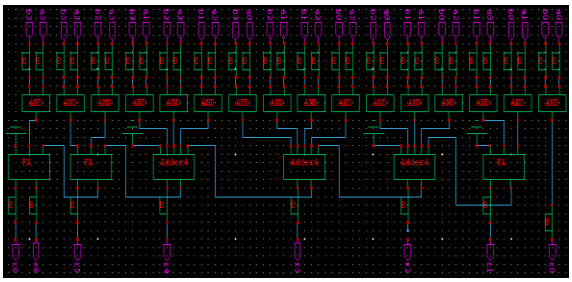

Fig.3: Schematic of 4-bit pipeline Multiplier

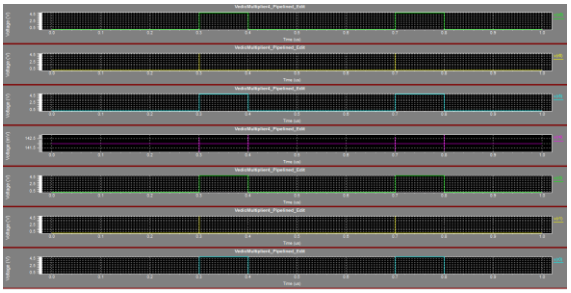

Fig.4: Output of 4-bit pipeline Multiplier in 180nm technology

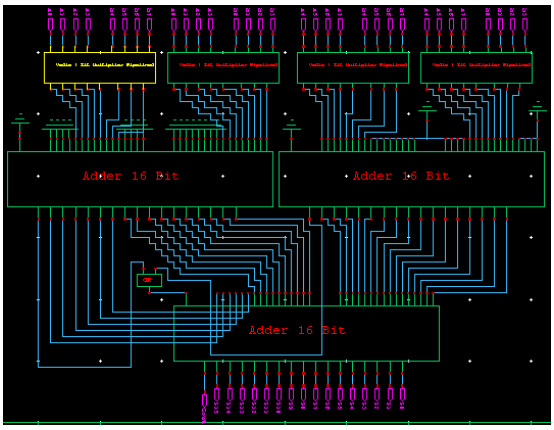

Fig.5: Schematic of 8-bit pipeline Multiplier

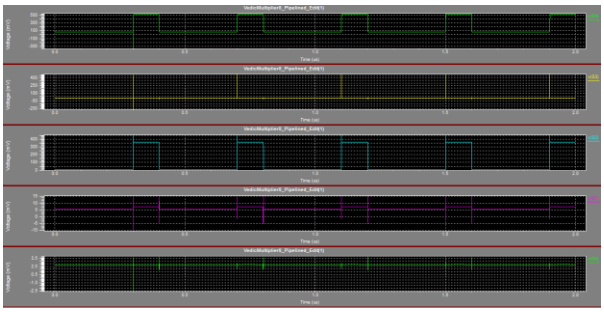

Fig.6: Output of 8-bit pipeline Multiplier in 180nm Technology

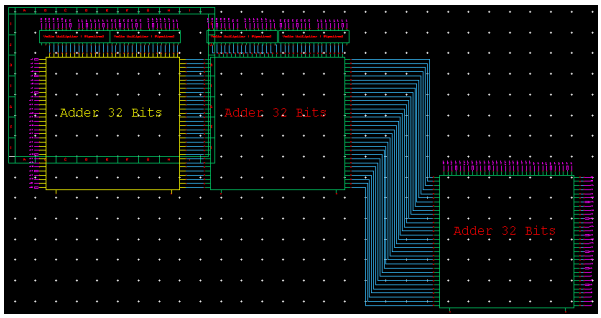

Fig.7: Schematic of 16-bit pipeline Multiplier

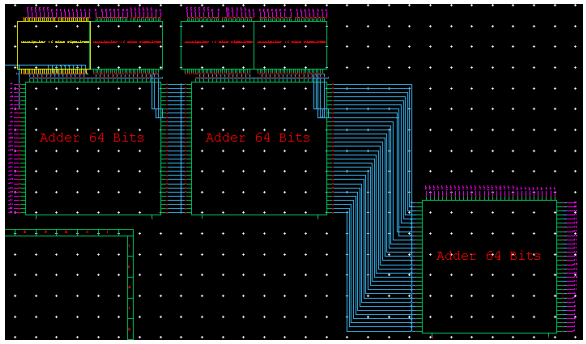

Fig.8: Schematic of 32-bit pipeline Multiplier

The output of 4-bit pipeline multiplier, 8-bit pipeline multiplier, on 180nm technology is shown in above fig 4,6. And its parameter on 180nm technology is shown in table below.

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Table 1: Parameters of Adder

Type of adder	Technology	Parameter	
		No. of gates	Power
Full adder	180nm	14	8.7704×10^{-5}
4-bit Adder	180nm	56	5.0427×10^{-4}
8-bit Adder	180nm	112	2.9435×10^{-6}
16-bit Adder	180nm	224	3.4530×10^{-4}
32-bit Adder	180nm	448	1.4821×10^{-3}

Table 2: Parameters of 32-bit Multiplier

Multiplier	Technology	Parameter	
		No. of gates	Power
4-bit multiplier	180nm	240	2.6689×10^{-3}
8-bit multiplier	180nm	1638	1.6733×10^{-3}
16-bit multiplier	180nm	3276	5.0198×10^{-3}
32-bit multiplier	180nm	6552	2.1836×10^{-2}

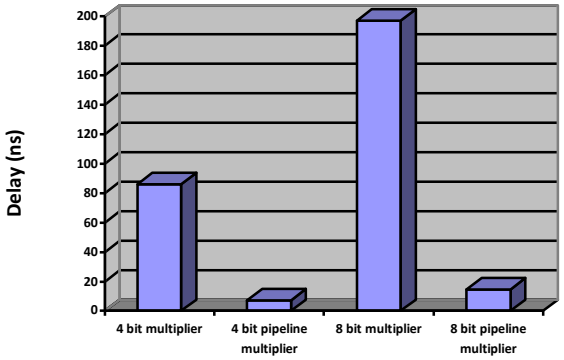
Table 3: Parameters of 32-bit pipeline Multiplier

Multiplier	Technology	Parameter	
		No. of gates	Power
4-bit pipeline multiplier	180nm	400	2.9102×10^{-3}
8-bit pipeline multiplier	180nm	2278	1.2823×10^{-3}
16-bit pipeline multiplier	180nm	10456	5.4916×10^{-3}
32-bit pipeline multiplier	180nm	44512	2.3809×10^{-2}

Table 4: The 4×4-bit & 8×8-bit Vedic Multiplier with and without pipelining in terms of Delay

Type of Multiplier	Without Pipelining	With Pipelining	% Optimization in Delay
4-bit Multiplier	86.12n	7.30n	91.52%
8-bit Multiplier	197.05n	14.60n	92.59%

Below is the graph showing delay comparisons of 4×4 and 8×8 bit Vedic Multiplier with and without pipelining for Feature Size 0.18µm



IV. CONCLUSION

In the present paper we generated a1-bit full adder using this full adder we generate 4-bit, 8-bit,16-bit & 32 -bit adder. We use these adder and generated the 4-bit , 8-bit, 16-bit & 32-bit multiplier . Also all the multipliers are generated using a Ancient Indian Vedic Mathematics technique.And we will see the result of adder & multipliers on 180nm technology.In that no. of gates are continuously increasing according to the no. of gates power level change but it will increased in little amount by using the pipelining concept. Also we see that the result in terms of Delay then 91.52% delay optimization occurs in 4-bit pipeline multiplier when compared with 4-bit multiplier and 92.59% delay optimization occurs in 8-bit pipeline multiplier when compared with 8-bit multiplier so the delay can reduced by using the pipelining concept.

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