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Design of a Low Power D-Flip Flop using AVL Technique

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Abstract: Power optimization is a very crucial issue in low voltage applications. This paper presents a design of D-Flip flop circuit using AVL techniques for low power operation. It reduces the value of total power dissipation by applying the adaptive voltage level at ground (AVLG) technology in which the ground potential is raised and adaptive voltage level at supply (AVLS) in which supply potential is increased. The main aim of the design is to investigate the power dissipation for D-Flip flop for the proposed design style. The simulation results show the there is a significant reduction in power consumption for this proposed cell with the AVL technique. The AVLS technique has less power dissipation 1.3480nwatts compared to AVLG technique 2.5729nwatts. The circuit is designed using Mentor Graphics 130nm technology.

Keywords: D Flip-flop, AVL Technique, Low power, Mentor Graphics.

I. INTRODUCTION

Sequential circuits are the logic circuits whose outputs at any instance of time depend not only on the present inputs but also on the past outputs. Sequential circuits are of two types (i) synchronous or clocked and (ii) synchronous or un-clocked. The simplest kind of sequential circuit is a memory cell that has two states. It can be either 1 or 0. Such two state sequential circuits are called flip-flops because they flip-from one state to another and then flop back.

Flip-flops are used as the memory elements which are the basic building blocks of an IC. They are used in many applications like parallel data storage, shift registers, frequency division and counters etc. As synchronous flip-flops uses a master-clock generator, which generates a periodic train of clock pulses. This leads to huge power consumption of power in synchronous circuits. So, by eliminating the unnecessary switching of the transistors with respect to clock signal in memory elements we can reduce the power dissipation to a large amount. And also by avoiding un-wanted switching of internal transistors the power can be reduced. The adaptive voltage level Logic is a better way to implement circuits designed for low power applications.

II. D- FLIP FLOP USING AVLG TECHNIQUE

The figure 2.1 shows the basic block diagram of TSPC based D Flip-flop. In AVLG technique, combinations of 1-N-MOS & 2-P-MOS transistors are connected in parallel. So that an input clock pulse is applied at the NMOS of circuit of AVLG and rest of all P-MOS are connected to ground.

This AVLG circuit is connected at the ground terminal of conventional one by removing ground. This ground terminal is connected to the AVLG circuit. Figure 2.2 shows the circuit diagram of D Flip Flip-flop designed using AVLG technique.

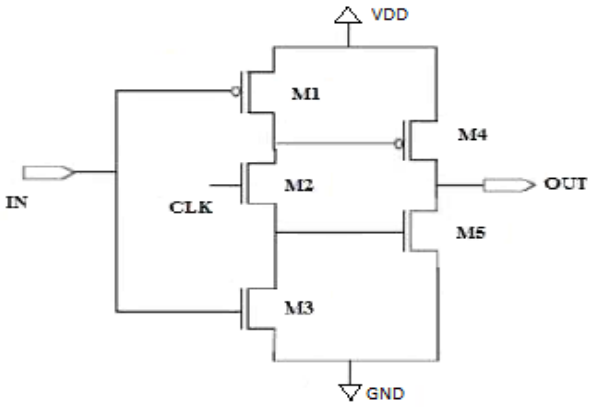

Figure 2.1 Basic TSPC based D Flip-flop

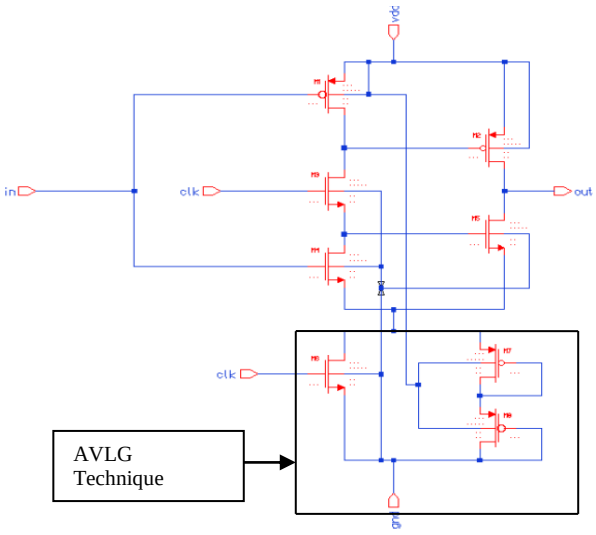

Figure 2.2 D Flip-flop designed using AVLG technique

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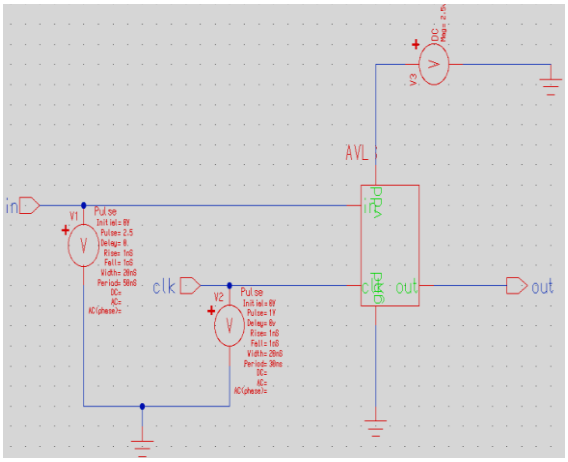

Figure 2.3 Test circuit of D Flip-flop Using AVLG Technique

III. D- FLIP FLOP USING AVLS TECHNIQUE

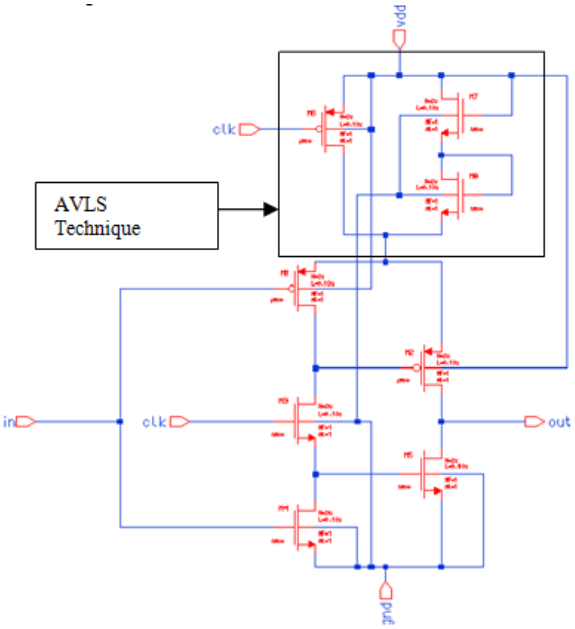

Figure 3.1 D Flip-flop designed using AVLS technique

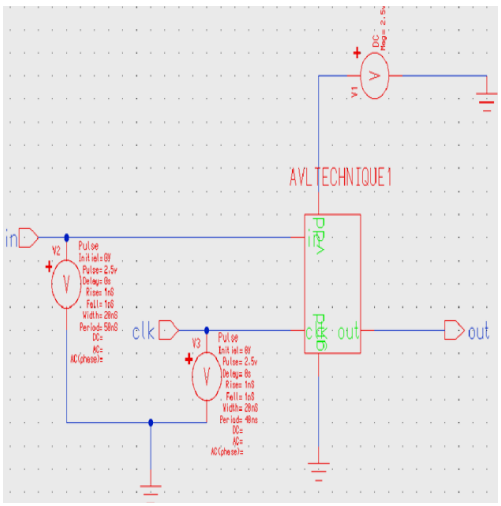

Figure 3.2 Test circuit of D-Flip flop Using AVLS Technique

In AVLS technique, a combination of 2- N-MOS & 1-P-MOS are connected in parallel. So that an input clock pulse is applied at the P-MOS of circuit of AVLS and rest of all N-MOS are connected to drain terminal. This AVLS circuit is connected at the voltage supply source terminal of conventional one by removing voltage supply source. A very small leakage current is flowing in designing using AVLS technique. Also power dissipation is very less here. Figure 3.1 shows the circuit of D- Flip flop designed using AVLS technique. Figure 3.2 shows the test circuit of D Flip-flop designed using AVLS Technique.

IV. SIMULATION RESULTS

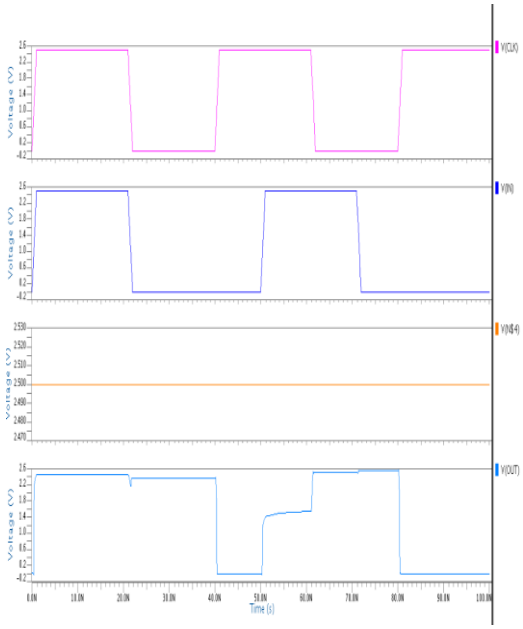

Figure 4.1 Simulation of D Flip-flop designed using AVLG technique

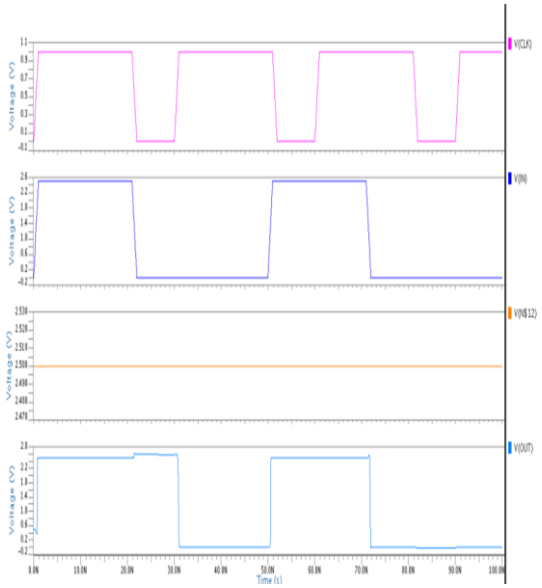

Figure 4.2 Simulation of D Flip-flop designed using AVLS technique

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Table 4.1: Power Analysis

Power Dissipation	AVLG Technique	AVLS Technique
	2.5729nwatts	1.3480nwatts

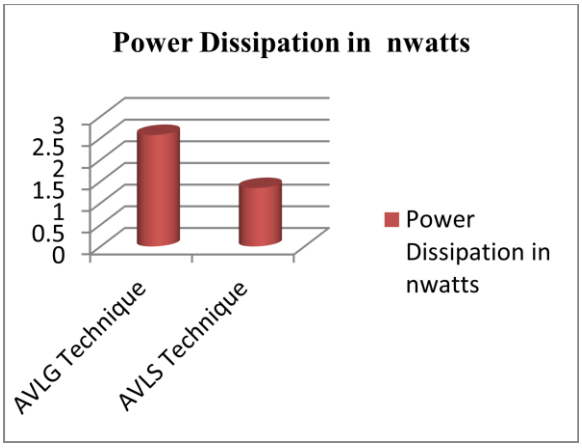

Fig 4.3 Power dissipation chart

V. CONCLUSION

The D Flip-flop is designed in Mentor Graphics 130nm technology. The Simulation results clearly explain the reduction in the power consumption by incorporated with AVL Technique that is either AVLG or AVLS Technique. The AVLS technique has less power dissipation 1.3480nwatts compared to AVLG technique 2.5729nwatts.

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BIOGRAPHY

Somashekhar Malipatil received his B.E degree in Electronics & Communication Engineering from Maharaja Institute of Technology, Mysore in the year 2011 and worked as a lecturer for a period of 2 years in polytechnic college from august 2011 to September 2013. Completed his M.Tech in VLSI Design & Embedded Systems from AIET, Kalaburagi in the year 2015. He presented one paper in international conference and two papers in national conference. He published 4 papers in international journals. His research interest includes Low Power VLSI Design and Advanced VLSI Design.