IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 11, November 2015

Realization of Synchronized Computation and Communication Using Penta MTJ Elements

A. Lakshminarayanan[1], V. Krishnakumar[2], N. Jayapal[3], R. Shankar [4], K. Shajudeen[5]

Assistant Professor, Dept of ECE, Kongunadu College of Engineering and Technology, Thottiyam[1, 2, 3, 4, 5]

Abstract: Advanced computing systems infix spintronic devices to boost the outflow performance of standard CMOS systems. High speed, low power, and infinite endurance area unit vital properties of magnetic tunnel junction (MTJ), a spintronic device that assures its use in reminiscences and logic circuits. This paper presents a Penta MTJ-based gate that provides simple cascading, self-referencing, less voltage headroom downside in pre charge sense electronic equipment and low space overhead contrary to existing MTJ-based gates. Penta MTJ is employed here as a result of it provides warranted disturbance free reading and inflated tolerance to method variations at the side of compatibility with CMOS method. The gate is valid by simulation at the 180 -nm technology in Cadence virtuoso.

Index Terms: Counter, magnetic logic gate, magnetic tunnel junction.

I. INTRODUCTION

The spin is used for storing data and therefore the charge for its process. it's the potential to interchange CMOS logic and memory [1]. In deep sub micrometer, scaling of CMOS causes the leak power to dominate over all alternative power parts [2]. Digital signals area unit pictured in typical CMOS logic by the presence or absence of electrical charge in terms of voltage VDD or ground. However, in spintronics, digital signals area unit pictured by up and down spin of negatron. In recent years, researchers have developed spintronic devices, like magnetic tunnel junctions (MTJs), that operates on the principle of tunnel magneto resistance (TMR) [3]. AN MTJ consists of 2 ferromagnetic layers separated by AN compound layer with the aptitude to boost the performance of CMOS logic circuit in terms of power dissipation, space needed, and interconnection delay [4]. Use of Penta MTJ in an exceedingly serial circuit is helpful.

II. LITERATURE SURVEY

Several kinds of logic gates victimization MTJ area unit according within the literature. the twin properties of MTJ, namely, process and storage, facilitate to cut back the memory and interconnect delay/power [5] required to store the processed knowledge back to memory.

Though according magnetic logic gates facilitate in reducing power and delay however they need several drawbacks. In [7], a magnetic XOR circuit comprising of six MTJs and transistors is bestowed. Its space demand is a smaller amount however because the range of MTJ will increase, the writing energy conjointly rises. this can be owing to the necessity of Constant VDD provide for nodes of spin-diode and run power dissipation in CMOS at the nano scale, severally, that may be a serious limitation of hybrid circuit consisting of MTJ and CMOS. In [8], the computer circuit would need further electronic equipment to convert the voltage signals to this signal of ample magnitude for writing the MTJ of the next stage resulting in a rise in delay, power consumption, and area. Lyle et al. [6] designed a computer circuit with just one output MTJ that may notice operation by choosing correct predetermined, i.e., initial state and operative voltage. Moreover, the author has enforced solely linear logic like NAND, NOR, and majority perform. If a nonlinear logic like two-input XOR/XNOR were to be enforced victimization NAND/NOR, severally, then the output would be obtained in 3 stages. Milton Friedman et al. [11] and Horowitz and Hill [9] planned a spin-diode logic family and CMOS computer circuit, severally, within which the static power dissipation was quite the writing power dissipation. Penta MTJ-based realization of digital circuits has several benefits. First, Penta MTJ-based magnetic logic gates don't need referencing circuit because of the presence of 2 fastened layers with opposite spin orientations (self-referencing) contrary to MTJ.

Second, no additional hardware is required for complementary outputs because of the presence of pre charge sense electronic equipment (PCSA) for sensing. Third, the output of a spintronic device is directly detected by the PCSA therefore there's no have to be compelled to initialize the state of the output MTJ for sensing.

The structure of the Penta MTJ which comprises of two pinned layers:

1) Top pinned layer (TPL) and
2) Bottom pinned layer (BPL).

This paper is organized into four sections. Section III describes the Penta MTJ and logic in memory architecture. Section IV covers the design of three basic logic gates and implementation of XOR/XNOR along with simulation result to validate its functionality. Section V discusses the cascading of logic gate with the help of a 3-bit Gray counter as an example and also its simulation results. Section VI computes the energy and delay in writing and sensing.

III. MEMORY MANAGEMENT LOGIC

The logic-in-memory design, shown in Fig. 3, consists of 3 parts: 1) PCSA for sensing the distinction between the 2

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 11, November 2015

states of resistance; 2) Penta MTJ logic; and 3) Penta MTJ writing cell. PCSA (as shown in Fig. 2) could be a dynamic logic circuit having 2 phases, namely, a pre charge section Associate in Nursingd an analysis section. The discharging of each branches of PCSA depends upon their relative resistances such the low-resistance branch discharges the output node capacitance earlier that cuts off the opposite branch owing to the cross-coupled PCSA structure. The low-resistance branch pulls down toward ground and also the high-resistance branch pulls up toward VDD.

During pre charging, CLK is low that disconnects the higher 0.5 from the lower 0.5, i.e., pre charging of PCSA at the time of writing results in less delay furthermore as improved style. Stacking and high process voltage-temperature (PVT) variations just in case of standard MTJ in deep sub micrometer cause severe resistance couple that may conjointly cause PCSA failure in MTJ/CMOS hybrid logic circuits.

IV. DESIGN O F THREE BASIC LOGIC GATES AND IMPLEMENTATION OF XOR/XNOR

Logic gates act as basic building blocks for each combinative and ordered circuit. The essential structure of Penta MTJ-based gate is split into 3 elements, and delineate in Section II. Fig shows the Penta MTJ-based XOR/XNOR logic gates. For various logic gates, totally different writing electronic equipment is needed however the sensing portion remains identical.

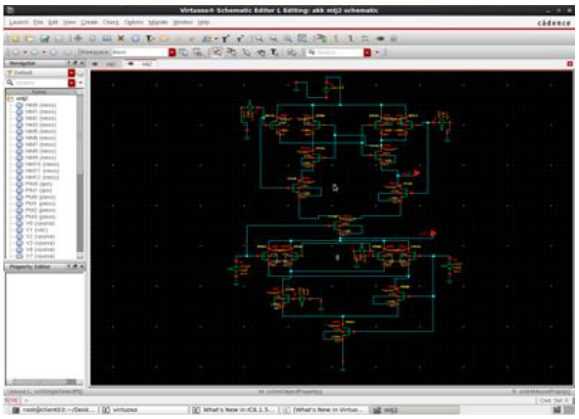

Fig 1.Xor/Xnor Logic

Fig 2 .Xor/Xnor Logic simulation result

Therefore, the knowledge is keep within the stapled layers mistreatment series or parallel mixtures of transistors as per the logic. Storing logic in Penta MTJ is intended such for storing one, all logic mixtures with high output square measure combined and therefore the web expression is evaluated mistreatment K-map and for storing zero, the complement of the expression is evaluated.

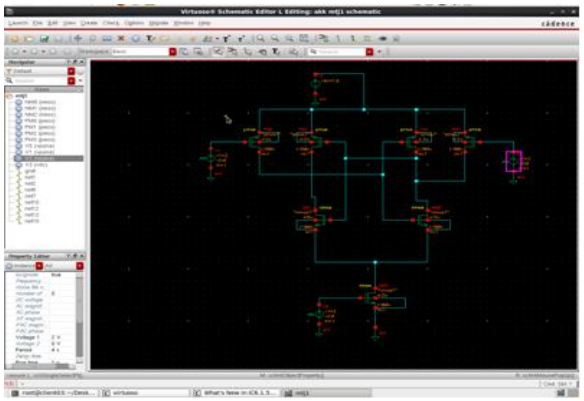

Fig 3.Logic Memory design

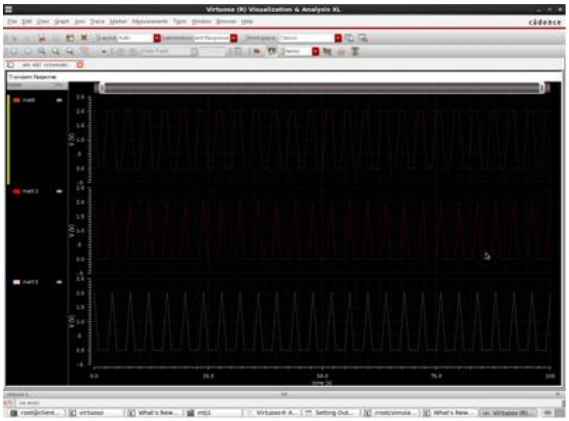

Fig 4 .Logic memory simulation result.

Fig2. Shows the simulation results of logic gates with each traditional and complementary output. A and B square measure the 2 inputs, zero output corresponds to the discharging of PCSA whereas one suggests that no discharging for traditional output. The analysis section begins once pre charging the outputs of the PCSA to VDD victimization the clock CLK.

V.CASCADING OF LOGIC GATE WITH 3-BIT GRAY COUNTER

Logic gates act as basic building blocks for each combinatory and successive circuits. the current state during a successive circuit like grey counter is hold on in flip-flops, that is extremely power overwhelming underneath standby condition. Use of

Penta MTJ during a successive circuit is useful as a result of just in case of unintentional closure.

The previous state is reconditioned from Penta MTJ inside few hundred picoseconds. Within the grey counter, PCSA is employed for sensing to get consecutive state, Penta MTJ for gift state storage and also the writing electronic equipment to assign consecutive state to the current state.

DOI 10.17148/IJARCCE.2015.41175

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 11, November 2015

For different logic gates, totally different writing electronic equipment is needed however the sensing portion remains identical. Therefore, the knowledge is hold on within the stapled layers exploitation series or parallel combos of transistors as per the logic. Storing logic in Penta MTJ is meant such for storing one, all logic combos with high output ar combined and also the web expression is evaluated exploitation K-map and for storing zero, the complement of the expression is evaluated.

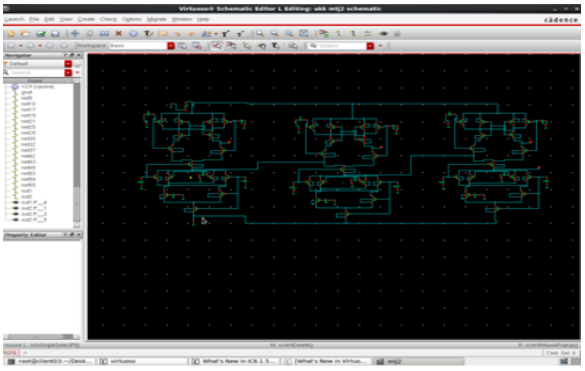

Fig5. Gray counter

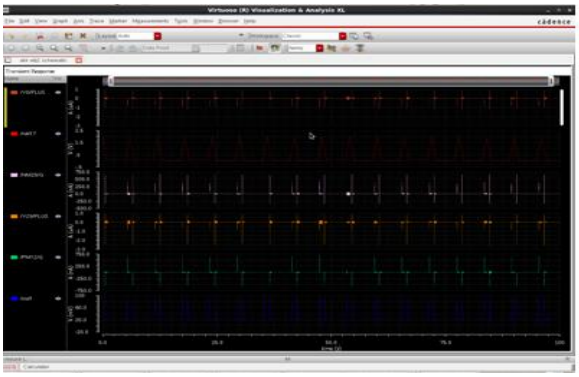

Fig 6 Gray counters simulation result

Figure shows the simulation results of logic gates with each traditional and complementary output. A and B square measure the 2 inputs, zero output corresponds to the discharging of PCSA whereas one suggests that no discharging for traditional output. The analysis part begins once pre charging the outputs of the PCSA to VDD mistreatment the clock CLK.

In this paper projected Penta MTJ-based grey counter, the change delay is assumed to be one.5 ns and also the writing energy is computed for this delay. The period of time of the clock for the grey counter is taken as two ns that correspond to a frequency of five hundred megacycles.

Table I Comparison table

Type	Power in mW	Transistor count	Writing & Sensing Delay in ns
MTJ-based gates	2.03343	14	12.39
Penta MTJ	1.09922	9	10.21

It can even be inferred from Table I that the Penta MTJ-based grey counter needs less range of transistors compared with MTJ-based grey counter owing to further writing electronic equipment demand just in case of MTJ. The sensing delay is a lot of within the planned gate owing to the presence of additional MN3 and MN4 transistors within the sensing path. However, these further transistors alter coincidental pre charging and economical writing that reduces errors.

VI. RESULTS AND DISCUSSION

The self referencing property of the Penta MTJ is helpful in decreasing the realm overhead as a result of its differential nature. The shift current density in PMA is directly proportional to the magnetization, property field, and also the thickness of the free layer. The thermal stability issue of Penta MTJ governs the information retention capability of the digital logic. The writing is completed per the previous state and, therefore, pre charging and writing aren't done at an equivalent time.

VII. CONCLUSION

The attractive options of Penta MTJ-based CMOS logic are low static power, short interconnect delay and effective power gating thanks to no volatility. Penta MTJ-based logic decreases the world overhead by removing the intermediate electronic equipment required for conversion of voltage to current or current to voltage. Penta MTJ conjointly provides secured disturbance free reading and inflated tolerance to method variations owing to its differential nature.

REFERENCES

[1] S. Parkin, X. Jiang, C. Kaiser, A. Panchula, K. Roche, and M. Samant, "Magnetically engineered spintronic sensors and memory," Proc. IEEE, vol. 91, no. 5, pp. 661–680, May 2003.

[2] S. A. Wolf et al., "Spintronics: A spin-based electronics vision for the future," Science, vol. 294, no. 5546, pp. 1488–1495, 2001.

[3] C. Chappert, A. Fert, and F. N. Van Dau, "The emergence of spin electronics in data storage," Nature Mater., vol. 6, no. 11, pp. 813–823, Nov. 2007.

[4] S. D. Pable and M. Hasan, "Interconnect design for subthreshold circuits," IEEE Trans. Nanotechnol., vol. 11, no. 3, pp. 633–639, May 2012.

[5] H.-P. Trinh, W. Zhao, J.-O. Klein, Y. Zhang, D. Ravelsona, and C. Chappert, "Magnetic adder based on racetrack memory," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 6, pp. 1469–1477, Jun. 2013.

[6] S. Lee, N. Kim, H. Yang, G. Lee, S. Lee, and H. Shin, "The 3-bit gray counter based on magnetic-tunnel-junction elements," IEEE Trans. Magn., vol. 43, no. 6, pp. 2677–2679, Jun. 2007.

[7] A. Lyle et al., "Magnetic tunnel junction logic architecture for realization of simultaneous computation and communication," IEEE Trans. Magn., vol. 47, no. 10, pp. 2970–2973, Oct. 2011.

[8] J. S. Friedman, N. Rangaraju, Y. I. Ismail, and B. W. Wessels, "A spin-diode logic family," IEEE Trans. Nanotechnol., vol. 11, no. 5, pp. 1026–1032, Sep. 2012

[9]M. K. Gupta and M. Hasan, "Design of high speed energy efficient masking error immune PentaMTJ based TCAM," IEEE Trans. Magn., no. 99.

[10] W. Xu, T. Zhang, and Y. Chen, "Design of spin-torque transfer magnetoresistive RAM and CAM/TCAM with high sensing and search speed," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 1, pp. 66–74, Jan. 2010.

[11] A. Makarov, V. Sverdlov, D. Osintsev, and S. Selberherr, "Fast switching in magnetic tunnel junctions with two pinned layers: Micromagnetic modeling," IEEE Trans. Magn., vol. 48, no. 4, pp. 1289–1292, Apr. 2012.