Design of Linear Feedback Shift Register using Reversible Logic

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Abstract: Reversible logic is playing an important role in research areas and has found its applications in low power CMOS VLSI, Nanotechnology and Quantum computation. Recently, several researchers have focused their efforts on the design and synthesis of efficient reversible logic circuits. LFSR's are attractive structures in the area of digital system testing and fault tolerant computing. In this work, we present designs of reversible LFSR using D flip flops with asynchronous set/reset. The comparison of proposed design is done in terms of the quantum cost, delay and garbage out puts. The important reversible gates used for Reversible logic design are Feynman gate, Fredkin gate, Toffoli gate, SAM gate etc.

Keywords: Low-power VLSI, Low-power CMOS design, reversible logic, LFSR.

1. INTRODUCTION

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. With the number of chip components doubling every 18 months, as per Moore's Law, the Irreversible Technologies would dissipate a lot of heat and reduce circuit life. It is here the Reversible Logic comes into action in not only recovering the lost information but also dissipating less heat. Landauers principle states that logic computations that are not reversible necessarily generates KT*log2 joules of heat energy for every bit of information that is lost, where k is the Boltzmann's constant and T is the absolute temperature at which the computation is performed. For room temperature T, the amount of dissipating heat is small (2.9x10-21 joules) but not negligible [1].

Bennett showed that KTln2 energy dissipation would not occur if computation is carried out in a reversible way [2]. In the year 1994 Shor [5] did a remarkable research work in creating an algorithm using reversibility for factorizing large number with better efficiency when compared to the classical computing theory. After this the work on reversible computing has been started by more people in different fields such as nanotechnology, quantum computers and CMOS VLSI.

Reversible logic is being considered as an alternative of traditional irreversible logic as reversible computing does not erase or lose any information hence the reversible logic has a theoretical potential to dissipate no energy. Reversible circuits are designed using reversible logic gates that have the same number of inputs and outputs and have one-to-one mapping between inputs and outputs; thus, the input states can be always reconstructed from the output states [7]. A gate (circuit) is reversible if it maps each input assignment to a unique output assignment, that is, if the mapping of inputs to outputs is bijective. Thus, the number of inputs and outputs in a reversible gate or circuit are equal. The N*N reversible gate can be represented as shown in Figure 1.
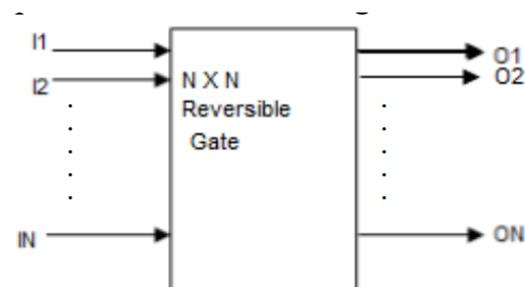
Figure 1

Recently, the design of reversible sequential circuits has also attracted the attention of researchers such as the work in [4, 9, 12, 13].

The paper is organized as follows: Section 2 presents the basic definitions related to reversible gates; Section 3 presents the basic reversible gates and their quantum representation; Section 4 presents the design of asynchronous set/reset D- FF using Fredkin Gates and SAM gates Section 5 presents the Design of LFSR using reversible logic and comparisons of the proposed designs; Section 6 presents the conclusions.

2. BASIC DEFINITIONS RELATED TO REVERSIBLE LOGIC

Definition 2.1: The function f(x1, x2 … xn) of n Boolean variables is called reversible if:
1. The number of outputs is equal to the number of inputs.
2. Any input pattern maps to a unique output pattern. In other words, the output of a reversible function is a permutation of the set of its inputs [14].

Definition 2.2: For an (n, k) function, i.e. function with n-input k-output, it is necessary to add inputs and/or outputs to make it reversible. "Garbage" is the number of outputs added to make an (n, k) function reversible. While the word "constant inputs" is used to denote the pre-set value

inputs that were added to an (n, k) function to make it reversible. The constant inputs are known as ancillary inputs[14].The relation between garbage outputs and constant inputs is

Input + constant input= output + garbage

Definition 2.3: Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1 [18].

Definition 2.4: The Delay of a Reversible Logic Gate is the maximum number of gates in a path from any input line to its corresponding output line.

3. BASIC REVERSIBLE LOGIC GATES

There are many number of reversible logic gates that exist at present. The quantum cost of each reversible logic gate is an important optimization parameter [16]. The quantum cost of a 1x1 reversible gate is assumed to be zero while the quantum cost of a 2x2 reversible logic gate is taken as unity. The quantum cost of other reversible gates is calculated by counting the number of V, V^+ and CNOT gates present in their circuit. V is the square root of NOT gate and V^+ is its Hermitian. The V and V^+ quantum gates have the following properties:

$$V * V = NOT \dots\dots\dots\dots\dots\dots (1)$$
$$V * V^+ = V^+ * V = 1 \dots\dots\dots\dots (2)$$
$$V^+ * V^+ = NOT \dots\dots\dots\dots\dots (3)$$

Some of the important reversible logic gates are
1) NOT Gate
The simplest Reversible gate is NOT gate and is a 1*1 gate [7]. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost.It is as shown in the Figure 3.1
Input Vector = A, Output Vector=A'

(a) Block diagram   (b) symbol
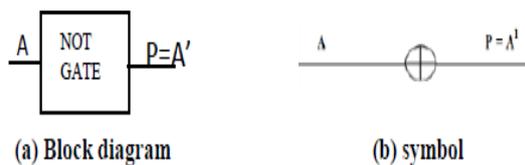
Figure 3.1

2) CNOT /Feynman Gate:
Feynman gate [17]is also known as controlled-not gate (CNOT). It is a 2*2 reversible gate with Quantum cost of 1. The CNOT or Feynman gate can be described as: Input Vector = (A, B) Output Vector=A XOR B
As shown in Figure 3.2

(a) Block diagram   (b) Quantum cost of CNOT/FEYNMAN Gate
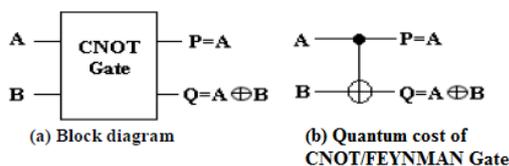
Figure 3.2

3) Double Feynman Gate:
The double Feynman gate is 3*3 reversible gate having inputs (A, B, C) and outputs P=A,Q=A XOR B, R=A XOR C with a quantum cost of 2[8]. The double Feynman can be described as:

(a) Double Feynman Gate   (b) Quantum Representation of Double Feynman Gate
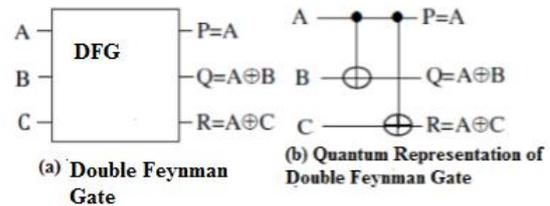
Figure 3.3

4) TOFFOLI Gate:
TOFFOLI gate which is a 3*3 reversible gate with inputs (A, B, C) and outputs P=A, Q=B, R=AB XOR C. It has Quantum cost five [5].

(a) Toffoli Gate   (b) Quantum Representation of Tofilli Gate
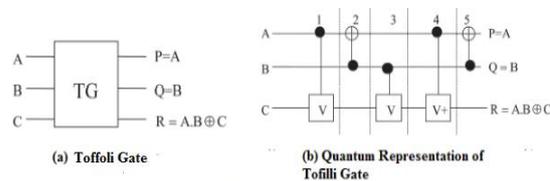
Figure 3.4

5) PERES Gate:
Peres gate which is a 3*3 reversible gate having inputs (A, B, C) and outputs P = A; Q = A XOR B; R = AB XOR C. It has Quantum cost four [6].

(a) Peres Gate   (b) Quantum implementation of Peres Gate
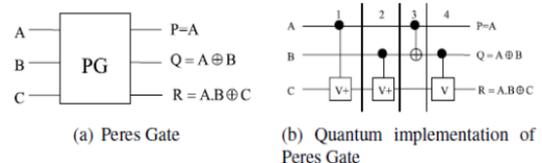
Figure 3.5

6) FREDKIN Gate:
Fredkin gate is a 3*3 reversible gate with inputs (A, B, C) and outputs P=A, Q=A'B+AC, R=AB+A'C. It has Quantum cost five [6].

(a) Fredkin Gate   (b) Quantum Representation of Fredkin Gate
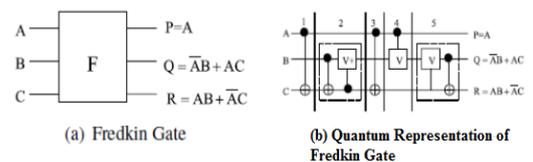
Figure 3.6

7) SAM Gate:
SAM gate is a 3*3 reversible gate with inputs A, B, C and outputs P=A', Q=A'B XOR AC', R=A'C XOR AB.The quantum cost of SAM gate is 4[3].

(a) SAM Gate   (b)Quantum Representation of SAM Gate
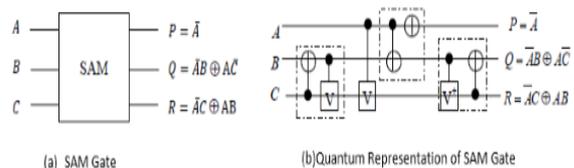
Figure 3.7

4. DESIGN OF MASTER SLAVE D FF WITH ASYNCHRONOUS SET/ RESET

4.1 The Master-Slave D FF with asynchronous Set/Reset using Fredkin and Feynman gates:
The characteristic equation of gated D flip-flop is **$Q=CLK'.Q +CLK.D$**. The D flip-flop can be realized by one Fredkin gate and one FG. It can be mapped with Fredkin gate by giving CLK, D and Q respectively in 1st, 2nd and 3rd inputs of Fredkin gate [18]. The D FF can be modified as master slave FF [18]. This is further modified with asynchronous Set/Reset as shown in figure 4.1. In this design the first two Fredkin gates with CLK,D inputs implement the logic for master slave FF. The Fredkin gate used in master latch is the positive enable reversible D Latch, and the Fredkin gate used in Slave latch is the negative enable reversible D Latch .The Fredkin gate with inputs C_1, C_2 is used to provide the asynchronous set and reset as proposed. The Fredkin gate can be used to avoid the fan out of a signal by assigning that signal to its input A and other two inputs B and C with the inputs B=0 and C=1 as shown in figure 4.2(a).

(b) Reversible asynchronous set/reset master-slave D flip-flop

Figure 4.1.1

(a) Application of the Fredkin gate to avoid the fanout

(b) Asynchronous reset of the Q and R outputs of the Fredkin gate

(c) Asynchronous set of the Q and R outputs of the Fredkin gate
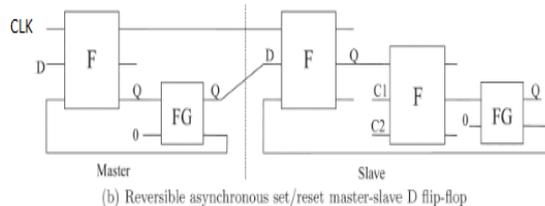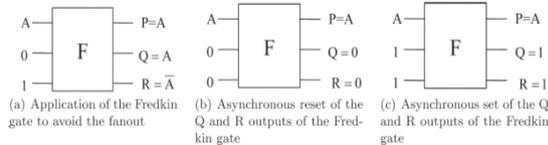
Figure 4.1.2

The Fredkin gate can be used to asynchronously reset its Q & R output's to 0 by assigning the values of 0 to inputs B and C as shown in figure 4.2(b).As shown in figure4.2(c) by assigning 1 to B and C inputs of Fredkin gate it can asynchronously set its Q and R output to 1.The quantum cost of the DFF with asynchronous set/reset discussed is 17. In our delay calculations, we use the logical depth as measure of the delay [Mohammadi and Eshghi 2009][11]. The delay of each 1x1 gate and 2×2 reversible gate is taken as unit delay called Δ. Any 3×3 reversible gate can be designed from 1×1 reversible gates and 2×2 reversible gates, such as CNOT gate, Controlled-V and Controlled-V^+gates. Thus, the delay of a 3×3 reversible gate can be computed by calculating its logical depth when it is designed from smaller 1×1 and 2×2 reversible gates [6],[10],[15]. The SAM gate, the Fredkin gate, Toffoli gate are the three major 3×3 reversible gates used in this work for designing the DFF circuits, thus in this section we calculate the delays of the Fredkin gate, SAM gate and Toffoli Gate. Based on the logical depth the delay of SAM gate is 4Δ, and Fredkin gate and Toffoli gate is 5Δ.The designed asynchronous D FF involves 3 Fredkin gates, 2

Feynman gates, so the delay is 17Δ.The number of garbage outputs for the proposed design are 5.The designed Master –Slave D FF with asynchronous Set/Reset can be represented with a symbol as shown in the figure 4.5(b).

4.2 The Master-Slave D FF with asynchronous Set/Reset from SAM, Toffoli and Feynman gates:
The characteristic equation of gated D flip flop can be realized by one SAM Gate and one Feynman Gate, where the inputs CLK, D, Q are mapped to 1st, 2nd and 3rd inputs of SAM gate [3]. The D FF is modified as Master Slave FF with asynchronous Set/Reset as shown in the Figure 4.2.1. In this design, the two SAM gates are used to provide the necessary logic for implementation of master slave logic and the Toffoli gate with inputs C_1, C_2 is used to provide the asynchronous set and reset, as described below. The Toffoli gate can be used to avoid the fan out of a signal by assigning that signal to its input B and other two inputs A and C with the inputs A=1 and C=0 as shown in figure 4.2.2(a)

Figure 4.2.1

(a) Appliction of Tofolli gate to avoid Fanout

(b) Asynchronous reset of the Q and R outputs of Tofolli gate

(c)Asynchronous set of Q and R outputs of Tofolli gate
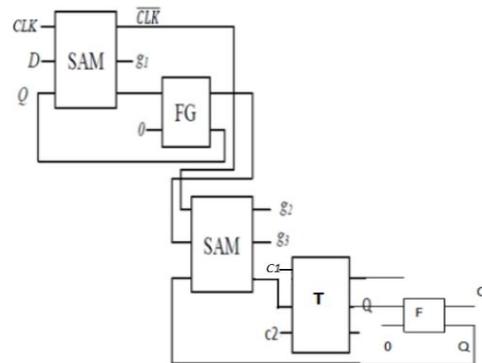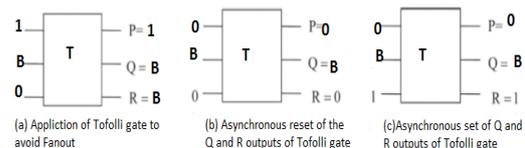
Figure 4.2.2

The Toffoli gate can be used to asynchronously reset its Q & R output's to 0 by assigning the values of 0 to inputs A and C as shown in figure 4.2.2(b). As shown in figure 4.2.2(c) by assigning 0 to A and 1to C inputs of Toffoli gate it can asynchronously set its R output to 1.The quantum cost of the DFF discussed is 15. The ,designed asynchronous D FF involves 2 SAM gates, 1 Toffoli gate, 2 Feynman gates, so taking the logical depth into consideration the delay is 15Δ . The number of garbage outputs for the proposed design is 5.The designed Master –Slave D FF with asynchronous Set/Reset can be represented with a symbol as shown in the figure 4.5(b)

(a)   (b)
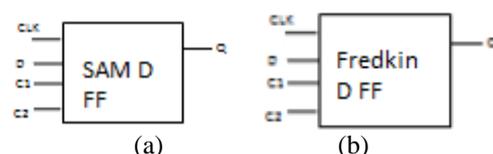
Figure 4.5

5. DESIGNING LFSR USING REVERSIBLE LOGIC

A linear feedback shift register (LFSR) consists of N registers connected together as a shift register. The input to the shift register comes from XOR of particular bits of the register. On reset, the registers must be initialized to a non-zero value. The LFSR is an example of a maximal length shift register because its output sequence through all 2^n-1 combinations (excluding all 0's).The inputs fed to the XOR are called the tap sequence and are often specified with a characteristic polynomial. We in this paper proposes two designs of 3 bit LFSRwith the characteristic polynomial $1+x^2+x^3$. LFSRs are used for high speed counters and Pseudo-random number generators. This pseudo random sequence are handy for built-in self-test and bit error rate testing in communication links. They are also used in many spread spectrum communications systems such as GPS and CDMA where their correlation properties make other users look like uncorrelated noise. The following table lists characteristic polynomials for some commonly used maximal length LFSR's

Characteristic Polynomials

N	Polynomial
3	$1+x^2+x^3$
4	$1+x^3+x^4$
5	$1+x^3+x^5$
6	$1+x^5+x^6$
7	$1+x^6+x^7$
8	$1+x+x^6+x^7+x^8$
9	$1+x^5+x^9$

Table 5.1

The proposed design of LFSR is shown in the figure 5.1. The design uses D FF's and Feynman gate. The designed LFSR in the first proposal use Master Slave D FF with asynchronous Set/Reset designed from Fredkin gates and Feynman gates as proposed in the section 4.1 named as Fredkin D FF. The designed LFSR for the second proposal make use of Master Slave D FF with asynchronous Set/Reset designed from SAM gates, Toffoli gates and Feynman gates as proposed in the section 4.2 named as SAM D FF. In both the designs Feynman gate is used to avoid fan-out.

The Feynman gates are used to overcome fan-out for CLK and output Q0, Q1, Q2.The values provided to the inputs C1, C2force the FF's to either set or Reset condition. . On reset, the Flip Flop's must be initialized to a non-zero value. If all the 3 FF's are set to 1 i.e., Q0Q1Q2=111 then designed LFSR will go through the count as shown in the table 5.2. The proposed two designs are compared in terms of quantum cost, delay and garbage outputs as shown in table 5.3 and 5.4.

LFSR Sequence

Cycle	Q0	Q1	Q2
0	1	1	1
1	0	1	1
2	0	0	1
3	1	0	0
4	0	1	0
5	1	0	1
6	1	1	0
7	1	1	1
Repeats forever			

Table 5.2

A comparison of Master Slave D FF with asynchronous Set/Reset

Proposed design	Quantum cost	Delay	Garbage Output
Fredkin gate based	17	17	5
SAM gate based	15	15	5

Table 5.3

A comparison of 3 bit LFSR of the characteristic polynomial$1+x^2+x^3$

Proposed design	Quantum cost	Delay	Garbage Output
Fredkin gate based	58	58	16
SAM gate based	52	52	16

Table 5.4

The proposed circuit can be used as a Pseudo random bit sequence generator where Q2 is considered as the output from the circuit, in this case the Feynman gates used to avoid fan out of Q0 and Q1 can be removed. The sequence generator is shown in the figure 5.2. The output Q2 follows the sequence 1110010 for the example considered earlier.

The 3-Bit LFSR with Characteristic polynomial $1+x^2+x^3$
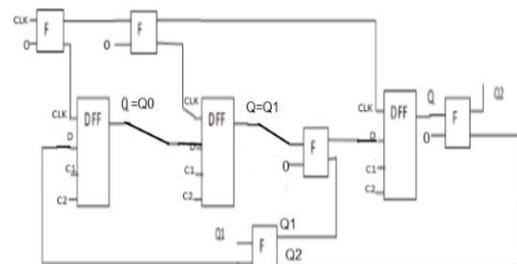
Figure 5.1

Pseudo-random bit sequence generator

Figure 5.2

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6. CONCLUSION

In this work, we have presented novel designs of reversible D FF with asynchronous set/reset which are optimized in terms of quantum cost, delay and garbage outputs. We conclude that the choice of reversible gates and the design approach to carefully select a reversible gate for implementing a particular logic function will significantly impact the quantum cost, delay and garbage outputs of the reversible design. The application of these FF's as LFSR is designed and discussed. The application of LFSR as pseudo random bit sequence generator is proposed .Further advancement of the proposed work is to use the proposed D FF's towards the designs of complex reversible sequential circuits such as FSM.

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