IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

*International Journal of Advanced Research in Computer and Communication Engineering*
*Vol. 5, Issue 4, April 2016*

# A Fast 16x16 Vedic Multiplier Using Carry Select Adder on FPGA

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**Abstract***:* Vedic mathematics is one of the ancient Indian system of mathematics that was rediscovered in the early twentieth century This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance using Carry select adders. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. In Vedic Mathematics calculation based on 16 sutras is a unique technique of calculations . This paper presents design and implementation of high speed 16x16 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like addition and shifting . Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra for 16x16 bits multiplication and carry select adder is simulated and implemented on XilinxISE9.2i.

**Keywords:** Ripple Carry (RC) Adder, Vedic Mathematics, Vedic Multiplier (VM), Urdhava Tiryakbhyam Sutra, Carry select adder, Verilog HDL.

## I. INTRODUCTION

Multiplication is an fundamental function in arithmetic operations based on this operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing(DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit.

[1]. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications.

Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents different multiplier architectures.

In this paper a simple 16 bit digital multiplier is proposed which is based on Urdhva Tiryakbhyam (Vertically & Crosswise) Sutra of the Vedic Math's. Two binary numbers (16-bit each) are multiplied with this Sutra. The main concept of this paper is that the speed of propagation and decrease in delay of the conventional architecture. This paper is organized as follows.

Section II describes basic methodology of Vedic multiplication technique. Section III describes the proposed methodology of Vedic multiplication technique with Carry select adders. Section IV describes the design and implementation of Vedic multiplier module by using XilinxISE9.2i. Section V comprises of Result and Discussion in which device utilization summary and computational path delay obtained for the proposed Vedic multiplier (after synthesis) is discussed. Finally Section VI comprises of Conclusion

## II. VEDIC MULTIPLICATION TECHNIQUE

The use of Vedic mathematics is to reduce the typical calculations in conventional mathematics to very simple one. Because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

The proposed Vedic multiplier is based on the "Urdhva Tiryagbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since

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the partial products and their sums are calculated in parallel and the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

*A. Vedic Multiplier for 2X2 bit Module*

The method is explained below for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Fig. 2.1. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

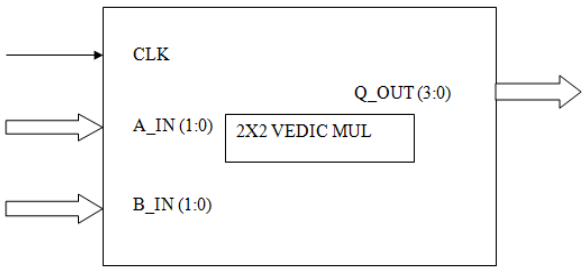


Fig. 2.1 Block diagram of 2X2 Vedic Multiplier

Let's take two inputs, each of 2 bits; say A1A0 and B1B0. Since output can be of four digits, say Q3Q2Q1Q0. As per basic method of multiplication, result is obtained after getting partial product and doing addition.

A1 A0
X B1 B0
---
A1B0 A0B0
A1B1 A0B1
---
Q3 Q2 Q1 Q0

In Vedic method, Q0 is vertical product of bit A0 and B0, Q1 is addition of crosswise bit multiplication i.e. A1 & B0 and A0 and B1, and Q2 is again vertical product of bits A1 and B1 with the carry generated, if any, from the previous addition during Q1. Q3 output is nothing but carry generated during Q2 calculation. This module is known as 2x2 multiplier block [5,6,7].

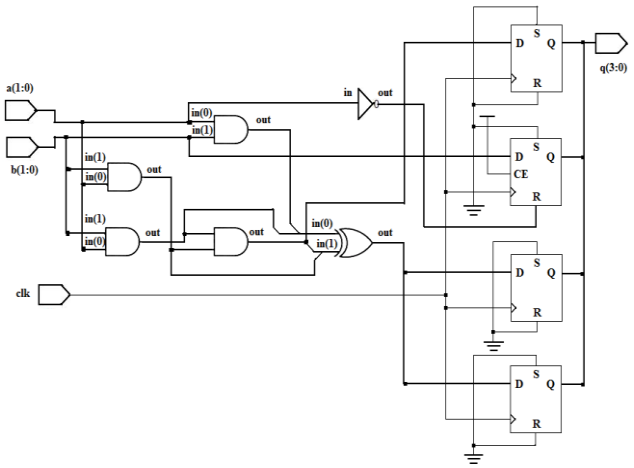


Fig. 2.2 RTL model of 2X2 Vedic Multiplier

*B. Vedic Multiplier for 4X4 bit Module*

For higher no. of bits in input, little modification is required. Divide the no. of bit in the inputs equally in two parts.

Let's analyze 4x4 multiplications, say A3A2A1A0 and B3B2B1B0. Following are the output line for the multiplication result, Q7Q6Q5Q4Q3Q2Q1Q0. Block diagram of 4x4 Vedic Multiplier is given in fig 2.3.

Let's divide A and B into two parts, say A3 A2 & A1 A0 for A and B3B2 & B1B0 for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block,

A3A2 A1A0
X B3B2 B1B0
---

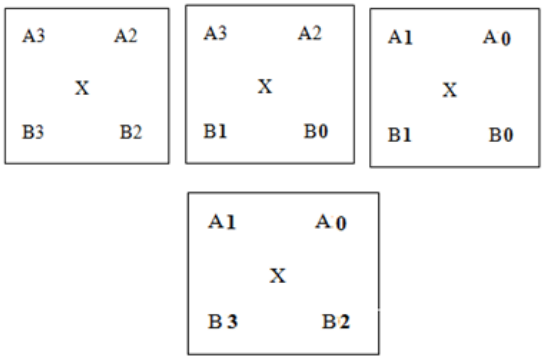


Fig. 2.3 Algorithm of 4x4 bit Vedic Multiplier

Each block as shown above is 2x2 bits multiplier. First 2x2 multiplier inputs are A1 A0 and B1 B0.The last block is 2x2 multiplier with inputs A3 A2 and B3 B2.

The middle one shows two, 2x2 bits multiplier with inputs A3A2 & B1B0 and A1A0 & B3B2. So the final result of multiplication, which is of 8 bit, Q7Q6Q5Q4Q3Q2Q1Q0.

The 4x 4 bit multiplier is structured using 2X2 bit blocks as shown in figure 2.4.

IJARCCE
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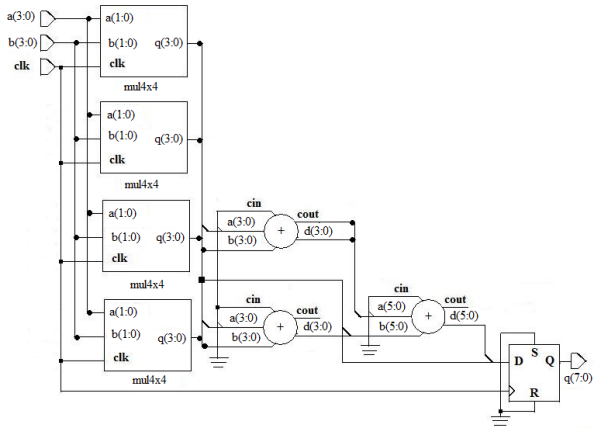


Fig. 2.4: RTL View of 4x4 Bit Vedic Multiplier by ModelSim

*C. Implementation of 8x8 bits Vedic Multiplier*

The 8x 8 bit multiplier is structured using 4X4 bit blocks as shown in figure 2.5. In this figure the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

$$P= A \times B= (AH-AL) \times (BH-BL)$$
$$= AH \times BH+AH \times BL + AL \times BH+ AL \times BL$$

The outputs of 4X4 bit multipliers are added accordingly to obtain the final product. Thus, in the final stage two adders are also required [10,12].

Now the basic building block of 8x8 bits Vedic multiplier is 4x4 bits multiplier which implemented in its structural model. For bigger multiplier implementation like 8x8 bits multiplier the 4x4 bits multiplier units has been used as components which are P= A x B= (AH-AL) x (BH-BL)
= AH x BH+AH x BL + AL x BH+ AL x BL

The outputs of 4X4 bit multipliers are added accordingly to obtain the final product. Thus, in the final stage two adders are also required [11,12].

The structural modelling of any design shows fastest design.

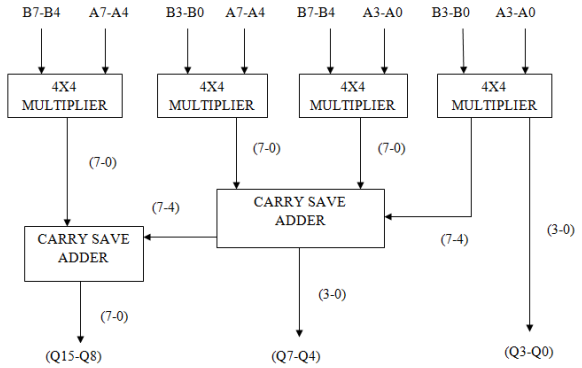


Fig.2.5 8X8 Bits decomposed Vedic Multiplier

*D. Implementation of 16x16 bits Vedic Multiplier*

The 16X16 bit multiplier structured using 8X8 bits blocks as shown in Fig. 2.6. The 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL.

The outputs of 8X8 bit multipliers are added accordingly to obtain the 32 bits final product.

Thus, in the final stage two adders are also required [12]. The structure of 16X16 is again obtained from the decomposition of 8X8 vedic multiplier.

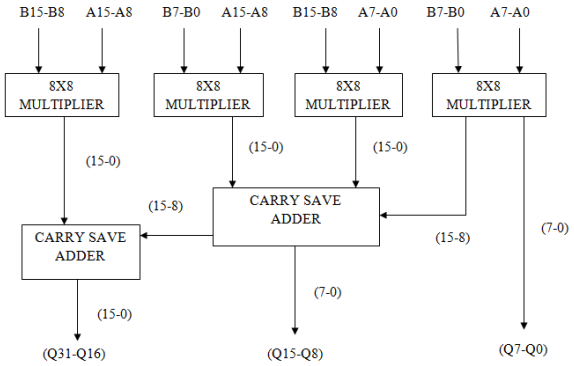


Fig. 2.6 16x16 Bits decomposed Vedic Multiplier

## III. VEDIC MULTIPLICATION USING CARRY SELECT ADDER

The vedic multiplier requires 4 bit, 6 bit , 12 bit, 16 bit , 24 bit adders at each stage of 2X2, 4X4, 8X8 and 16x16 multiplication. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.

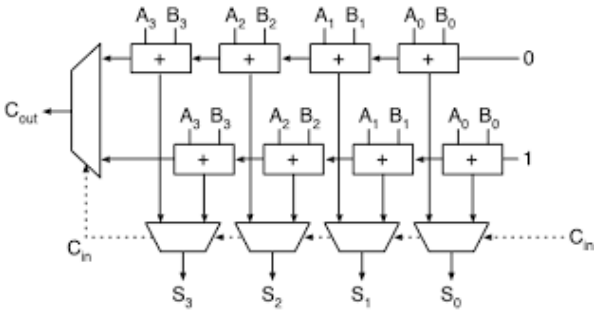


Fig. 3.1 4 bit Carry Select Adder

The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs for a block size of $\lfloor\sqrt{n}\rfloor$. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The $O(\sqrt{n})$ delay is derived from uniform sizing, where the ideal number of full-adder elements per block is

IJARCCE

ISSN (Online) 2278-1021
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equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

In this paper we propose a 16X16 vedic multiplier using carry select adders as its one of the basic component. This will reduce the area in FPGA and also improve the performance in terms of speed. It will be verified by comparing it will hardwired unsigned multiplier.

## IV. DESIGN AND IMPLEMENTATION OF 16X16 VEDIC MULTIPLIER USING CARRY SELECT ADDER

The 16X16 multiplier is implemented and simulation results were tested in XilinxISE9.1i and ModelSim inbuilt simulator.

Implementation and simulation of its decomposed 8X8, 4X4, 2X2 and carry select adder is also done in XilinxISE9.1i.

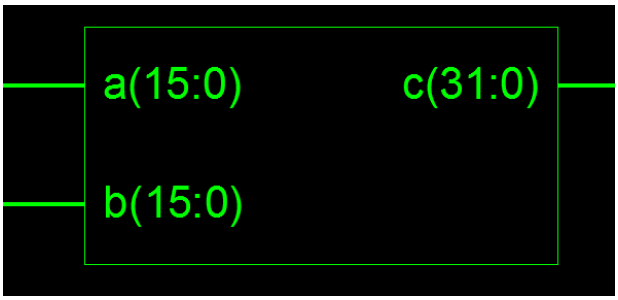


Fig.4.1 16X16vedic multiplier RTL view

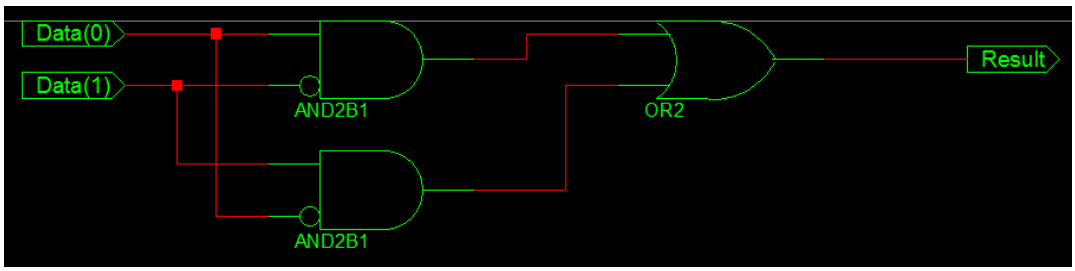


Fig.4.2 16X16vedic multiplier components (a)

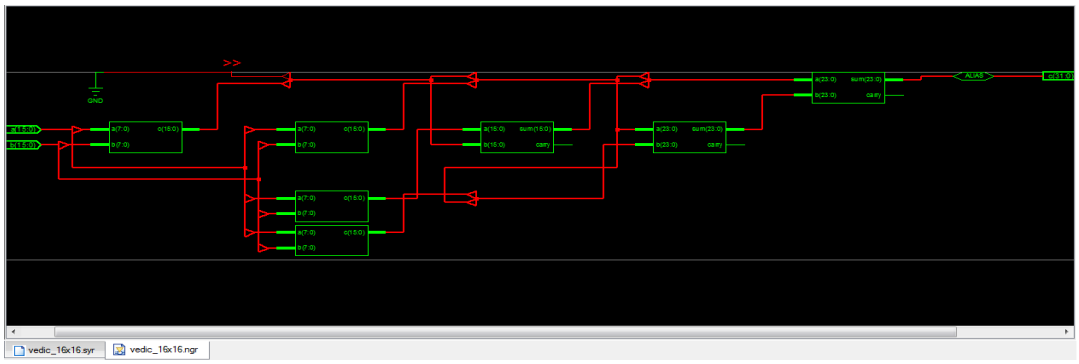

Fig.4.3 16X16vedic multiplier components (c)

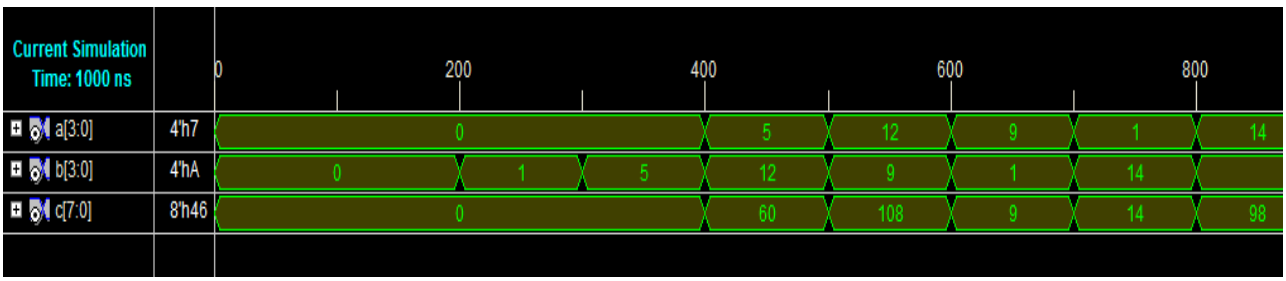


Fig.4.4 4X4vedic multiplier simulation result1

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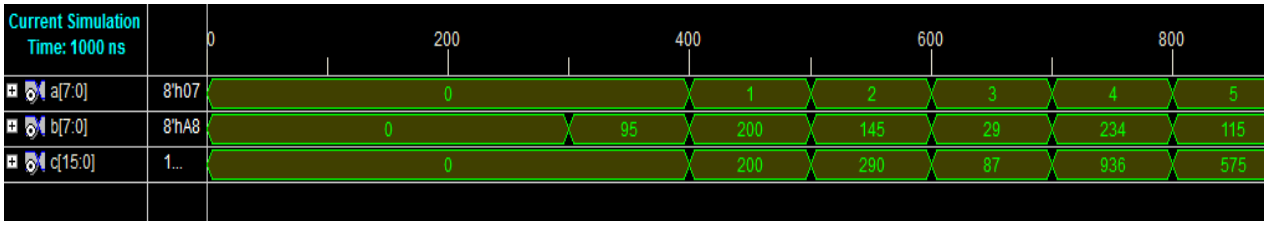


Fig.4.5 8X8vedic multiplier simulation result2

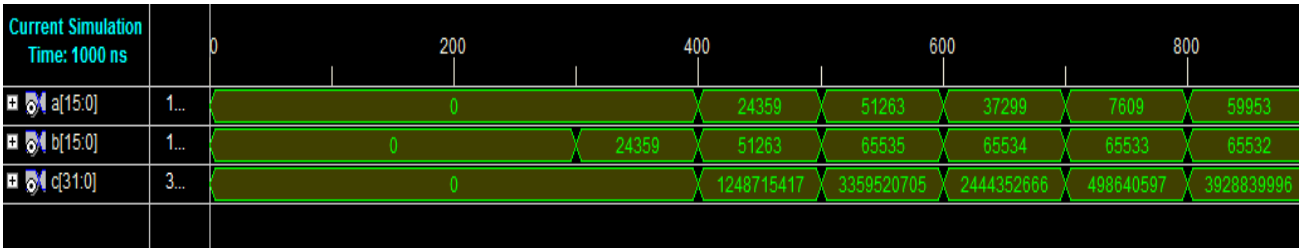


Fig.4.6 16X16vedic multiplier simulation result3

## V. RESULT AND DISCUSSION

Simulation of 16X16 vedic multiplier using carry select adder shows a large reduction in area and better performance in terms of speed. The area delay product is also reduced but it is greater than a normal udhrava tribhakayam multiplier due the fact that redundancy in the adder section is increased.

TABLE I: COMPARISON OF DIFFERENT MULTIPLIERS PERFORMANCE IN TERMS OF AREA AND SPEED

| Type of multiplier | Speed / delay in ns | Area in terms of slices(LUT Buffer,register) | Area delay product |
|---|---|---|---|
| **Hardwired multiplier** | 110ns | 1372 | 150920 |
| **Vedic Multiplier** | 98ns | 854 | 83692 |
| **Vedic multiplier with carry select adder** | 88ns | 1240 | 109120 |

## VI. CONCLUSION AND FUTURE WORK

The designs of 16x16 bits Vedic multiplier have been implemented on Spartan XC3S500-5-FG320 and XC3S1600-5-FG484 device. The computation delay for 16x16 bits Hardwired multiplier was 110 ns and for 16x16 bits Vedic multiplier was 96 ns. The proposed vedic multiplier with carry select adder has a delay of 88 ns only. It is therefore seen that the Vedic multipliers are much more faster than the conventional multipliers. The algorithms of Vedic mathematics are much more efficient than of conventional mathematics.

Vedic Mathematics, developed about 2500 years ago, gives us a clue of symmetric computation. If all those methods effectively implement hardware, it will reduce the computational speed drastically. Therefore, it could be possible to implement a complete ALU using all these methods using Vedic mathematics methods.

Vedic mathematics is long been known but has not been implemented in the DSP and ADSP processors employing large number of multiplications in calculating the various transforms like FFTs and the IFFTs. By using these ancient Indian Vedic mathematics methods world can achieve new heights of performance and quality for the cutting edge technology devices.

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