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Analytical Study of Multipliers for High Speed Applications

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Abstract: Convolution is having wide area of application in Digital Signal Processing. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Convolution and deconvolution is central to many applications of Digital Signal Processing and Image Processing. Primary requirement of any application to work fast is that increase the speed of their basic building block. Multiplier is the heart of convolution. It is most important but, slowest unit of the system and consumes much time in the system. Many methods are invented to improve the speed of the multiplier, amongst all vedic multiplier is under focus because of faster working and low power consumption. In this project we have implemented the high speed convolution system using vedic mathematics.

Keywords: Convolution, Vedic Mathematics, VHDL.

I. INTRODUCTION

The ancient system of Vedic Mathematics was re-introduced to the world by Swami Bharati Krishna Tirthaji Maharaj, Shan-karacharya of Goverdhan Peath. "Vedic Mathematics" was the name given by him. Bharati Krishna, who was himself a scholar of Sanskrit, Mathematics, History and Philosophy, was able to reconstruct the mathematics of the Vedas. According to his re-search all of mathematics is based on sixteen Sutras, or word-formulae and thirteen sub-sutras. Vedic mathematics reduces the complexity in calculations that exist in conventional mathematics. Generally there are sixteen sutras available in Vedic mathematics.

The power of Vedic mathematics is not only confined to its simplicity, regularity, but also it is logical. Vedic mathematics' logics and steps can be directly applied to problems involving trigonometric functions, plane and sphere geometry, conics, differential calculus, integral calculus and applied mathematics of various kind.

The advantage of Vedic mathematics lies in the fact that it simplifies the complicated looking calculations in conventional mathematics to a simple one in a much faster and efficient manner. This is attributed to the fact that the Vedic formulae are claimed to be based on the "natural principles on which the human mind works". Hence this presents some effective algorithms which can be applied to various branches of engineering

Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application. In this paper the sutra's which is used for the multiplication i.e Urdhva Triyakbhyam Sutra. Array multiplier is also taken which is to compare the results between Vedic and conventional multipliers. The results are compared in terms of delay. Vedic multipliers are to be the best compared to conventional ones as we know that from the earlier.

II. RELATED WORK

Surabhi Jain, SandeepSaini [1] proposed a paper on direct method of computing the discrete linear convolution, circular convolution and deconvolution. The approach is easy to learn because of the similarities to computing the multiplication of two numbers. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on ancient Indian Vedic mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The results show that the implementation of linear convolution and circular convolution using Vedic mathematics is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures. According to Mrs. Rashmi Rahul Kulkarni [2], convolution is carried out by serial processing. They used only one 4×4 bit Vedic multiplier based on UrdhvaTiryagbhyam sutra. Though hardware is less, delay is more as sixteen multiplications are carried out one by one using only single multiplier. In this paper, convolution of two finite length sequences is computed using direct method. This method is similar to the multiplication of two decimal numbers, this similarity that makes this method easy to learn and quick to compute. As Vedic multiplier is high speed multiplier among existing multipliers, UrdhvaTiryagbhyam algorithm from Vedic mathematics is used for 4×4 bit multiplication and to improve speed parallel processing approach is used.G. Ramanjaneya Reddy and A. Srinivasulu [3] presented convolution process using hardware computing and implementations of discrete linear convolution of two finite length sequences (NXN). This implementation method is realized by simplifying the

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convolution building blocks. The purpose of this analysis is to prove the feasibility of an FPGA that performs a convolution on an acquired image in real time. The proposed implementation uses a changed hierarchical design approach, which efficiently and accurately quickens computation. The efficiency of the proposed convolution circuit is tested by embedding it during a prime level FPGA. It additionally provides the required modularity, expandability, and regularity to form different convolutions. This particular model has the advantage of being fine-tuned for signal processing; in this case it uses the mean squared error measurement and objective measures of enhancement to achieve a more effective signal processing model. They have coded their design using the Verilog hardware description language and have synthesized it for FPGA products using ISE, Modelsim and DC compiler for other processor usage.MadhuraTilak [4], presented a novel method of implementing linear convolution of two finite length sequences (N×N) in hardware using hardware description language (VHDL). In this paper, an optimized design for linear convolution is presented. This design model has advantage of fine tuning depending on the requirement for enhancing the signal processing model. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches using XILLINX software. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches. The proposed circuit is also modular, expandable and regular which provides flexibility. The proposed system design is coded using VHDL language and synthesized for FPGA products with XILLINX 13.1 software.

III. PROPOSED WORK

A. Convolution:

Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combining two signals to obtain a third signal. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Convolution is an operation which takes two functions as input, and produces a single function output (much like addition or multiplication of functions).Consider two finite length sequences x(n) and h(n) on which the convolution operation is to be performed.

$$y(n) = x(n) * h(n) \quad (1)$$

$$y[n] = \sum_{k=-\infty}^{\infty} x(k)h(n-k) \quad (2)$$

B. Block Diagram:

A block diagram of proposed system is shown in Figure 2. It consists of multiplier based on Vedic sutra i.e.Urdhva-Tiryagbhyam that is embedded into convolution of two finite sequences. System block diagram is shown in Figure 2. Primary requirement of any application to work fast is that increase the speed of their basic building block. Multiplier is the heart of convolutionand it is most important but, slowest unit of the system and consumes much time in the system. Many methods are invented to improve the speed of the Multiplier, amongst all Vedic Multiplier is under focus because, of faster working and low power consumption. In this project the speed of Convolution module is improved using Vedic multiplier. It consists of multiplier based on Vedic sutra i.e. URDHVA Tiryagbhyam that are embedded into convolution of two finite sequence.

C. Conventional Multiplier:

An array multiplier is a digital combinational circuit that is used for the multiplication of two binarynumbers by employing an array of full adders and half adders. This array is used for the nearly simultaneous addition of the various product terms involved. To form the various product terms, an array of AND gates is used before the Adder array. To clarify more on the concept, let us consider a 4×4 bit multiplication with A and B being the multiplicand and the multiplier respectively. Assuming A = (1 0 0 1) and B= (1 0 1 0), the various bits of the final product can be written as:-

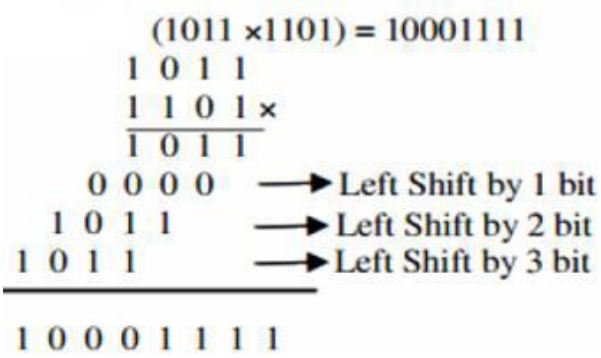

Fig.1: Example of conventional multiplier

For the above multiplication, an array of sixteen AND gates is required to form the various product terms and an Adder array is required to calculate the sums involving the various product terms and carry combinations in order to get the final Product bits.

The Hardware requirement for an m x n bit array multiplier is given as:-

(m x n) AND gates,
(m-1).n Adders in which n HA(Half Adders) and
(m-2).n FA(full adders).

Here from the above example it is inferred that partial products are generated sequentially, which reduces the speed of the multiplier. However the structure of the multiplier is regular.Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this multiplier is less economical.

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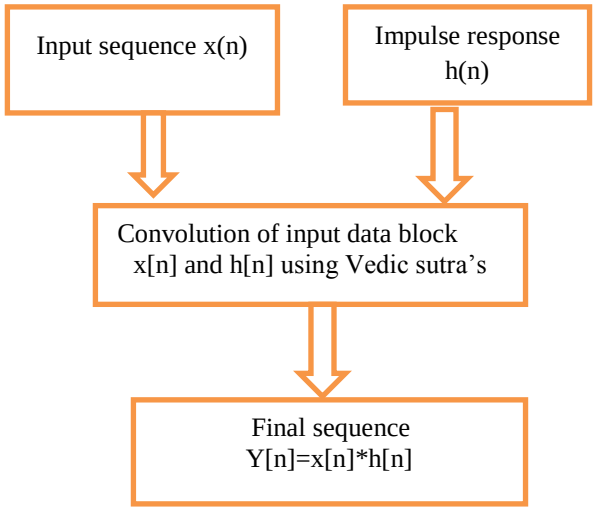

Fig.2: System Block Diagram

Consider 4x4 multiplications, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for this multiplication is P7 P6 P5P4P3P2 P1 P0. Using the fundamental of Array Multiplication, taking partial product addition is carried out in Carry save form; we can have the following structure for multiplication as shown in Figure 3.

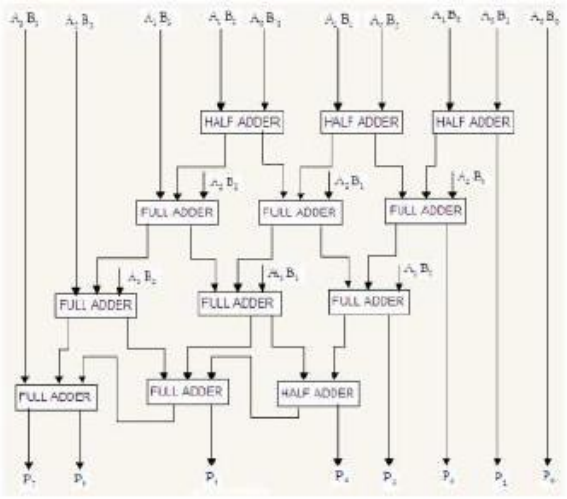

Fig.3: Structure for conventional multiplier

UrdhvaTiryagbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures.Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient.

D. Vedic Multiplier:

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness JagadguruShankaracharyaBharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. The sutras and sub-sutras were reintroduced to the world by Swami Bharati Krishna Tirthaji Maharaja in the form of book Vedic M Ancient Indian.

The work presented here, makes use of Vedic Mathematics. "UrdhvaTiryagbhyam Sutra" or "Vertically and Crosswise Algorithm" of Vedic mathematics for multiplication is used to develop digital multiplier architecture. The multiplication of two 4 bit number using UrdhvaTiryagbhyam is shown in figure 4.

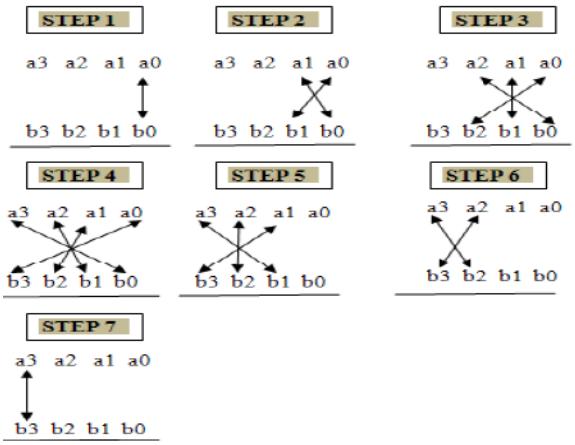

Fig.4: Multiplication of two 4 bit numbers using UrdhvaTiryagbhyam method

Thus, the product terms can be calculated as

A1=a0*b0
A2=a0*b1+a1*b0+prevcarry
A3=a0*b2+a1*b1+a2*b0+prevcarry
A4=a0*b3+a1*b2+a2*b1+a3*b0+prevcarry
A5=a1*b3+a2*b2+a3*b1+prevcarry
A6=a2*b3+a3*b2 + prevcarry
A7=a3*b3+ prevcarry

After comparative study of conventional multipliers and Vedic multiplier, UrdhvaTiryagbhyam sutra is shown to be an efficient multiplication algorithm.Therefore we are using Vedic multiplier in convolution system to improve its performance.

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E. Proposed Convolution:

The linear convolution of x(n) and h(n) is y(n) = f(n) * g(n). This can be solved by several methods, resulting in the sequence y(n). In this approach for calculating the convolution sum is set up like multiplication (except carries are not performed out of a column).where the convolution of x(n) and h(n) is performed. To get convolution of two sequences, where each sequence consist of 4 samples, sixteen partial products are calculated and afterwards they are added to get convolution sequence y[n]. In this paper, Partial products are calculated by using Vedic multiplier based on UrdhvaTiryagbhyam algorithm. Here to minimize hardware, width of each input sample is restricted to 4 bit. Hence maximum possible input sample value would be (1111)2 or (15)10 or (F) h. Multiplier required is 4×4 bit. Each multiplier gives 8 bit long partial product. Convolution outputs y[6] and y[0] are direct Partial products. While remaining obtained after addition of intermediate partial products.

Let two discrete length sequences are x[n] and h[n].Where x[n] = {x3 x2 x1 x0} and h[n] = {h3 h2 h1 h0} are convolved. As each sample is four bit long ,each partial product is eight bit long e.g. x0h0, x3h0, x3h3 all are eight bit long. y[n] = x[n] * h[n], in a wayasmentioned above. Procedure is rearranged as shown in figure 5.

x[n]			x3	x2	x1	x0
	×					
h[n]			h3	h2	h1	h0
			x3h0	x2h0	x1h0	x0h0
		x3h1	x2h1	x1h1	x0h1	
	x3h2	x2h2	x1h2	x0h2		
x3h3	x2h3	x1h3	x0h3			
Y6	Y5	Y4	Y3	Y2	Y1	Y0

Fig.5: Convolution of x[n] and h[n]

In propose system to generate sixteen partial products, sixteen vedic multipliers are used and to perform further operations of addition, all the outputs are latched as shown in figure.6.

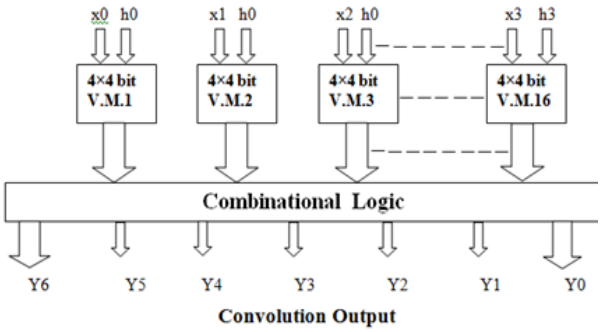

Fig.6: Block Diagram for convolution

As shown in figure 6, 4 bit long samples are applied to 4X4 bit Vedic multipliers (V.M.).Output of each Vedic multiplier is 8 bit long partial product. Vedic multiplier uses UrdhvaTiryagbhyam algorithm for multiplication. In parallel processing, to generate sixteen partial products, sixteen Vedic multipliers are used to boost speed. To perform further operation of addition, all outputs are latched. And corresponding output Y0, Y1, Y2, Y3, Y4, Y5 and Y6 are produced. Maximum possible length of Y0 and Y6 is 8 bit, while of Y1 toY5 is 9 bit. The design is built in VHDL.

IV. RESULT & DISCUSSION

This chapter presents the test environment and the experimental results of design modules. The objectives of this project are to design the Vedic multiplier architecture in convolution to improve speed performance. The design is implemented in VHDL, simulated using Xilinx.

A. Simulation of Convolution:

The multiplier is simulated on Xilinx simulator. The figure 7 shows the simulation result of multiplier. a and b are the inputs of 4 bit each and prod gives multiplication result.

The simulated result of conventional multiplier is shown below

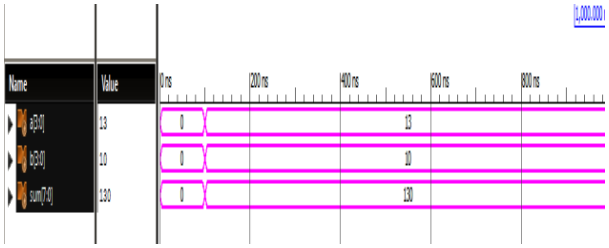

Fig. 7: Simulation of multiplier

The Vedic multiplier is simulated on Xilinx simulator. The figure 8 shows the simulation result of Vedic multiplier. a and b are the inputs of 4 bit each and prod gives multiplication result based on urdhva- tiryagbhyam.

The simulated result of Vedic multiplier is shown below

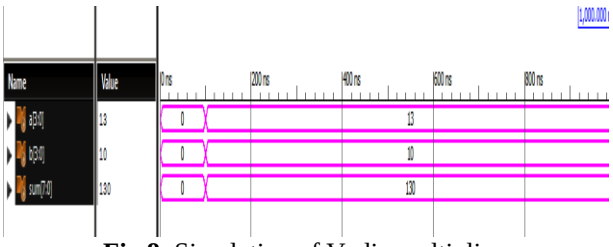

Fig.8: Simulation of Vedic multiplier

The Convolution module is simulated on Xilinx simulator. The figure 9 shows the simulation result of Convolution module using Vedic Mathematics.

The simulated result of Convolution using Vedic Multiplier is shown below.

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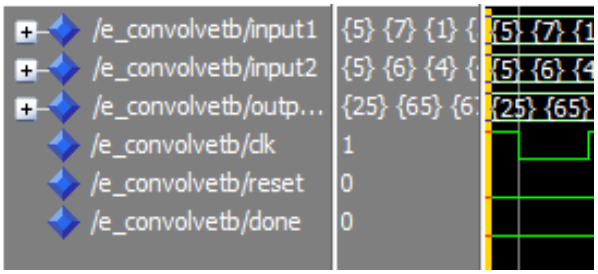

Fig.9: Simulation of Convolution

Method	Delay
Conventional Multiplier	17.544ns
Proposed Vedic Multiplier	9.585ns

V. APPLICATION

- The main application of such system is in digital image processing as convolution plays an important role in many algorithms in edge detection and related processes.
- Speeding up convolution and deconvolution using a Hardware Description Language for design entry not only increases (improves) the level of abstraction, but also opens new possibilities for using programmable devices.

VI. CONCLUSION

The propose system provides a method for calculating the linear convolution with the help of Vedic algorithms that is easy to learn and perform. It presents faster implementation of linear convolution. The execution time required for propose convolution using Vedic multiplication algorithm compare with that of conventional convolution with the simple multiplication is less from the simulated result.

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