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A Comparative Analysis of Variable Partitioned Adder

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Abstract: In high speed VLSI applications adders play important role. According to conventional studies much research is done on various parameters like delay, area, and power. Considering recent scenario optimization of all parameters is needed, this gives rise to idea of hybrid systems. Thus two new hybrid carry select adders are studied involving the Carry Select and Section Carry based Carry Lookahead sub adders. In this paper comparative study of 32bit Hybrid carry select adder is proposed involving variable input bit partitioning resulting in optimized delay. Performance of proposed designs is studied under Verilog HDL and subsequently implemented in a FPGA (Spartan-3E). The results obtained show that the carry select adder utilizing section-carry based carry lookahead logic with (8-8-8-8) input bit partitioning encounters minimum data path delay.

Keywords: Carry select adder, input partitioning, Verilog, FPGA.

1. INTRODUCTION

Adder is the basic building block of every arithmetic and logical operations. There are various types of adder already exist i.e Ripple carry adder(RCA),Carry lookahead adder(CLA),Carry select adder(CSLA),Carry save adder(CSA) and so on. So there is need to concentrate on the various performance parameter of adder such as speed, area, power and delay. Among all these adders CSLA provides the good compromise between low area occupancy of RCA and High speed performance of CLA. This is the only reason that we are focusing on CSLA. Also Carry select adder (CSLA) belongs to the family of high speed square-root time adders. Carry select adders are realized using the following:

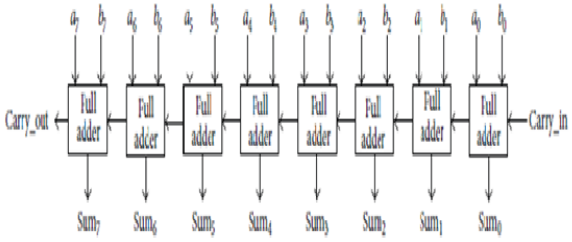
a. Full adders and 2 : 1 multiplexers.
b. Full adders, binary to excess 1 code converters, and 2 : 1 multiplexers
c. Sharing of common Boolean logic.

Carry select adder is classified as Homogeneous and Heterogeneous CSLA. It has been widely implemented using the following topologies and computational elements:

a. Conventional CSLA
b. CSLA with Binary to excess converter. (BEC)
c. CSLA based on common Boolean logic (CBL) sharing
d. Hybrid CSLA and CLA structures
e. Hybrid CSLA and CLA including BECs

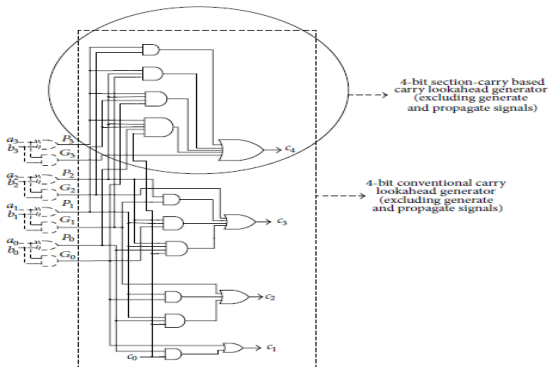
Ripple Carry Adder (RCA)

Multiple full adder circuit can be cascaded in parallel to add N-bit number. It is a logic circuit in which the carry out of each full adder is the carry in of the succeeding next full adder. As carry bits get rippled it is called as ripple carry adder. The carry generated from each full adder is given to next full adder and so on. Hence, the carry is propagated in a serial computation. Hence, delay is more as the number of bits is increased in RCA.



a) 8- bit RCA [1]

Carry Look Ahead Adder (CLA)



b) 4-Bit Conventional & Section Carry Based Carry Lookahead Adder[1]

Carry lookahead adder solves the carry delay problem by calculating the carry signals in advance based on input signal. Therefore CLA is faster than RCA. Carry look ahead adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate in the generation and propagation stage. Carry logic block gets very complicated for more than 4-bits. Section-carry based CLAs (SCBCLAs) were proposed as an alternative to conventional CLAs for a 32-bit addition operation, the SCBCLA was found to exhibit reduced

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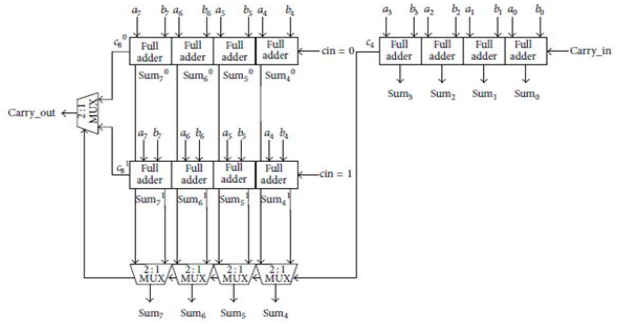
propagation delay than the conventional CLA by 15.2%. In conventional CLA all the four carries generated by carry logic block are used but in Section-carry based CLAs (SCBCLAs) only the last carry i.e C_4 generated by CLB is used for sum generation. As in SCBCLA the concentration is only on last carry generated so propogation delay of SCBCLA gets reduced than conventional CLA.

Carry Select Adder (CSLA)



c) 8-bit conventional CSLA comprising full adders and 2:1 MUXes (CSLA type)[1]

The carry select adder generally consist of two RCA and multiplexer. Here the input partitioning is used i.e. the least significant 4- bits were generated using RCA method and MSB 4- bits using CSLA. The carry generated by 4-bits RCA is served as select input for mux. As two RCA were used for MSB 4-bits the sum will be generated on basis of carry input selected. Carry Select Adder (CSLA) architecture consists of independent generation of sum and carry i.e., Cin=1 and Cin=0 are executed parallely. Depending upon Cin, the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the sum will be selected. Hence, the delay is reduced.

2. PROPOSED WORK

The proposed work consist of implementation of 32 bit Hybrid CSLA with input bit partitioning technique. CSLAs can be implemented on the basis of uniform or non-uniform primary input partitions; accordingly they are labeled as "uniform" or "non-uniform". "Input partitioning" basically means splitting up of the primary inputs into groups of inputs so as to pave the way for addition to be done in parallel within the partitions; Referring to Figure 1, it can be seen that 32 bit inputs have been split into four uniform groups of 8-input pairs; thus it can be said that the 32-bit CSLA is realized according to a 8-8-8-8 input partition. 32-bit hybrid CSLAs incorporating a SCBCLA in the first 8- least significant stage with inputs ($a_0b_0 - a_7b_7$) producing the requisite sum as ($sum_0 - sum_7$) followed by Carry select Adder block with next stage of least significant bits(a8b8-a15b15). SCBCLA blocks constitute three functional blocks: propagate generate logic, look ahead carry generator, and the sum producing logic. The SCBCLA, the sum producing logic consists of full adders and an XOR gate, with the XOR gate providing the sum of the primary inputs a_7,b_7 and c_7. While rippling of carries occurs internally within the carry-propagate adder constituting the SCBCLA and producing the requisite sums, the lookahead carry signal corresponding to an adder section is generated independently (in parallel) and serves as the lookahead carry input for the successive CSLA stage.Similarly, above processes is repeated for the remaining 16 input bits.

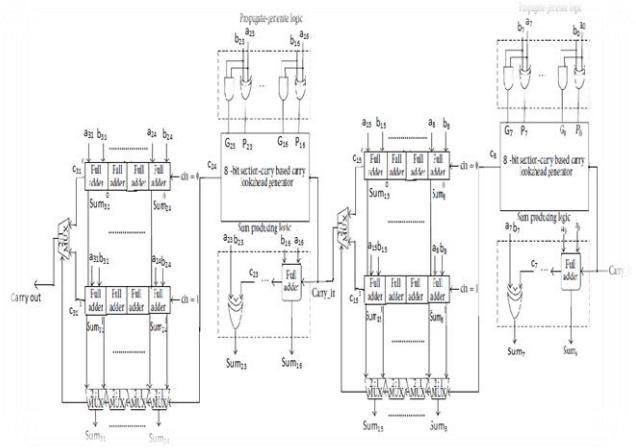


FIGURE 1: 32-Bit hybrid CSLA with 8-8-8-8 bit input partitioning

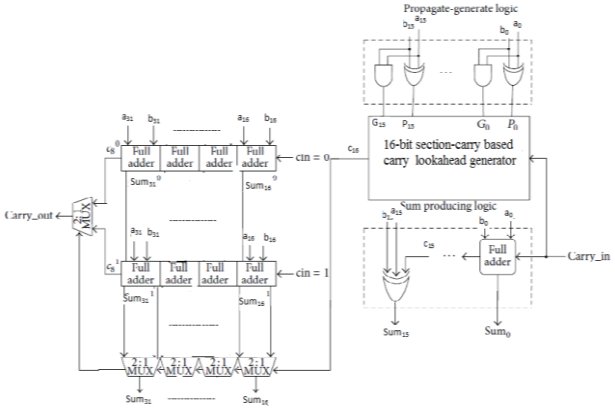


FIGURE 2: 32-Bit hybrid CSLA with -16 bit SCBCLA in the least significant stage

32-Bit hybrid CSLA as shown above with input bit partitioning of 16-16 is also implemented. least significant 16 bits are provided to SCBCLA block which in terms provides carries which are propagated to CSLA block.

3. RESULTS

Verilog HDL modules of 32 bit hybrid CSLAs corresponding to two different input partitioning were described and implemented in Xilinx ISE Design Suite. The maximum combinational path delay has been estimated ascertained from the design summary.Results after synthesis and place and route for 8-8-8-8 input partitioning for CSLA-SCBCSLA was found to be 15.979ns (10.980ns logic, 4.999ns route) (68.7% logic, 31.3% route) And for 16-16 input partitioning it was found to be 37.405ns (23.695ns logic, 13.710ns route) (63.3% logic, 36.7% route).

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Table: Comparison of Adders for Delay

Input partition	Adder	Delay (ns)
8-8-8-8	CSLA-SCBCSLA [1]	17.897
	Proposed CSLA- SCBCSLA	15.979
16-16	CSLA-SCBCSLA [1]	21.097
	Proposed CSLA-SCBCSLA	23.695

4. CONCLUSION

CSLA is an important member of the high-speed adder family. In this paper, new hybrid CSLA topologies was put forward: carry selectcum-section-carry based carry lookahead adder (CSLASCBCLA). The speed performances of the corresponding CSLA structures have been analysed based on the studies of 32-bit dual-operand additions. Uniform input data partitions were considered for the proposed CSLA implementations and FPGA-based synthesis was performed. It has been found for dual-operand additions; the proposed CSLA- SCBCLA architecture is faster. From the inferences derived through this work, it is likely that the proposed hybrid CSLA architectures of bit partitioning (8-8-8-8) results in lesser critical path delay over (16-16) input partitioning technique.

REFERENCES

1. V. Kokilavani,1 K. Preethi,1 and P. Balasubramanian "FPGA-Based Synthesis of High-Speed Hybrid Carry Select Adders" Hindawi Publishing Corporation Advances in Electronic Volume 2015, Article ID 713843.
2. Ms. S.Manjui, Mr. V. Sornagopae" An Efficient SQRT Architecture of Carry Select Adder Design by Common Boolean Logic." 2013 IEEE
3. V. Kokilavani, P. Balasubramanian, and H. R. Arabnia, "FPGA realization of hybrid carry select-cum-section-carry based carry lookahead adders," in *Proceedings of the 12th International Conference on Embedded Systems and Applications*, pp. 81–85,2014.
4. B. Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," *IEEE Transactions on VLSI Systems*, vol. 20, no. 2, pp. 371–375, 2012.
5. I.-C.Wey, C.-C.Ho, Y.-S. Lin, and C.-C. Peng, "An area-efficient carry select adder design by sharing the common boolean logic term," in *Proceedings of the International MultiConference of Engineers and Computer Scientists (IMECS '12)*, vol. 2, pp. 1091–1094, March 2012.
6. Y. Wang, C. Pai, and X. Song, "The design of hybrid carrylookahead/ carry-select adders," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, no. 1, pp. 16–24, 2002.
7. G.A. Ruiz, "New static multi-output carry lookahead CMOS adders," *IEE Proc. Circuits, Devices and Systems*, vol. 144, no. 6, pp. 350-354, 1997.
8. J.B. Kuo, H.J. Liao, H.P. Chen, "A BiCMOS dynamic carry lookahead adder circuit for VLSI implementation of high-speed arithmetic unit," *IEEE J. of Solid-State Circuits*, vol. 28, no. 3, pp. 375-378, 1993.
9. C.-C. Wang *et al*., "A low power high-speed 8-bit pipelining CLA design using dual-threshold voltage domino logic," *IEEE Trans. On VLSI Systems*, vol. 16, no. 5, pp. 594-598, 2008.
10. G. Yang *et al*., "A 32-bit carry lookahead adder using dual-path all-N logic," *IEEE Trans. on VLSI Systems*, vol. 13, no. 8, pp. 992-996, 2005.
11. R. Zlatanovici, S. Kao, B. Nikolic, "Energy-delay optimization of 64- bit carry-lookahead adders with a 240ps 90nm CMOS design example," *IEEE J. of Solid-State Circuits*, vol. 44, no. 2, pp. 569-583, 2009.
12. A.Blotti, R. Saletti, "Ultra low-power adiabatic circuit semi-custom design," *IEEE Trans. on VLSI Systems*, vol. 12, no. 11, pp. 1248-1253, 2004.

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