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Design Approach to Realise SoC to Generate "Time Stamping Signal" from Satellites and Updating on Ethernet for Synchronization

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Abstract: The objective of this research paper is to design a "System-On-Chip (SoC)" having required modules/functional blocks in a single chip to generate accurate timing signal, derived from the satellites (GPS) signals, these are called "Timing Systems". The timing signal is distributed over Ethernet network using protocols like Serial, IRIG, NTP etc for time stamping, time updation & to use for synchronization of systems. The satellites (GPS) signals are generally from GPS / GLONASS / GALILEO satellites constellation. The satellite signals are received and through the process of triangulation precise position of the receiver and thereby accurate time information is derived. In the absence of signals from the GPS satellites, the time updation process continues with a local clock source built with in the SoC.

Keywords: SoC, FPGA, GPS, NTP, IRIGB, Ethernet, TGL, PTP, IP Core, Acquisition, Tracking.

I. INTRODUCTION

Timing systems are devices which generate a precise reference signals primarily for Time Stamping applications. The reference input is generally signals from GPS / GLONASS / GALILEO satellites constellation. The satellite signals are received and precise position of the receiver and thereby accurate time information is derived. In the absence of signals from the satellites, the time updation process continues with a local clock source with a defined accuracy. The derived time is distributed over a Ethernet network using protocols like Serial, IRIG, NTP etc.

All the systems / devices on a Ethernet network can get synchronized to this common time reference. Once all systems are time synchronized, it becomes easier to run a variety of time critical applications like event logging, fault analysis, time display, access control, data communication etc. Typical areas of use are Military and Aerospace for radar signals synchronization, launch operations, Electronic Warfare, Industrial applications like Power plants for failure analysis, weather monitoring, data logging and smart grid, also for commercial applications like displays, access control etc.

II. GLOBAL POSITIONING SYSTEM (GPS)

GPS is a constellation of 36 satellites in 6 orbits. With 6 satellites per orbit, at any time 4 satellites will be active and 2 satellites as spare per orbit, 24 satellites will be active all the time transmitting their instantaneous position to the earth. GPS receivers located on the earth acquire signals from these satellites continuously and using the principle of triangulation compute the co ordinates of the location and the time information. The current position & time info along with an accurate pulse signal appearing every second are output from the receiver for further use.

III. SOC FUNDAMENTALS

SOC, SOPC, PSOC, ASIC, ASSP and FPGA are the jargons in use while referring to any complex function implementation on a single silicon die. SOC primarily means that all the functions of a system being available on a single silicon chip. SOPC and PSoC mean the same and are SOCs whose functionality is user programmable. All micro controllers fall into this category to start with. Whereas ASIC (Application Specific Integrated Circuit) and ASSP (Application Specific Standard Package) too can be put under the category of SOC depending on whether a micro controller is part of it or not.

With FPGA densities on the rise all the time (now at 20 million gates) and also mixed signal FPGAs hitting the market, FPGAs have become the defacto device to be labeled as SOC. Apart from abundant logic blocks available for any complex algorithm implementation, hard core blocks like PLL, memories (Flash, RAM implementable as FIFO, SRAM, DPRAM), ADCs, DACs, communication engines like UARTs, I2C, SPI, CAN bus, USB, Ethernet etc and Controllers (ARM, Power PC) , Serializers / Deserializers make FPGA the ideal device for implementing SOC.

Ethernet details:
Ethernet is the dominant standard for commercial local area networking, with a vast ecosystem of operating systems and application software. Gigabit Ethernet derives from 10 and 100 Mbps Ethernet.

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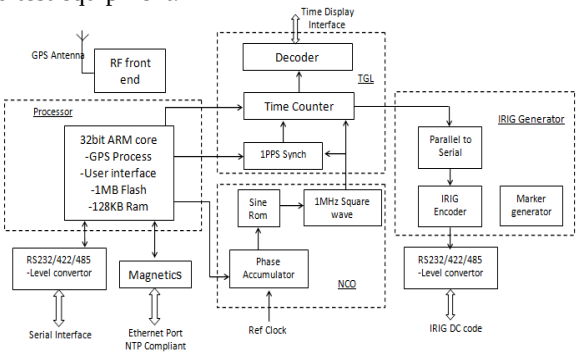
A major ingredient in Ethernet's success is its simplicity, which enables low cost implementations for the lower layers' hardware, with higher-level functions typically mechanized by processor software. As the result of its success, Ethernet is used in offices, factories, personal computers, and medical applications. This enables Ethernet users to be able to leverage a vast COTS ecosystem of network interfaces and switches, cables, connectors, operating system stacks, application software, and test equipment.



Design Approach:

The Timing systems basically derive Time information from the GPC satellites and process to generate the Timing signals to upload onto Ethernet for various applications. The fundamental blocks of the timing system are GPS receiver signal processing, time extraction &updation, generation of back up clock reference, Encoding and conversion to standard protocol formats for time distribution & synchronization. The design proposal is to discuss the implementation of all the timing blocks in a single SoC with external interfaces devices like Ethernet, Serial convertors etc. The following block diagram explains the interfaces between the major blocks. The SoC is basically a FPGA having IP Cores

GPS Receiver:

The first element in a GPS receiver is the RF front end consisting of Antenna, LNA, Down Conversion & Baseband signal extraction. These parts being mainly RF related will be implemented off the chip. Rest of the processing will be done on the FPGA. Once the GPS signal is conditioned properly for digitization, an Analog-to-Digital Converter (ADC) on chip, samples the signal and provides digital samples for further baseband digital signal processing.

The baseband signal processing elements of a GPS receiver are the removal of both the C/A code (Despreading) and the carrier frequency (Down conversion) to extract the data message. Upon obtaining the data message, the detection of the preamble is performed and the beginning of the subframe is obtained. The required baseband signal processing is divided into 3 separate, sequential functions: Acquisition, Tracking, and Navigational message decoding and processing. Acquisition is a coarse synchronization process used to acquire the signal for removing code phase and Doppler Effect.

Tracking is the next step carried out to remove code and carrier frequency, this is a fine synchronization process. At last data processing is done to recovery the GPS data.

The major blocks of GPS Receiver are listed below, which will be implemented in the software ported on FPGA.

Acquisition:

Acquisition is the process by which the receiver determines the satellites are in view such that it can track them and begin to navigate. To track the transmitted signal, the receiver must remove the carrier frequency and C/A code. It is used to identify the satellites for the users and determine the coarse values of the carrier frequency and the code phase of the signal

Tracking:

Satellites constantly move in the orbit. Hence the distance between the transmitter and receiver vary a lot. Hence once if the signal is acquired, the tracking must be started by synchronization method of locally generated carrier and locally generated code. The tracking is running continuously to follow the changes in frequency as a function of time. If the receiver loses track of a satellite, a new acquisition must be performed for that particular satellite.

Two types of tracking methods are,

a) **Code tracking :** The code tracking method is to generate an exact code replica and it is correlated with the incoming signal.

b) **Carrier tracking:**To demodulate the navigation data successfully, an exact carrier wave replica has to be generated. To track a carrier wave signal, phase lock loops (PLL) or frequency lock loop (FLL) are often used.

Data processing

After removing carrier and PRN code (gold codes) the remaining bits are given as data. The data is divided into frames. An entire frame is transmitted within 30 seconds. Each sub frame starts with 30-bit telemetry word (TLM). The TLM word consists of 22 preamble bits it is followed by telemetry message and ended up with parity bits. The receiver considers the preamble data to determine the start of sub frame. Sub frame provides the ephemeris data (satellite orbital position), satellite constellation information, atmospheric modeling parameters (for correcting positioning errors) and almanac data of long term coarse satellite orbital parameters. From the data output the following results are obtained :

- Date information.
- Time information
- Position of satellites is determined.

All the sub blocks of GPS Rx are implemented through an 32 bit ARM11 soft core implemented on the FPGA. The date and time information along with an 1PPS reference tick signal are fed to the time generation logic block

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Time Generation Logic (TGL) :-
This block consists of the following sub blocks,

Time counter
This is primarily a BCD counter of 54 bits which can accommodate time of the year with micro seconds resolution. The time of the year as extracted from the GPS receiver is loaded into the counter chain at the occurrence of 1PPS time tick. The time generated is also read back by the ARM11 controller for distributing over a serial interface in a proprietry format and over Ethernet port using IEEE standard NTP protocol. In the absence of GPS signals, the time updation is maintained by a locally generated accurate clock signal from NCO.

Display Decoder
It decodes the BCD time into a code suitable for displaying on 7 segment displays.

Numerically Controlled Oscillator (NCO) :-
NCO works on the principle of Direct Digital Synthesis (DDS). The basic blocks are a phase accumulator, a sine ROM and a square wave generator. An external clock source of 10MHz is used as input to phase accumulator which is basically a binary counter which is configured to over flow after reaching a preset terminal count which corresponds to a complete sine wave cycle. The sine ROM is essentially memory in which the address is the phase input and data is sine. As the counter traverses from minimum to maximum, the ROM o/p is a digitized sinusoidal signal with 8 bit resolution at the required frequency of 1MHz. The square wave generator is a digital comparator with inputs from the Sine ROM and a preset thresh hold. The o/p is a 1MHz square wave signal which is fed to the time generation logic as clock.

IRIG Generator:-
IRIG stands for Inter Range Instrumentation Group, a standard for distribution of time info in serial bit form over a campus network. Typical application areas are Military and Aero space (Launch sites) and Power Generation stations. Depending on the time resolution and frequency of transmission, it is categorized into A,B,D,E and G. Also the signal can be a digital or Analog - modulated by a 1KHz, 10Kz and 100 KHz sine wave. In the current application only DC implementation is done. The input to this block is a parallel BCD time along with strobe clocks. The parallel time is converted to serial at a rate decided by the standard A,B, D, E and G. This is selectable from external inputs. To aid in recovery / decoding of this serial time info , marker signals are added/ inserted every 10 bits. Then the entire serial binary time stream is pulse width modulated as below :-

a. A logic zero is represented by a pulse with duty cycle of 20% (20% period ON and 80% period OFF)
b. A logic one is represented by a pulse with duty cycle of 50% (50% period ON and 50% period OFF)
c. A marker is represented by a pulse with duty cycle of 80% (80% period ON and 20% period OFF)

The PWM serial time info is further level translated external to the FPGA and is made available for distribution.

Utilization of FPGA resources:-
All the major blocks were implemented in Xilinx Spartan 3AN series FPGA (700K gate, 13,248 logic cells,). The individual blocks were implemented, checked for their functionality and integrated to realize the entire system. Following is the breakup of logic resource utilization:

#	Block	Logic Cells used	Memory bits used	Remarks
1	GPS Receiver, ARM11 core, memory	4850	64K	RAM bits used
2	Time Generation Logic	138	NIL	
3	NCO	1100	4K	RAM bits used
4	IRIG	96	NIL	
5	Total	6184	68K	

CONCLUSIONS

In the present application the time reference generation is restricted to only IRIG and NTP formats. The same can be enhanced for PTP over Ethernet, USB and other interfaces.

REFERENCES

[1]. Mr.PhilippeCoussy, Mr.AdelBaganne, Mr.Eric Martin"A Design Methodology for Integrating IP into SoC Systems"University de Bretagne – France
[2]. Mr.AmirHekmatpour, Mr.RobertDevins, Mr.Dave Roberts &Mr.Michael Hal "An Integrated Methodology for SoC Design, Verification, and Application Development" IBM Microelectronics
[3]. Arm System-On-Chip Architecture (Hand book)
[4]. Mr.ThomasHollstein, Mr.ZeboPeng, Mr.RaimundUbar, Mr.ManfredGlesner. "Challenges for Future System-on-Chip Design" European Conference on Circuit Theory and Design, August-2001 - 28-31, Finland
[5]. Mr.Weiwei Chen, Mr.Xu Han, Mr.RainerDomer "ESL Design and Multi-Core Validation using the System-on-Chip Environment" University of California, Irvine, USA
[6]. Mr.Chuan Lin, Mr.HaiZhou "Retiming for Wire Pipelining in System-On-Chip" Electrical and Computer Engineering - Northwestern University - IL 60208.
[7]. Mr.Jan M. Rabaey, Mr.Ali M. Niknejad, BorivojeNikolic, Mr.AlbertoSangiovanni "Embedding Mixed-Signal Design in Systems-on-Chip"
[8]. Mr.William D. Mensch, Mr.Dennis A. Silage "System-on-chip design methodology in engineering education"The Western Design Center, Inc., Mesa, AZ, USA&Temple University, Philadelphia, PA, USA,
[9]. Dr. David J Greaves, "System on Chip Design and Modelling" University of Cambridge
[10]. V.Madisetti and Mr.C.Arpnikanandt "Platform-Centric SOC Design Methodology"
[11]. Mr.Tien-Fu Chen, "Overview of SOC Architecture design" National Chung Cheng Univ.
[12]. Mr.NikolayKavaldjiev, Mr.Gerard JM Smit "A Survey of Efficient On-Chip Communications for System-On-Chip" University of Twente– Netherland
[13]. G.Kavya, V.ThulasiBai- Sathyabama University, "Implementation of GPS Signal Acquisition and Tracking in FPGA" Prathyusha Institute of Technology and Management Chennai, Published in IJRET: International Journal of Research in Engineering and Technology eISSN: 2319-1163 | pISSN: 2321-7308.