IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 5, May 2016

Comparison between Voltage Domain and Time Domain ADCs-A Review

Deepali D Toraskar [1], Mahantesh P Mattada[2], Hansraj Guhilot[3]

PG Student, Deparment of ECE, Sanjay Ghodawat Institutes, Kolhapur,India [1]

Assistant Professor, Department of ECE, Sanjay Ghodawat Institutes, Kolhapur, India [2]

Principal, Department of ECE, KC College of Engineering Kopri, Thane, India [3]

Abstract: A review of comparison of various types of ADC's with Time Based ADC. The performance of the analog to digital converters has become very important in signal processing applications. Most important parameters on which their performance depend are: resolution, power consumption, size, conversion time, static performance, dynamic performance, and price. It became very important to understand the functioning and performance before implementing the ADC in the system. This paper discusses and compares the voltage domain ADCs with Time Based ADC's.

Keywords: Analog-to-digital converters, Time Based ADC, Time to Digital Converter.

I. INTRODUCTION

Today, digital signal processors (DSP) and digital integrated circuits are taking advantage of technology scaling to achieve improvements power, speed, size and cost. Meanwhile, as technology scaling reduces supply voltage and intrinsic transistor gain, analog circuit designers face disadvantages. Due to these disadvantages of technology scaling, two new broad trends have emerged in ADC research. The first trend is digitally assisted analog design, which emphasizes the relaxation of analog domain precision and the recovering accuracy (and performance) in the digital domain. This approach helps to reduce power consumption. The second trend is the representation of signals, and the processing of signals, in the time domain. Technology scaling and its focus on high-performance digital systems offers better time resolution by reducing the gate delay. Therefore, if we represent a signal as a period of time, rather than as a voltage, we can take advantage of technology scaling, and potentially reduce power consumption and die area [6].

To overcome the challenge of low-voltage design is to process a signal in the time-domain. Time resolution has been improved in nanometer-scale devices due to the reduction of gate delay, despite the reduction in supply voltage. Hence, time-domain processing potentially offers a better solution compared to voltage-based methods, when implemented in deep sub-micron VLSI fabrication processes. This 'digital' approach is more power efficient compared with pure analog solutions, utilized for amplitude measurement of input signals [5]. Timing measurement accuracy presents a major challenge and we can use various methods in which accuracy can be achieved using CMOS processes.

In this paper, we discuss and compare pipelined ADC, SAR ADC, Sigma Delta ADC in Voltage domain ADC and Time Domain ADC. We compare it on basis of resolution, power consumption, size, conversion time and price

II. VOLTAGE DOMAIN ADC

A. Pipeline ADC

The pipeline ADC is the architecture is used for applications that require both speed and accuracy and where latency is not concern. The basic idea behind the pipeline ADC is that each stage will first sample and hold the input then compare with VREF/2. If the input is greater than VREF/2, output a 1 for that stage and pass the input voltage directly to the next stage. If the input is less than VREF/2, output a 0 for that stage and multiply the input voltage by 2 before passing it to the next stage. Figure 1 shows the block diagram for this basic operation.

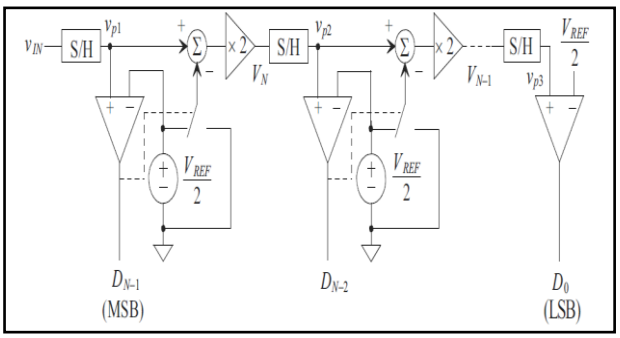

Figure 1 Pipeline ADC Block Diagram [1]

There an error in the early stages of the pipeline will propagate through the pipeline affectively being amplified by 2 by each successive stage as we refer [1]. Errors can be created by the comparators not switching at the correct point. Due to offset in comparator which will result in it making the wrong decision. The sample and hold may also have some offset causing same problem of the comparator making a wrong decision. The other source of error is the multiply by 2 function, because it is difficult to multiply by a gain of exactly 2. These limitations with real op-amps and comparators will result in differential nonlinearity (DNL) and integral nonlinearity (INL) errors.

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 5, May 2016

B. SAR ADC

In successive approximation ADC the only change in design is a very special counter circuit known as Successive Approximations Register. This register counts by trying all values of bits starting with the most-significant bit and finishing at the least significant bit. Overall count process, the register monitor the comparator's output to see if the binary count is greater than or less than the analog signal input, adjusting the bit values accordingly. The advantage to this counting process gives much faster results. Important point to note on Successive Approximation ADC is that in digital ramp type or Counter type ADC, the time taken for conversion depends on the magnitude of the input voltage, but in SAR ADC the conversion time is independent on applied input voltage. Advantages of SAR ADC are speed is high compared to digital ramp type and counter type ADC. Good ratio of speed to power.

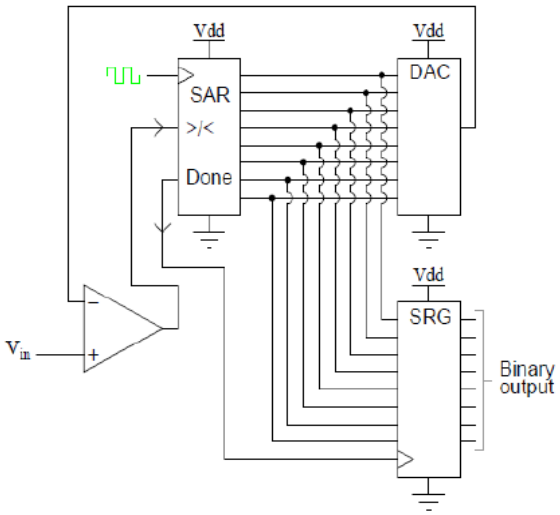

Fig 2: Successive Approximation ADC

Disadvantages of SAR ADC are cost is high as compare to counter type ADC due complexity in design. Applications of SAR ADC in data acquisition techniques at the sampling rates higher than 10 KHz [2].

C. Sigma – Delta ADC

The sigma-delta (Σ-Δ) ADC architecture had its origins in the pulse code modulation (PCM) systems. In this converter, the analog input voltage signal is given to the input of an integrator, producing a voltage rate-of-change, at the output. This ramping voltage is compared against ground voltage (0 volts) by a comparator. The comparator acts as a 1-bit ADC, producing 1 bit of output (low or high) depending on whether the integrator output is positive or negative. Then comparator's output is latched through a D-type flip-flop and fed back to another input channel on the integrator, to drive the integrator in the direction of a 0 volt output. D flip flop is clocked at high frequency. The basic circuit diagram is shown in fig 3. The leftmost op-amp is the summing integrator. The next op-amp, the integrator feeds into is the comparator, or 1-bit ADC. This output is given to D-type flip-flop, which latches the comparator's output at every clock pulse, sending either a low or high signal to the next comparator which at the top of the circuit. This final comparator is necessary to convert the single polarity 0V /5V logic level output voltage of the flip-flop into a +V / -V voltage signal to be fed back to the integrator. If the integrator output is +V, the first comparator will output a high signal to the D input of the flip-flop. At the next clock pulse, this high signal will be output from the Q line into the non-inverting input of the top (last) comparator.

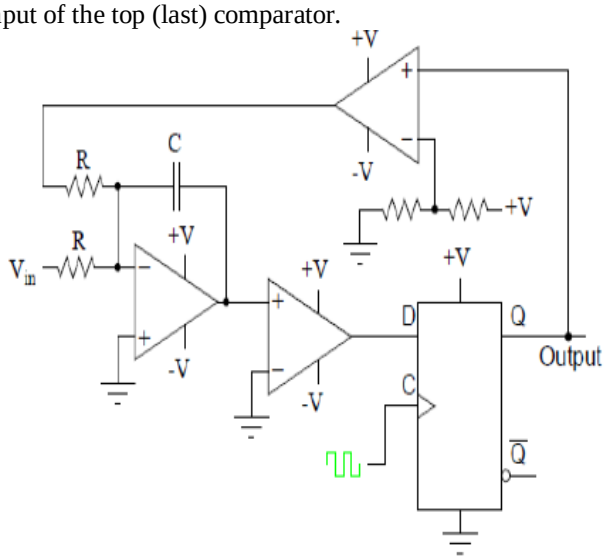

Fig 3: Block diagram of Delta Sigma ADC [1]

Here this last comparator, seeing an input voltage greater than the threshold voltage of 1/2 +V, saturates in a positive direction, sending a full +V signal to the other input of the integrator. This +V feedback signal tends to drive the integrator output in a negative direction. If that output voltage becomes more negative, then feedback loop will send a corrective signal (-V) back around to the top input of the integrator to tend it in a positive direction. This is the delta-sigma concept in action: the first comparator senses a difference between the integrator output and zero volts.

Advantages of this ADC is that modern Sigma-delta converters offer high integration, low power consumption, high resolution, and low cost. Due to that advantage making it as a good ADC choice for applications such as process control, weighing scales and precision temperature measurements [7].Limitation of this ADC is that higher order (4th order or higher) and multi-bit feedback DAC requires large area, so complexity is more.

III. TIME DOMAIN ADC

A. Time based Pipeline ADC

A hybrid pipelined ADC which uses both voltage and time domain information is proposed [3]. While maintaining high linearity, the proposed ADC employs a new voltage-to-time conversion scheme using a scalable, power efficient, residue amplifier with minimal dc gain in its first stage. This scheme without sacrificing bandwidth, not only reduces the power consumption of the ADC but also relaxes the design trade-off of the amplifier in a low supply voltage deep sub-micron process.

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 5, May 2016

Shown in Fig. 4 is the proposed hybrid voltage and time based pipelined ADC. It consists of a conventional 4 bit MDAC (Multiplying Digital-to-Analog Converter) and a FLASH in voltage domain, a zero-crossing comparator for V-T conversion, four time-domain pipeline stages and a 2.5 bit TDC for backend pipelined stage, and other supporting blocks. The ADC generates a 14 bit digital output with a 1 bit redundancy between the pipeline stages.

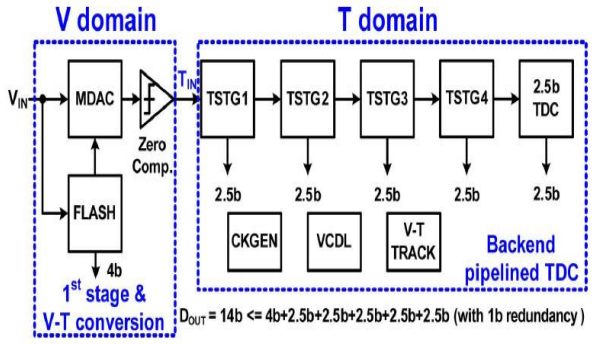

Fig. 4. Proposed time-based pipelined ADC [3].

V-T tracking block, which provides a coarse current reference to the V–T converter in the MDAC and four time-domain pipeline stages, follows the relation between the voltage and time domain gain. The linear gain error correction is enabled by the proposed V-T converter despite the use of a low gain nonlinear amplifier. For sub-TDCs time reference, a voltage controlled delay line (VCDL) is referred.The important features of the proposed ADC are as follows: wide signal bandwidth and high resolution can be attained with the pipelined Nyquist ADC architecture. Next is a nonlinear and low gain power-efficient amplifier can be used for linear V-T conversion in the first stage based on the proposed V-T conversion. Next, for low power consumption a simple charge pump based on pipelined architecture is employed. Finally, the high accuracy is easier to achieve than a conventional TDC [3].

B. SAR ADC

Time to digital converter operates in two steps, first in the time domain by using a delay-line TDC and then in the voltage domain by using a SAR ADC. In first stage the time residue is converted to voltage by using a switch-based time-to-voltage converter (TVC). Pseudo-differential time-domain signaling is presented to improve the linearity of the proposed TVC [4].

The block diagram of the proposed two-step N-bit TDC is shown in Fig. 5.

It consists of an m-bit delay-line TDC, followed by a residue generator, a TVC, and an N−m bit SAR ADC. The proposed TDC offers advantages compared with the N bit delay-line-based TDC. The proposed architecture can benefit from the energy-efficient SAR ADC and the reduced delay line that consumes the largest power, as compared with an N-bit delay-line TDC.

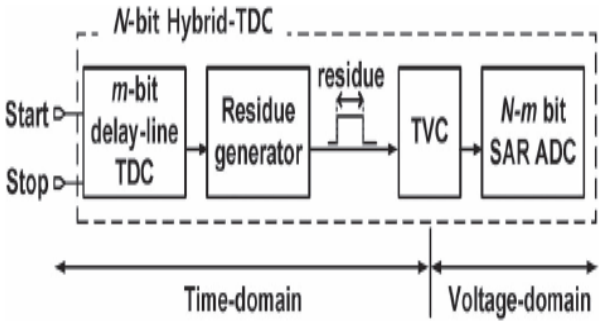

Fig. 5. Block diagram of the hybrid-domain TDC

In order to minimize the power consumption of the proposed TDC, an optimum m should be chosen, which involves the trade-off between the delay line and the TVC. When m is increased and more bits are resolved in the first-stage TDC, the power consumption of the delay-line TDC is increased, but the TVC can be less linear. When m is decreased and more bits are resolved in the second-stage ADC, the delay-line TDC consumes less power, but the TVC must be more linear and thus consumes larger power [5]. A hybrid-domain two-step TDC that achieves an time-to-digital conversion with subpico-resolution has been presented. The proposed architecture exploits the energy efficient ADC to achieve low power consumption and relaxes the linearity requirement of the TVC [6].

C. Sigma Delta ADC

The diagram in Fig. 6 shows a sinusoidal input of peak-to-peak amplitude of V_{pp} centered at $V_{FS}/2$, where V_{FS} is the full scale voltage, is digitized using time-mode circuits. The input signal is sampled-and-hold at frequency fs then a PWM block transforms the voltage into a pulse-width which is digitized using the TDC (Time to digital converter). The conversion of the analog signal into the digital format is performed in the time-mode. The only one part is performed in voltage-mode is the pulse width modulation [7].

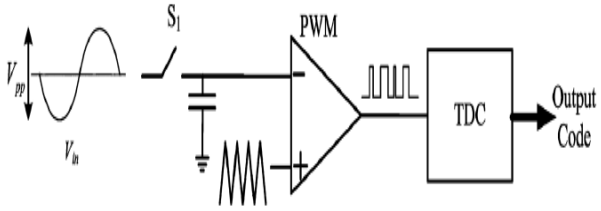

Fig.6. Open-loop time-mode-based ADC [7].

Here the concept of the ∑Δ modulator is adopted in time-mode designs as shown in Fig. 7 shows the analogy between the voltage-mode ∑Δ modulator and its time-mode counterpart. The PWM convert the input voltage into a pulse and the TDC generates a multi-bit digital output,D_{out} that corresponds to the pulse-width and provides a time-quantized feedback pulse,$P_q(t)$, which emulates the DAC output in traditional ∑Δ modulators. On the other hand, the timing-accuracy of the feedback signal (the feedback pulse width $P_q(t)$) should be in the order of the targeted SNR.

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 5, May 2016

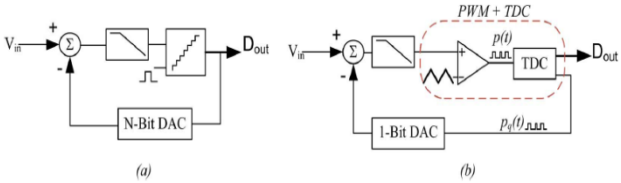

Fig. 7. Voltage-mode versus time-mode modulator [7]. (a) Voltage-mode modulator. (b) Time-mode modulator

In conclusion, TDC-based ∑Δ modulator more suitable to nanometric technology by minimizing the analog portion of the system. Since a reduced number of time-quantization steps is required compared to the open loop case, along with low latency to minimize the excess loop delay. For time-mode based ∑Δ modulators, inverter-chain-based TDC is a suitable choice [8]

IV. COMPARISON OF VARIOUS VOLTAGE DOMAIN ADC AND TIME DOMAIN ADC

	VOLTAGE DOMAIN			TIME DOMAIN		
Parameter	Pipeline ADC	SAR ADC	Sigma-Delta ADC	Pipeline ADC	SAR ADC	Sigma-Delta ADC
Conversion Method	Small parallel structure, each stage works on a few bits	Binary search algorithm, internal circuitry runs at higher speed	Comparator senses the difference and integrator sums the comparator's output with the analog input signal, Oversampling ADC	ADC employs a new voltage-to-time conversion scheme and that time converted into digital signal.	Signal is converted to time domain by using a delay-line TDC and then in the voltage domain by using a SAR ADC	Analog voltage converted variable pulse by using PWM and further TDC is used
Selection of this architecture	High speeds, lower power consumption than flash ADC	Low power consumption , small size	low to medium speed, digital filter reduces anti aliasing requirements	High speed, small die area, low power consumption as compared voltage domain pipeline ADC	High speed, Small die Area as compared to voltage domain SAR ADC	High speed, low power consumption as compared to voltage domain Sigma-Delta ADC
Resolution	few Msps to 100+ Msps, 8 bits to 16 bits resolution	Medium to high resolution (8 to 16bit)	High resolution	Sub-micron resolution	Sub-pico Resolution	Sub-nano resolution
Disadvantages	Parallelism increases throughput at the expense of power and latency	Speed limited to~5Msps.May Require anti aliasing filter	Higher order (4th order or higher) and multi-bit feedback DAC require large area	It is difficult to reduce the power consumption of the pipelined ADC	It is difficult to measure time signal	The TDC shows competitive area and power consumption

V. CONCLUSION

This comparison suggests that, in theory, time-based architectures are more efficient as compared with conventional ADC. This paper, can be a guideline to one who want to replace voltage-domain circuits with time-based alternatives. Intuitively, as the voltage supply is dropped, the voltage level detection gets more challenging in presence of amplitude noise (e.g., voltage and current thermal noise). However, when we transfer the signal to time, the circuit works with the full supply voltage and hence is not affected by amplitude noise.

This work has made several important contributions to the field of ultra-low power ADC design, in deep-submicron CMOS technologies. In particular we have:

1. Time-based and "digitally-friendly" ADC architecture
2. Proposed theory which describe the advantages of Time based ADC architecture compared to conventional approaches.

REFERENCES

[1] Mrs. Jasbir Kaur, Saurabh Kansal, "Study of Various ADCs and Compare Their Performance and Parameters", International Journal

of Advanced Engineering Research and Technology (IJAERT) Volume 3 Issue 3, March 2015.

[2] Jim LeClare, Principal Member of Technical Staff, "A Simple ADC Comparison Matrix", Jun 27, 2003 Taehwan Oh, Member, IEEE, Hariprasath Venkatram, Member, IEEE, and Un-Ku Moon, Fellow, IEEE, "A Time-Based Pipelined ADC Using Both Voltage and Time Domain Information", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 4, APRIL 2014

[3] Jungho Kim, Student Member, IEEE, Young-Hwa Kim, Student Member, IEEE, KwangSeok Kim, Student Member, IEEE, Wonsik Yu, Student Member, IEEE, and SeongHwan Cho, Senior Member, IEEE, "A Hybrid-Domain Two-Step Time-to-Digital Converter Using a Switch- Based Time-to-Voltage Converter and SAR ADC", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 62, NO. 7, JULY 2015

[4] Zule Xu, Student Member, IEEE, Masaya Miyahara, Member, IEEE, and Akira Matsuzawa, Fellow, IEEE, "Picosecond Resolution Time-to-Digital Converter Using Gm-C Integrator and SAR-ADC" IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 61, NO. 2, APRIL 2014.

[5] Jiayi Jin, Student Member, IEEE, Yang Gao, and Edgar Sánchez-Sinencio, Life Fellow, IEEE, "An Energy-Efficient Time-Domain Asynchronous 2 b/Step SAR ADC With a Hybrid R-2R/C-3C DAC Structure", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 6, JUNE 2014

[6] Mohamed M. Elsayed, Student Member, IEEE, Vijay Dhanasekaran, Member, IEEE, Manisha Gambhir, Member, IEEE, Jose Silva-Martinez, Fellow, IEEE, and Edgar Sánchez-Sinencio, Life Fellow, IEEE, "A 0.8 ps DNL Time-to-Digital Converter With 250 MHz Event Rate in 65 nm CMOS for Time-Mode-Based ∑Δ Modulator", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 9, SEPTEMBER 2011

[7] Jorg Daniels, Student Member, IEEE, Wim Dehaene, Senior Member, IEEE, Michiel S. J. Steyaert, Fellow, IEEE, and Andreas Wiesbauer, Member, IEEE, "A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 57, NO. 9, SEPTEMBER 2010.

[8] L. Hernandez and E. Prefasi, "Analog-to-digital conversion using noise shaping and time encoding," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 7, pp. 2026–2037, Aug. 2008.

BIOGRAPHIES

Miss. Deepali D. Toraskar, PG Student in Department of ECE, Sanjay Ghodawat Institutes, Kolhapur, India. Currently she is working on CMOS implementation of Time based ADC. Her area of interests are CMOS VLSI Design and Embedded Systems.

Prof. Mahantesh P. Mattada, working as Assistant Professor in Department of ETC, Sanjay Ghodawat Institutes, Kolhapur, India. He received B.E Electronics & Communication, Masters Degree, M.Tech in VLSI Design and Embedded Systems from V.T.U Belagavi. Currently he is working on design and testing of various Time to Digital Converter architectures. His area of interests are CMOS VLSI Design, Digital Design using FPGA.

Dr. HansrajGuhilot, Principal& Professor, Department of ECE, KC College of Engineering Kopri, Thane, India. He received B.E. in Electronics from University Visveswaraiah College of Engineering, Bangalore and M.Tech in Industrial Electronics from Karnataka Regional Engineering College, Surathkal in 1981 and 1985 respectively. He holds 9 international and 1 Indian patents. His areas of interests are Smart Sensors, Agro-Electronics, Biomedical and Mixed Mode VLSI Design. He is as an expert in Power Electronics especially his patented solution on a power processor for metal halide lamps and High Frequency Electronic Ballast for lighting has been major breakthroughs in the industry. He has published more than 30 research papers and was felicitated by Ministry of Human Resource Development, Govt. of India, for owning international patents.

DOI 10.17148/IJARCCE.2016.55142