IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 5, May 2016

Development of FPGA based Processing Electronics for Gamma Ray Spectrometer (GRS) and Comparisons between two Different Methods

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Abstract: In the instrumentation field, γ rays make their own value because of its high energy nature. The spectroscopy based on γ rays is used in the space exploration programs, nuclear physics, geophysics, medicine & thermonuclear fusion. This paper describes the development of processing electronics & data acquisition system designed for Gamma Ray Spectrometer (GRS) for the future space mission. The surface composition in terms of concentration of major elements is one of the most fundamental information about any planetary body. Gamma ray spectrometer is the mostly used technique to determine the elemental abundances of the elements of the surface and it's subsurface. High purity Germanium (HPGe) detector is planned to be used in this Gamma Ray Spectrometer. Processing electronics covers the analysis of the analogue data, coming from pulse shaping amplifier. In this analogue data, output of the pulse shaping amplifier is a Gaussian shape pulse, where peak amplitude gives the information of the incoming energy of γ ray. Processing electronics includes event trigger generator, peak detector, ADC & FPGA based setup to generate histogram of γ ray counts. In data acquisition part NI DAQ card & LabVIEW software are used for plotting of the histogram.

Keywords: Filed Programmable Gate Array (FPGA), Analogue to Digital Converter (ADC), Data Aqauisition software (LabVIEW), Data Aqauisition card (NI DAQ card), Gamma Ray Spectrometer (GRS).

I. INTRODUCTION

The Gamma ray spectrometer is the mostly used technique for determining the elemental abundances of any planetary surfaces. In the instrumentation field, γ rays make their own value because of its high energy in nature. The spectroscopy based on γ rays is used in the space exploration programs, nuclear physics, geophysics, medicine & thermonuclear fusion. From all research areas, our main focus is to find out elemental composition of any planetary surface by measuring the energy of γ - rays. After a long study of various detectors, we have selected HPGe (High Purity Germanium) for the detection of gamma rays. The advantages of this detector are: high detection efficiency, very high energy resolution, coverage of a very wide energy range.

Only drawback of using this detector is, HPGe detector needs liquid nitrogen temperature (~70K - 90K) for the operation to minimize the effects of the leakage current.

Generation of the γ - rays: The generation of the γ rays happens in two ways: either through natural radio-activity or by the interaction of GCR particles with the surface. Th, K, U etc. are few natural radio-active elements which keep on generating the γ - rays. In case of interaction of GCR particles with the surface: when the high energy proton (> 100 MeV) interacts with the surface, it generates neutrons. These neutrons further interact with the surface materials and then γ - rays are generated from the nucleus.

Fig. 1 depicts the generation of the γ - rays with both the processes. The measurement of the energy of the γ - ray gives the information of the element present on surface or subsurface of planetary body.

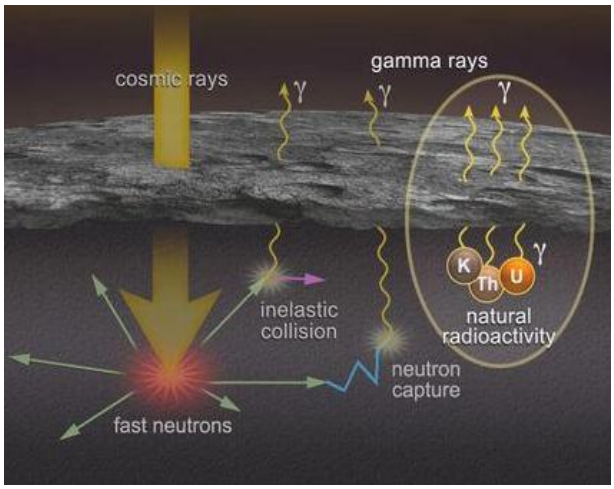

Fig. 1: Generation of the γ - rays

II. BLOCK DIAGRAM OF GAMMA RAY SPECTROMETER

The block diagram of the Gamma Ray Spectrometer (GRS) is shown in the Fig. 2.

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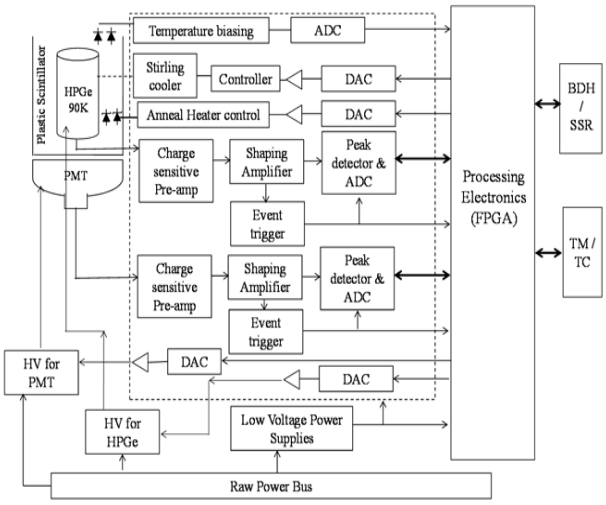

Fig2. Block diagram of GRS

The complete GRS can be divided into 4 sub - systems:

Detector:

In the block diagram (Fig. 2), HPGe detector is used for the detection of gamma rays. The detector is cooled to a very low temperature around 90K. In this block diagram, Anti - Coincidence Shield (ACS) detector is used for the background subtraction.

Front End Electronics (FEE):

HPGe detector and ACS detector both have independent FEE. The output of the detector is fed to the CSPA (Charge Sensitive Pre-Amplifier), where output charge from the detector is converted into voltage by using a feedback capacitor. The overall design of CSPA is different for both the HPGe and ACS detector. The value of feedback capacitor depends on measurable energy range of the detector. The output of the CSPA is further given to the pulse shaping amplifier. Pulse shaping amplifier shapes the output of CSPA (exponential decaying pulse) to Gaussian shape pulse for better FWHM (Full Width at Half Maximum) requirements.

Processing electronics (PE):

The output of shaping amplifier is further compared to a DC voltage for the triggering, which works as low level discriminator (LLD). The outputs of the pulse shaping amplifier and LLD are given to the processing electronics. Processing electronics includes the peak detector, ADC and FPGA. Peak detector holds the peak of the incoming pulse, once the peak is detected. The peak detector is controlled by FPGA. Once the peak is detected, ADC starts working convert the analogue data into 12-bit digital data. This 12 bits data represents the information about the energy of the γ - ray. PH300 (hybrid component from M/s Amptek Inc.) is used as the peak detector. MAX187 is the 12 bits ADC used for the analogue voltage detection.

Data Acquisition:

The output of the FPGA is further given to LabVIEW and NI DAQ card for the plotting and storing the data. FPGA controls the LabVIEW interface and other handshaking signals. Here FPGA generates the synchronization clock pulses for the NI DAQ card and LabVIEW reads the data on each rising edge of this synchronization pulse.

Here we are working on two methods to develop the processing electronics and LabVIEW data acquisition system.

Method 1: Use FPGA for only controlling & LabVIEW for data acquisition, processing system and storing.

Method 2: Use FPGA for both controlling and processing & LabVIEW for only data acquisition and storing.

III. COMPONENT OF PROCESSING ELECTRONICS

PH300 peak detector works in four modes: charging mode, hold mode, discharging mode & tracking mode. When event trigger detects the γ - ray, it generates a trigger pulse for FPGA to open the gate of peak detector so that pulses from shaping amplifier are detected by peak detector. In this case peak detector works in charging mode.

Form Fig. 3, the hold capacitor (inside peak detector) is charged up to rising time of input signal. Negative feedback is applied to amplifier through high impedance. So, as soon as input signal goes in decaying mode, hold capacitor holds the peak of the pulse and it generates a pulse as a trigger that peak is detected.

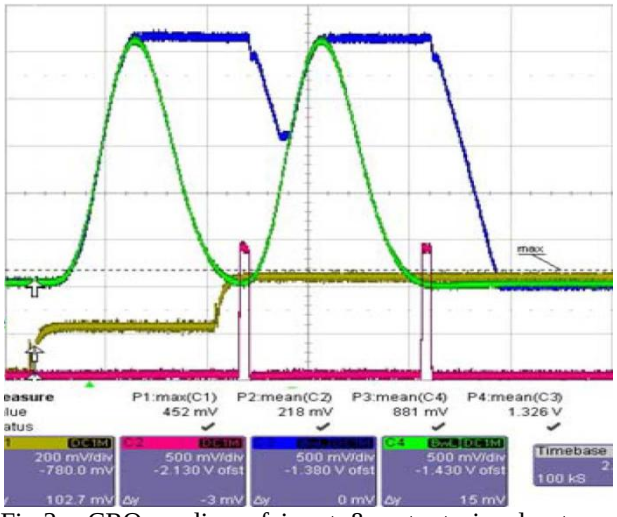

Fig.3. CRO reading of input & output signals at peak detector [1] (output of the shaper (green), output of the peak detector (blue), peak discharger pulse (red), input test signal (yellow))

With this pulse, FPGA starts operating the ADC for the analogue voltage conversion by giving falling edge of CS control line. FPGA monitors the status of output port of ADC. Because high value of ADC output port indicates completion of analog to digital conversion. FPGA starts reading this 12-bit serial output of ADC by giving 16 SCLK pulses. On the every falling edge of SCLK pulses, serial data is coming out from the output line of ADC. First 12 SCLK pulses are for 12-bits ADC conversion data & last 4 SCLK pulses are for trailing zeroes.

After Analogue to Digital Conversion, hold capacitor is discharged for the processing of next γ rays events. For

DOI 10.17148/IJARCCE.2016.5524

IJARCCE

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discharging of PH300, FPGA gives low value to RAMP & DUMP control lines of Peak detector. RAMP is for linear discharging & DUMP is for fast discharging process.

IV. COMPONENT OF DATA AQUASITION SYSTEM

NI DAQ card SCB - 68 & LabVIEW software is used for the data acquisition. This SCB - 68 kit gives flexibility to read or write data on level trigger mode or edge trigger mode. By selecting port or lines from the LabVIEW program, data can be read or written from port or individual lines. In LabVIEW program, data is acquired on each rising edge of synchronization clock which is given by FPGA. The graph is plotted between incident γ - rays energy and counts. This graph gives the information of the energy of the γ - rays andits intensity.

V. METHOD – 1

In this method role of FPGA is to control operations of peak detector & ADC by observing the event trigger generator pulses. LabVIEW is used for data acquisition processing. In data processing work, LabVIEW generates histogram of γ ray spectrometer data.

A. Simulation readings of Method-1 FPGA code

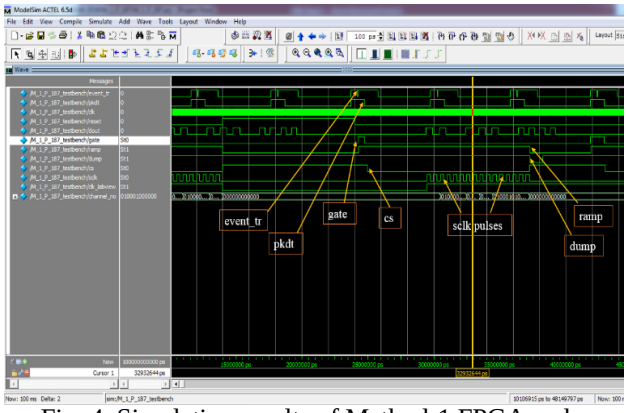

Fig. 4. Simulation results of Method-1 FPGA code

From Fig. 4. We can see that gate control signal of peak detector is set to high level when rising edge of event_tr signal occurs. After reaching at peak value of input, peak detector gives falling edge at PKDT signal to FPGA. By observing this PKDT signal FPGA start ADC operations.
For ADC operation, FPGA gives falling edge to ADC control signal CS to start analogue to digital conversion. Once the conversion is over FPGA gives 16 SCLK pulses to read serial output data from ADC. The last 4 SCLK pulses are for trailing zeroes, in time interval of last 4 pulses FPGA gives synchronization clock to NI DAQ card to read FPGA data.

B. CRO readings
From Fig. 5, we can analyze SCLK & DOUT signals & conclude that, output serial data form ADC is 0011111010000. Decimal value of this data is 2000. That means peak value of peak detector input signal is 2000 mV.

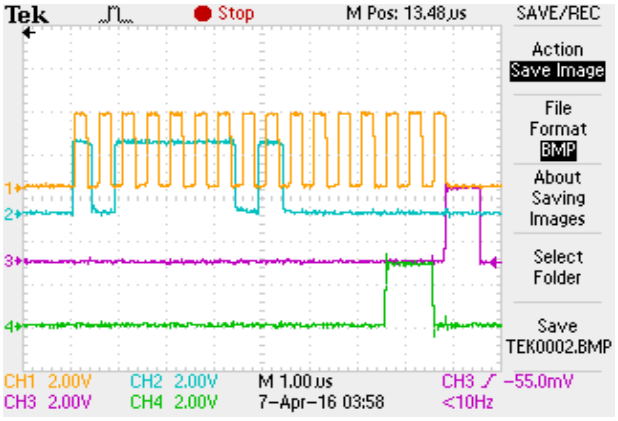

Fig.5. control signals of CRO readings of Method-1(SCLK pulses (yellow), output of ADC (blue), conversation start signal of ADC (pink), synchronization clock between FPGA & LabVIEW (green))

Calculations:
Analogue input of peak detector is: 2 V
ADC resolution in term of Voltage: 1 mV per bit
Data from ADC = Analog input / ADC voltage resolution
= 2 V / 1 mV
= 2000 (Channel number)

C. LabVIEW Readings

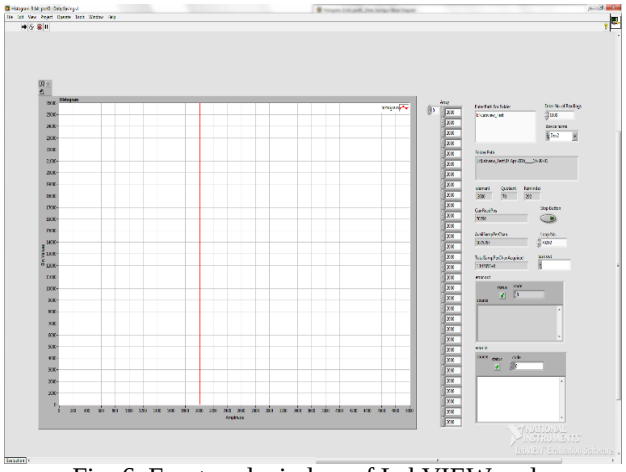

Fig. 6. Front-end window of LabVIEW code

From Fig. 6. We can see that graph is showing readings at 2000 channel number. Here, for testing purpose we are giving fix input voltage to the input of peak detector to analyze processing electronics & data acquisition part readings

From above graph result, it shows that both FPGA and LabVIEW are working fine.

D. LabVIEW data saving
By taking path from user, LabVIEW code will generate folder with the name of current date & time. Data is stored in .XLS file format. Those folders are looks like Fig.7.

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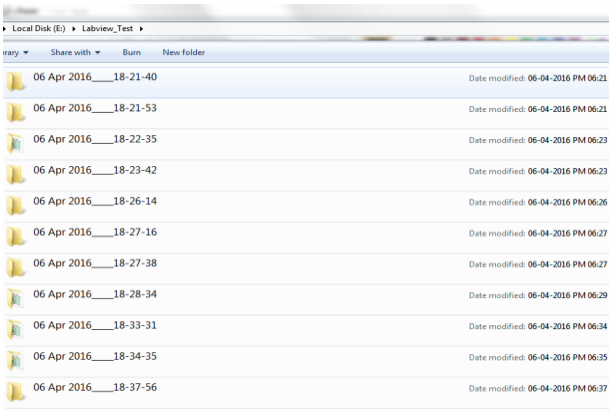

Fig7. LabVIEW data saving folder window

E. Limitations ofMethod-1

Method-1 has one limitation. The limitation is the reading speed of LabVIEW as it is very slow and reading speed changes over the period of time as per the back-end processes of computer. So the reading speed of LabVIEW is difficult to estimate.

F. Conclusion of Method-1

After working on Method-1 we could find that method-1 is not the right way to process the GRS data, because memory on LabVIEW DAQ card is full after several minutes. So, better way is to go with method-2 for processing GRS data.

VI. METHOD - 2

In this method, the role of FPGA is to control operations of peak detector & ADC by observing event trigger generator pulse. In data processing operation, FPGA generates histogram by using internal RAMs. Here LabVIEW program is used for data acquisition and storage along with the live display of data.

Connection overview: In this method FPGA generates control signals for controlling operations of peak detector & ADC. FPGA also generates histogram for fixed amount of time and after this time interval, FPGA sends histogram data to LabVIEW. FPGA generates clock pulses for NI DAQ card to read data from FPGA on the edge of this clock. FPGA array which contains histogram data is connected to the ports of NI DAQ card. We are using 2 RAMs of size of 4096x16 for histogram development.

FPGA code with internal RAMs interface: We have decided to make spectral data from the event data by counting event data in spectral bins. It will carry out using two 4K x 16 bit FPGA internal RAMs. While storing current data in one RAM, the previous second data, which is stored on another RAM, will be transmitted to NI DAQ card. The transmission of 1 second data is completed in 42ms with the clock frequency of 100 KHz.

Data transmission between FPGA & LabVIEW: FPGA gives 1 start pulse, 1 stop pulse, 5 clock pulses for header, 5 clock pulses for trailer & 4096 clock pulses for RAMs histogram data. In histogram data sending process, FPGA gives 4096 clock pulses to read data from each address of RAM & sends it to the LabVIEW.

Start Pulse data: 010000000000000000
Stop Pulse data: 100000000000000000
Header data: 001111111111111111
Trailer data: 001111111111111111

A. Smart design window of Methid-2 FPGA code

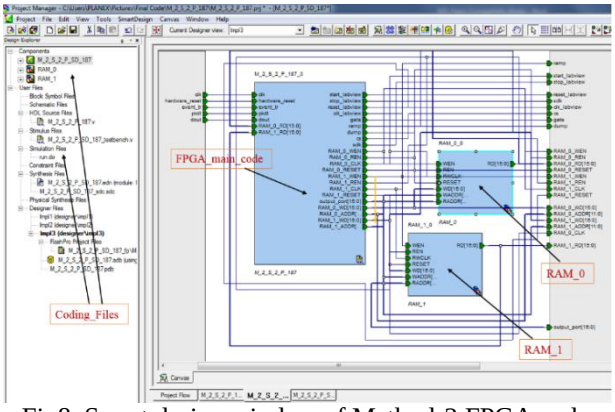

Fig8. Smart design window of Method-2 FPGA code

Fig8. Shows the interface between Verilog code and FPGA internal RAMs. For the simulating RAMs operations, control signals of RAMs are taken as an output.

B. Simulation reading-1 of Method-2 FPGA code

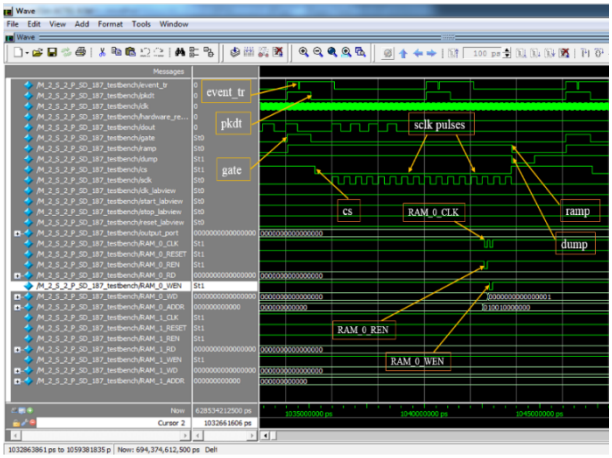

Fig. 9: Simulation result-1 of Method-2 FPGA code

In Fig. 9, it is shown that after 13 SCLK pulses we get the channel no. for the memory. That channel number is filled up in address line of RAM. FPGA gives low level signal to read-enable line & also clock signal to read data from RAM address. After reading data from RAM, FPGA increments the value & writes it back to the same address.

C. Simulation reading-2 of Method-2 FPGA code

Fig. 10 shows that after 1 second, RAM 0 switches from data storing to data transfer state. In this figure, star_labview line (to start LabVIEW data) is high for its first clock and output port value is 010000000000000000. Header part is started from 2nd clock. Header part includes first 5 clk_labview clock & output port value is 001111111111111111.

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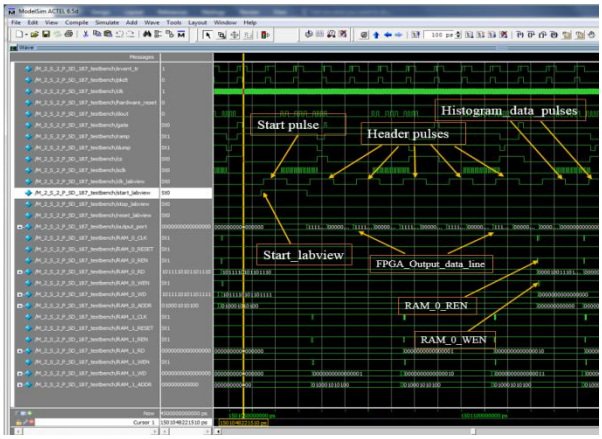

Fig. 10: Simulation result-2 of Method-2 FPGA code

D. Simulation reading-3 of Method-2 FPGA code

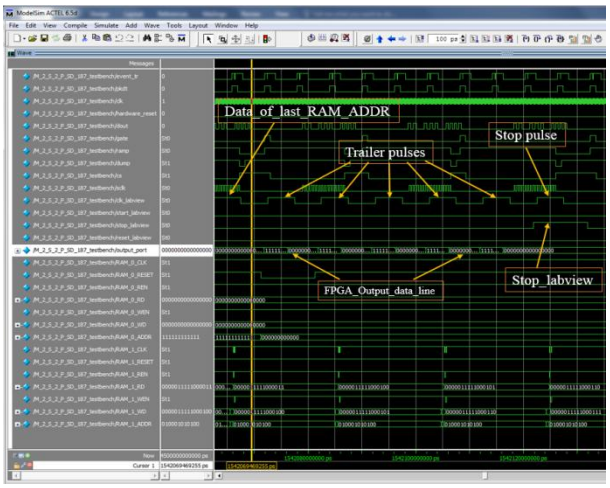

Fig. 11: Simulation result-3 of Method-2 FPGA code

From Fig. 11, we can see that after 5 clocks of header & 4096 clocks of histogram data, how trailer part & stop clocks are working. Trailer part includes 5 clk_labview clock & output port value of 001111111111111111. After trailer clock, last clock is for stop communication between LabVIEW & FPGA. In last clock stop_labview line is high & output port value is 010000000000000000. We can also see that RAM_0_RESET is low when 1st clock of trailer part forresetting all the output values of RAM.

E. Simulation reading-4 of Method-2 FPGA code.

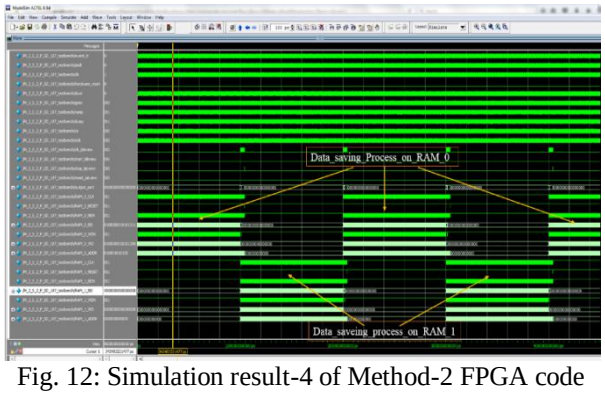

Fig. 12: Simulation result-4 of Method-2 FPGA code

Fig. 12: shows the simulation result of 4.5 second time interval and switching of RAMs in the different operating modes.

F. CRO reading-1

From Fig. 13, we can see that when the rising edge of event trigger generator pulse is detected, FPGA gives high value to the gate of peak detector. When falling edge of PKDT signal is detected FPGA gives low value to gate line to stop the further pulses. After hold capacitor is fully charged up to peak value of input, FPGA gives low value at CS line to start ADC conversion.

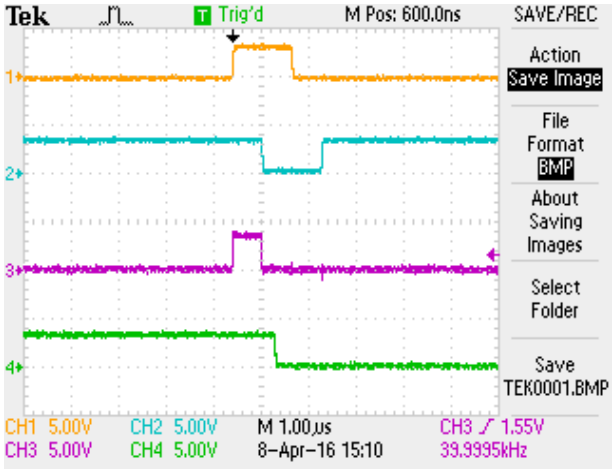

Fig. 13: CRO reading-1 of Method-2 (event trigger pulse (orange), PKDT control signal of peak detector (blue), gate control signal of peak detector(pink), CS conversion start signal of ADC (green))

G. CRO reading-2

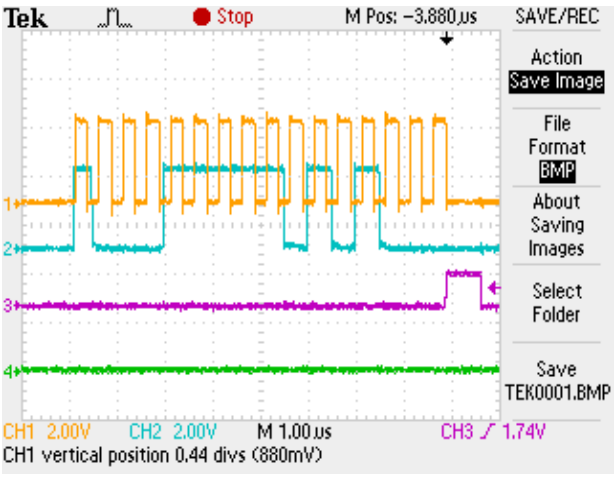

Fig. 14: CRO reading-2 of Method-2 **(**SCLK pulses (yellow), output of ADC (blue), CS signal of ADC (pink), synchronization clock between FPGA & LabVIEW (green))

From Fig. 14, we can see that when ADC gives high output, FPGA generate 16 SCLK pulses to read serial ADC data. In this 12-bit serial ADC output data, 1st SCLK pulse generate MSB of ADC output & 12th SCLK pulse generate LSB of ADC output. Last 4 SCLK pulses are

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International Journal of Advanced Research in Computer and Communication Engineering
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used for trailing zeroes. After 16 SCLK pulse, CS signal is high for the next conversation.
From Fig. 14, we can analyze SCLK & DOUT signals & conclude that, output serial data form ADC is 0000111110101. Decimal value of this serial data is 501. That means peak value of input signal of peak detector is 501 mV.

Calculations:
Analogue input of peak detector is: 501 mV
ADC resolution in term of Voltage: 1 mV per bit
Data from ADC = Analog input / ADC voltage resolution
= 501 mV / 1 mV
= 501 (Channel number)

H. LabVIEW readings

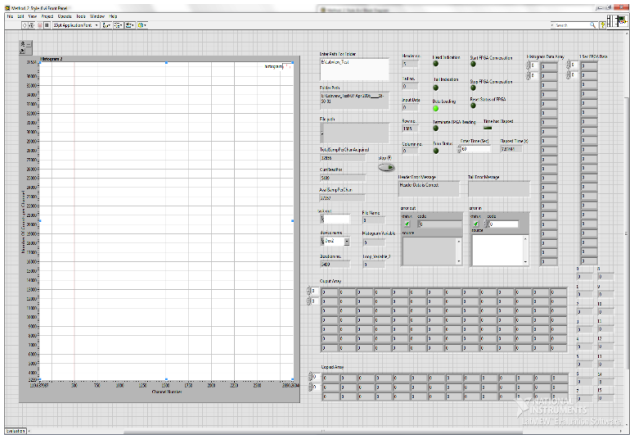

Fig. 15: Front-end window of LabVIEW code

From fig. 15, we can see that graph is showing readings at 501 channel number. Here, for testing purpose we are giving fix input voltage to the peak detector for analyzing the processing electronics & data acquisition part.
From graph result in Fig. 16, we can justify that both FPGA and LabVIEW are working fine.

I. LabVIEW data saving

By taking path from user, LabVIEW code generates folder with the name of current date & time. Data is stored in .XLS file format as shown in Fig. 7.

J. Advantage of Method-2 over Method-1

In Method 2 we are sending histogram data from FPGA to LabVIEW after particular time intervals. So, slow reading speed of LabVIEW is not affected in Method-2.

K. Conclusion of Method-2

By working on Method-2, we find out that method-2 is more efficient & reliable way of generating processing electronics & data acquisition system of γ - rays spectrometer.

VII. CONCLUSION

We have developed processing electronics & data acquisition system to process gamma ray energy data in the form of histogram & give it to graphical user interface.

All the simulation test & hardware test is done. Next step is the assembling of processing electronics with front-end electronics to get the full system ready.

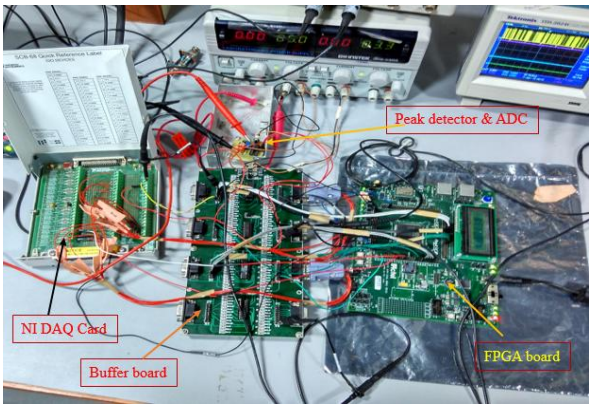

Fig. 16: Hardware Connections of Processing Electronics

ACKNOWLEDGMENT

We thank Physical Research Laboratory and Department of space for the funding of this study.

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