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Design & Optimization of CNTFET based Domino 1- Bit ALU

Ashish Sharma[1], Umesh Dutta[2], Sneha Arora[3], Vipin Kumar Sharma[4]

M.Tech Scholar, VLSI Design & Embedded System, Department of Electronics and Communication, FET,

Manav Rachna International University, Faridabad, Haryana, India[1, 3, 4]

Assistant Professor & Deputy Director MRIIC, Department of Electronics and Communication, FET,

Manav Rachna International University, Faridabad, Haryana, India [2]

Abstract: This paper presents a design technique of CNTFET based 1-Bit Arithmetic Logical Unit (ALU) using Domino Logic. Domino Logic offers smaller area and higher speed than Static Logic design. In this paper circuit performance of CNTFET based Domino logic 1-Bit ALU is compared with Static Logic 1-Bit ALU. The simulation results calculated using HSPICE have reported to show 38.6% reduction in delay and 12.8% reduction in area for Domino Logic as compared to Static Logic 1-Bit ALU(Full Adder Logic) at 32nm technology. For Optimization of CNTFET based Domino Logic 1-Bit ALU various parameters like diameter, temperature and pitch are varied at 32nm technology. The proposed Domino Logic 1-Bit ALU(Full Adder Logic) has shown reduction in Power Delay Product by 33.2% at 5nm pitch as compared to Domino logic 1-Bit ALU(Full Adder Logic) at 20nm pitch with CNT diameter at 1.487nm, 27℃ temperature and a reduction of 94.2% at 1.0179nm CNT diameter and 5nm pitch.

Keywords: ALU, CNTFET, Dynamic Logic, Domino Logic, Full Adder, Static Logic.

I. INTRODUCTION

With Advancement in technology as per Moore's law number of transistors on chip is increasing rapidly. As present devices are scaled down to increase performance in terms of speed, low power and less area up to nano scale region. Scaling of CMOS circuits in nano region have several problems like short channel effects, high power consumption and fabrication process. A possible approach to meet the challenges of nano scale CMOS consists of utilizing new circuit techniques together with alternative technologies to replace conventional silicon and the current MOSFET-based technology. Silicon based technology will reach its limits in 2020 when the channel length of MOSFET is below 10 nm [9].

The Carbon Nanotube Field Effect Transistor (CNTFET) is one of the most promising devices among emerging technologies. The CNTFET offers many potential advantages with respect to silicon-based technology.

Its operation principles and device structure are similar to CMOS, and therefore the mature design infrastructure of this latter technology can be utilized, together with its fabrication process[1].

As reported in the technical literature, the CNTFET has been experimentally demonstrated to have excellent current capabilities; an estimate of the performance of CNTFETs at single device level in the presence of process related effects and imperfections at 32 nm [1].

The power consumption of conventional CMOS circuits is composed of dynamic and static parts. The most power consumption comes from dynamic power consumption. The dynamic power is reduced by decreasing the activity factors, the switching capacitive power supply, or the operating frequency. Dynamic power consumption is large because of the circuits parasitic capacitance during CMOS circuit switching and clock frequency. The performance advantages have made dynamic logic circuits a main implementation option for high performance circuits. Since dynamic circuits have low input capacitance and less transistor count than its static counterparts, introducing dynamic circuits in the design results in high speed and compact area [1].

In this paper, we propose a technique that has higher speed of operation and low power i.e. designed using CNTFET technology. We have designed and optimized CNTFET based Domino Logic 1-Bit ALU which is simulated on HSPICE in 32nm technology. This paper is organized as follows: Section I starts with a brief introduction to the research work and overview of dynamic and static logic . Section II briefs about CNTFET technology, includes literature survey and parameters of CNTFET technology. Section III describes comparison between Dynamic and Static Logic. Section IV gives basic ALU description and its functioning. Section V describes Static 1-Bit ALU design. In Section VI, proposed Domino 1-Bit ALU is designed and optimized. In Section VII, methodology and metrics used for analysis are explained and in Section VIII and IX simulation results and conclusion are presented.

II. CNTFET TECHNOLOGY

Carbon nanotube field effect transistor (CNTFET) uses CNT as their semiconducting channels. A single-wall CNT (SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes it very promising for alternative to MOSFET[2]. An SWCNT can

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act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m) [10]. A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (n, m) [3]. The Nano tube is metallic if n = m or n − m = 3i, where i is an integer, else tube is semiconductor.
The diameter of the CNTFET is calculated by using following formula:

$$\text{Dcnt} = \frac{\sqrt{3}\,a_o\sqrt{n^2+m^2+mn}}{\pi} \qquad (1)$$

Where a0 = 0.142 nm is the inter-atomic distance between each carbon atom and its neighbor [11].
In CNTFET technology, the gate capacitance depends on the number of tubes and the pitch (where the pitch is defined as the distance between the centers of two adjacent CNTs in the same device) [7]. As the pitch decreases, the gate capacitance is also reduced due to the potential between adjacent CNTs (affecting the total gate capacitance). Moreover, the pitch also affects the current in the CNTFETs. Due to the screening effect [7], the total current of a CNTFET decreases as the pitch decreases.
The gate width can be approximated as

$$Wg = \text{Max}\,(Wmin \cdot N \cdot \text{pitch}) \qquad (2)$$

N is number of tubes, Wmin is minimum width of CNTFET
The I–V characteristics of the CNTFET are similar to MOSFET. Similar to the traditional silicon device, the CNTFET also has four terminals.
As shown in Fig.1, the undoped semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state [2]. As the gate potential
increases, the device is electro-statically turned on or off via the gate.
The voltage essential for turning ON transistor is called threshold voltage. Threshold voltage of Carbon Nano Tube is inversely proportional to diameter of CNT [3].

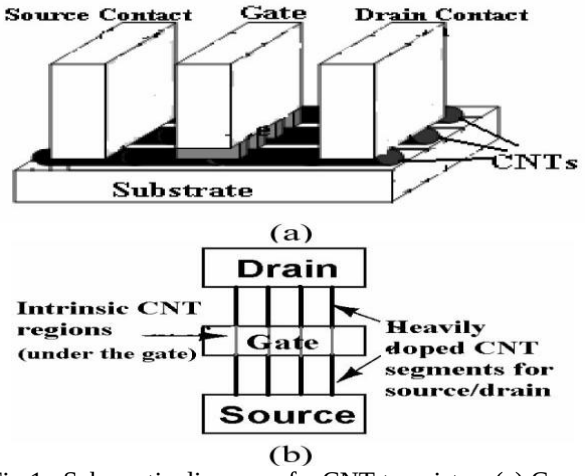

Fig.1. Schematic diagram of a CNT transistor (a) Cross sectional view. (b) Top view[10]

$$\text{Vth} = \frac{Eg}{2e} = \frac{\sqrt{3}\ aV\pi}{3\ eDcnt} \qquad (3)$$

Where, a=2.49Ao is carbon-carbon atom distance, $V\pi$ = 3.033eV is the carbon $\pi-\pi$ bond energy, e is the electron charge, Dcnt is diameter of CNT.

Some of the important characteristics of CNT are: high ION/IOFF ratio, the unique dimension band which suppresses back scattering. Comparing CNTFET and MOSFET, MOSFET have more scalability and less size which makes them more suitable for displacing. Due to the excellent electric properties of CNTFET, the CNTFET are attractive for the nano electronic applications [4].

III. STATIC VERSUS DYNAMIC LOGIC

A. Static Logic

In Static Logic CNTFET design, at every point in time, each gate output is connected to either Vdd or Vss via a low-resistance path. Also, the outputs of the gate assume that all the time value of the Boolean function implemented by the circuit.
A Static CNTFET gate is a combination of two networks - the pull-up network (PUN) and the pull-down network (PDN) as shown in Fig.2. The function of the PDN is to provide a connection between the output and Vdd anytime the output of the logic gate is supposed to be **1**. Similarly, the PDN connects the output to Vss anytime the output is supposed to be **0**.The PUN and PDN networks are constructed in a mutually exclusive manner such that one and only one of the networks is conducting in steady state[12].

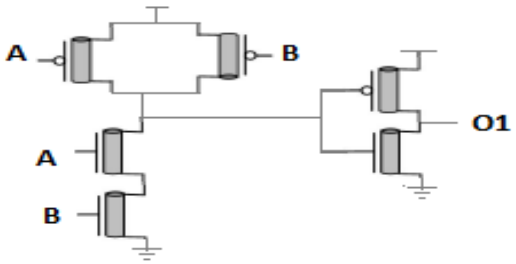

Fig.2. CNTFET based Static Logic AND Gate

The Static CNTFET gates have rail-to-rail swing, hence no static power dissipation. The speed of the static CNTFET circuit depends on the transistor sizing and the various parasitic that are involved with it. The problem with this type of implementation is that for N fan-in gate 2N number of transistors are required, i.e. more area required to implement logic. This has an impact on the capacitance and thus the speed.

B. Dynamic Logic

Dynamic CNTFET circuits rely on the temporary storage of signal values on the capacitance of high-impedance circuit nodes. These circuits also have no static power dissipation and use a sequence of precharge and conditional evaluation phases with the addition of a clock input as shown in fig.3. [8].

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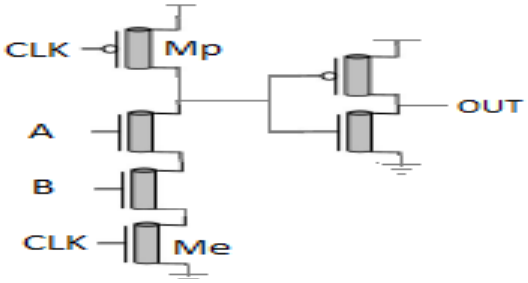

Fig.3. CNTFET based Domino Logic AND Gate

Pre-charge Phase :-
During this phase, the output node (OUT) is pre-charged to VDD through the pre-charge transistor Mp and CLK=0 during this time. At the same time, the evaluation transistor Me is OFF [6].

Evaluation Phase :-
With CLK=1, the pre-charge transistor Mp is in OFF state and the evaluation transistor Me is in ON state. The output depends on the input values and the pull-down path. Assuming the input is True or HIGH, the pull down network is ON and it makes the output pulled down LOW thus discharging the output node to ground through the footer device. The PDN remains in OFF condition, when the inputs are LOW or False. Hence, the pre-charged value on the output node (OUT) is retained. The primary feature of the dynamic circuits is that the evaluation can happen only once per every clock cycle [6].

The main advantages of the Dynamic CNTFET logic are increased speed and reduced implementation area. The problem with faulty discharge of precharged nodes in CNTFET dynamic logic circuits can be solved by placing an inverter in series with the output of each gate fewer devices are used to implement a given logic; this reduces the overall load capacitance and thus increases the speed.

IV. ALU DESIGN

ALU is the heart of any processor and is a part that is designed first. In digital electronics ALU performs arithmetic and bitwise logical operation on binary number system. It is essential block of central processing unit (CPU).

In digital circuit, digital calculation is done using binary logic i.e. low and high value (0 or 1) [3]. The efficiency of a processor greatly depends on the ALU [5]. The demand for high speed processing has been increasing as a r**e**sult of expanding computer and signal processing applications [5]. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing application [5].

In the 1-bit ALU shown in fig.4, it is a 3 function ALU block diagram. The logical operations are performed by the 2 input AND & OR gate while the arithmetic operations are performed by the full adder. The select lines are provided by a 4:1 Multiplexer through one out of 3 function can be selected.

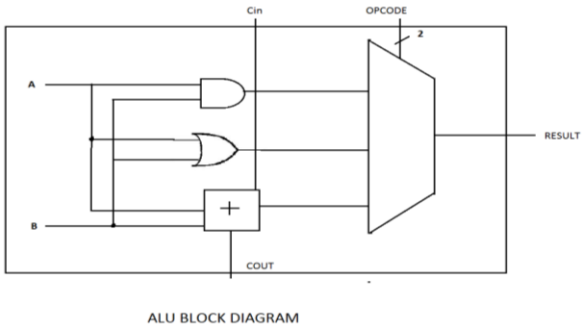

Fig.4. 1-Bit ALU Block Diagram [5]

V. STATIC 1-Bit ALU DESIGN

Fig. 5 shows schematic of Static 1- Bit ALU, it consist of both Pull Up and Pull Down Network. The Static Logic 1-Bit ALU is implemented using 70 CNTFETs. . Here in fig.5 A, B, C are inputs applied to circuit , result is taken through output node of the 4:1 multiplexer. The 1-Bit ALU is 3 function with 2 select lines of 4:1 Multiplexer for selecting logic Full Adder, OR logic, AND logic. The circuit consists of both static & dynamic parts, so the speed of operation of device is less than its Domino Logic counterpart.
Static 1-Bit ALU offers low power consumption as there are no load capacitance on the gate nodes as it does not use dynamic logic, which needs precharging and evaluation phases, resulting in higher power consumption.

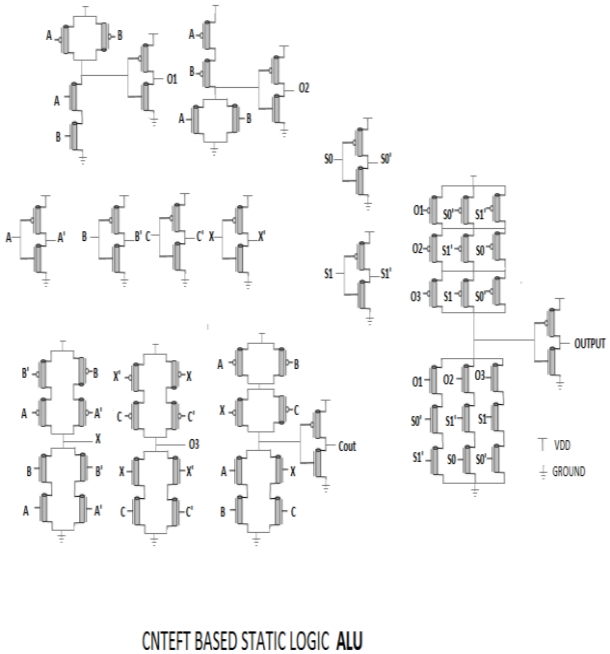

Fig.5. CNTFET based Static Logic 1-Bit ALU

VI. PROPOSED DOMINO 1-Bit ALU DESIGN

Fig.6 shows schematic of proposed Domino 1-Bit ALU, here only Pull Down Network is used, so the circuit consists of less number of CNTFETs. The pre-charge and evaluation phase allow navigation of data through circuit by changing of clock to 0 and 1 logic. The Domino 1-Bit

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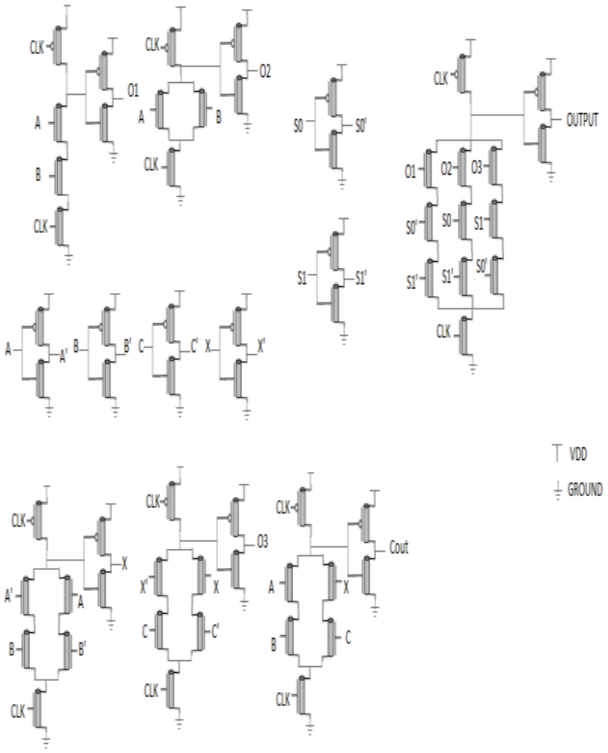
ALU circuit is implemented using 61 CNTFETs. Here in fig.6 A, B, C are inputs applied to circuit , result is taken through output node of the 4:1 multiplexer. The Domino 1-Bit ALU performs 3 functions, which are Full Adder logic, AND logic and OR Logic. The Functions of the 1-Bit ALU are performed through 2 select lines of the 4:1 Multiplexer .When Select lines S1, S0 is 00 AND Logic, when 01 OR Logic, when 10 Full Adder logic as shown in table I.

TABLE I
1-Bit ALU FUNCTION SELECTION

OPCODE		OPERATION
S1	S0	
0	0	AND LOGIC
0	1	OR LOGIC
1	0	FULL ADDER LOGIC



CNTFET BASED DOMINO LOGIC ALU

Fig.6. Proposed CNTFET based Domino Logic 1-Bit ALU

The Optimization of Domino 1-Bit ALU affects its speed of operation and average power consumption. The parameters varied for optimization are:-

A. CNTFET Diameter
It is varied changing various parameters that are i.e. varied changing the chirality vectors m and n as in eq. 1. Threshold voltage is inversely proportional to CNTFET diameter as shown in eq. 3, so starting operating voltage of the device can set.

B. Pitch of CNTFET
It is varied as it is related to gate capacitance device results in changes in speed, power consumption. With an increase in circuit speed, larger power consumption is often encountered, thus resulting in more heat at chip level.

C. Temperature Variation
Circuits with excessive power dissipation are more susceptible to run-time failures and account for serious reliability, thus Temperature variation is done to observe average power consumptions and delay under various temperatures.

VII. METHODOLOGY

The Static and Domino Logic 1-Bit ALU is simulated on HSPICE Software tool. For designing of any logic through HSPICE first its schematic is drawn according to the logic, then naming of the all the nodes in the circuit is done.
There are various model files available in HSPICE according to technology, which can be considered. The various characteristics of the circuit can plotted that are power, current, transient response through coding in HSPICE. In CNTFET model , the optimization of the circuit can be done changing the parameters in the code.
The metrics considered for comparative analysis are :

A. Average Power Consumption
It is power consumed by device logic from one state to another state. It denotes the power consumed by any circuit for its proper functioning. The unit of Power is in Watt.

B. Delay
The Delay, is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. The unit of Delay is in Second.

C. Power Delay Product
It is product of average power consumption and delay, PDP denotes the switching efficiency of the circuit. It shows how much effectively circuit work taking into consideration both speed and power. The unit of PDP is in Joule.

VIII. SIMULATION RESULTS

A. Comparative Analysis between CNTFET based Static and Domino Logic 1-Bit ALU
In this section, we present the results of HSPICE simulation using the CNTFET at 32nm technology. The comparison between Static and Domino Logic 1-Bit ALU are presented in table II, III and IV. The simulation are carried out with 1.0V supply voltage, 27 ℃ temperature and 1.4877nm CNTFET diameter.
The metrics for comparison are average power consumption, delay, power delay product. The graphs for comparison between Static and Domino Logic 1-Bit ALU are presented in Fig. 7, 8 and 9. The number of CNTFETs used for 1-Bit ALU implementation for Domino logic is

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61 as compared to 70 in Static Logic which results in area saving of 12.8%.

Table II depict that, Domino logic 1-Bit ALU(AND Logic) has 17.3% reduction in Delay, 14.1% reduction in Average power consumption, 29% reduction in PDP as compared to Static Logic 1-Bit ALU (AND Logic).

Table III depict that, Domino logic 1-Bit ALU(OR Logic) has 50.6% reduction in Delay, 12.3% reduction in Average power consumption, 56.8% reduction in PDP as compared to Static Logic 1-Bit ALU (OR Logic).

Table IV depict that, Domino logic 1-Bit ALU(Full Adder) has 38.6% reduction in Delay, 3.2% reduction in Average power consumption, 36.9% reduction in PDP as compared to Static Logic 1-Bit ALU (Full Adder).

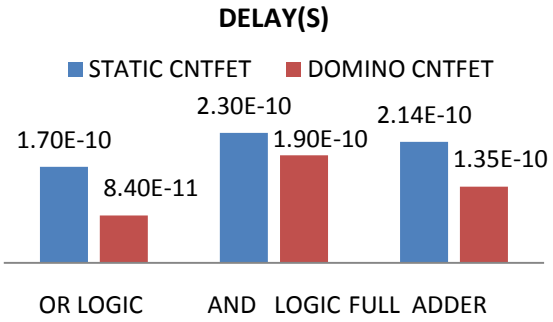

Fig.7. Comparison between CNTFET based Static and Domino 1-Bit ALU in terms of Delay

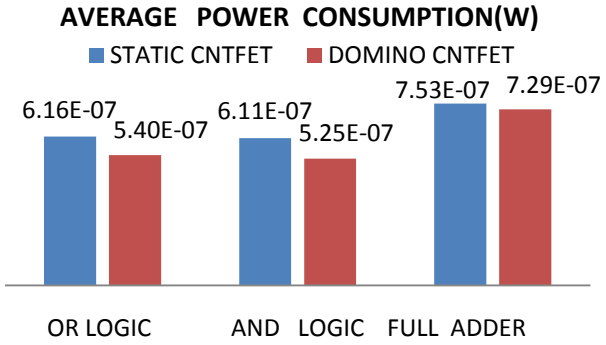

Fig.8. Comparison between CNTFET based Static and Domino 1-Bit ALU in terms of Average Power Consumption

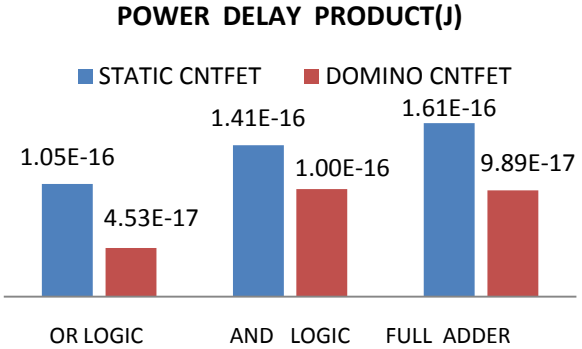

Fig.9. Comparison between CNTFET based Static and Domino 1-Bit ALU in terms of Power Delay Product

TABLE II
COMPARISON BETWEEN CNTFET BASED STATIC AND DOMINO LOGIC 1-Bit ALU(AND LOGIC)

Metric/ Technology	STATIC ALU (AND)	DOMINO ALU (AND)
Delay(s)	2.30E-10	1.90E-10
Average power consumption(w)	6.11E-07	5.25E-07
Power Delay Product(J)	1.41E-16	1E-16

TABLE III
COMPARISON BETWEEN CNTFET BASED STATIC AND DOMINO LOGIC 1-Bit ALU(OR LOGIC)

Metric/ Technology	STATIC ALU (OR)	DOMINO ALU (OR)
Delay(s)	1.70E-10	8.40E-11
Average power consumption(w)	6.16E-07	5.40E-07
Power Delay Product(J)	1.05E-16	4.53E-17

TABLE IV
COMPARISON BETWEEN CNTFET BASED STATIC AND DOMINO LOGIC 1-Bit ALU(FULL ADDER LOGIC)

Metric/ Technology	STATIC ALU (FULL ADDER)	DOMINO ALU (FULL ADDER)
Delay(s)	2.14E-10	1.35E-10
Average power consumption(w)	7.53E-07	7.29E-07
Power Delay Product(J)	1.61E-16	9.89E-17

B. Optimization of Proposed CNTFET based Domino 1-Bit ALU

In this section, the optimization of proposed Domino Logic 1-Bit ALU as shown in Fig.6 is carried out using HSPICE Stanford CNTFET at 32nm technology. Domino Logic 1-Bit ALU is optimized for analyzing its performance at different parameters. Optimization results are shown in the table V.

The results in table V shows Power delay Product(PDP) at 3 different temperature(27℃, 50℃, 75℃) with variation of CNT diameter 1.0179nm (m=13, n=0), 1.4877nm (m=19, n=0), 2.0358nm (m=26, n=0) and different pitch 5,10, 20nm . The optimization of proposed Domino Logic 1-Bit ALU(Full Adder Logic) has shown reduction in Power Delay Product by 33.2% at 5nm pitch as compared to Domino1-Bit ALU(Full Adder Logic) at 20nm pitch with CNT diameter at 1.487, 27℃ temperature and 94.2% at 1.0179nm CNT diameter at 5nm pitch.

From the three charts shown in Fig.10, 11, 12 of Power Delay vs Pitch for different diameter and temperature, we can observe that Power Delay Product will increase as temperature is increased. As pitch and CNT diameter is decreased Power Delay Product is also decreased. Also

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when diameter is 2.0358nm in the proposed Domino Logic 1-Bit ALU(Full Adder Logic), it has shown undesired output logic with opposite behavior of ideal performance as shown in Fig 12.

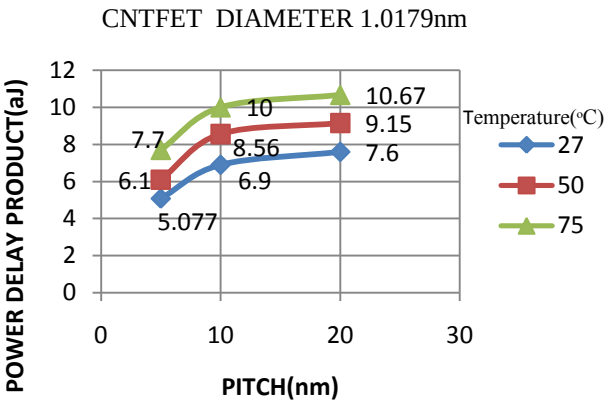

Fig.10. Comparison between Power Delay Product and Pitch for different CNTFET diameter 1.0179nm and different temperatures for proposed Domino 1-Bit ALU

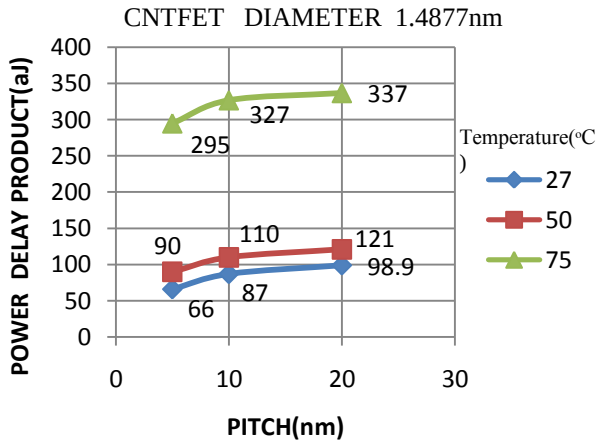

Fig.11. Comparison between Power Delay Product and Pitch for different CNTFET diameter 1.4877nm and different temperatures for proposed Domino 1-Bit ALU

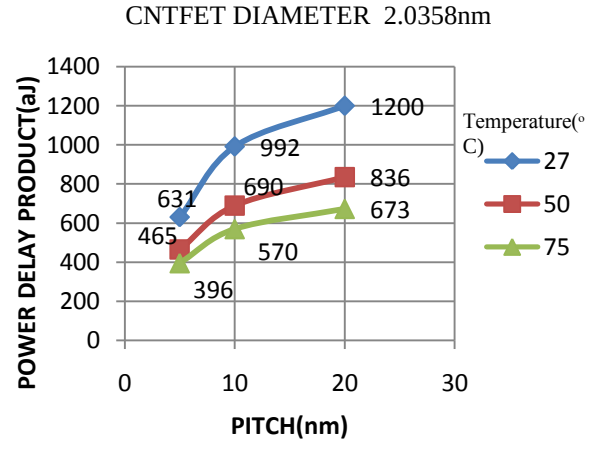

Fig.12. Comparison between Power Delay Product and Pitch for different CNTFET diameter 2.0358nm and different temperatures for proposed Domino 1-Bit ALU

TABLE V
OPTIMIZATION OF PROPOSED CNTFET BASED DOMINO LOGIC 1-Bit ALU(FULL ADDER LOGIC)

Temperature(°C)	Power Delay Product (attoWatt)								
	CNT diameter at 1.0179nm			CNT diameter at 1.487nm			CNT diameter at 2.0358nm		
	Pitch(nm)			Pitch(nm)			Pitch(nm)		
	5	10	20	5	10	20	5	10	20
27	5.077	6.9	7.6	66	87	98.9	631	992	1200
50	6.1	8.56	9.15	90	110	121	465	690	836
75	10.67	10	7.7	295	327	337	396	570	673

IX. CONCLUSION

In this paper, the number of CNTFETs used for 1-Bit ALU implementation for Domino logic is 61 as compared to 70 in Static Logic which results in area saving of 12.8%. Domino logic 1-Bit ALU(Full Adder Logic) has 38.6% reduction in Delay, 3.2% reduction in Average Power Consumption, 36.9% reduction in PDP as compared to Static Logic 1-Bit ALU (Full Adder Logic). The proposed and optimized design of Domino Logic 1-Bit ALU(Full Adder Logic) has shown reduction in Power Delay Product by 33.2% to 94.2%. It is also shown that Power Delay Product also depend on the diameter of the CNTs, pitch and temperature. The proposed CNTFET based Domino logic 1-Bit ALU can be further implemented in microprocessors and computational units.

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BIOGRAPHIES

Ashish Sharma, received B.Tech. degree from the Bharati Vidyapeeth College of Engineering, Delhi, India, in 2014, and M.Tech. Scholar from MRIU, Haryana, India in 2016. His current research interests include low power VLSI design, digital IC design and computer architecture, Embedded Systems and Networking.

Umesh Dutta, Assistant Professor and Deputy Director, MRIIC in Manav Rachna International University where he received many awards for teaching excellence and Researches done in various areas. His area of interest is in VLSI and Embedded Systems.

Sneha Arora, received B.Tech. degree from the Rajasthan Technical University, Kota, Rajasthan, India, in 2012, and M.Tech. from MRIU, Haryana, India in 2015. Her current research interests include interesting problems in device modeling, simulation of multigate transistors, as well as low power digital circuit design, and computer architecture/VLSI implementations of architectural ideas, and Embedded Systems, Microcontrollers.

Vipin Kumar Sharma, received B.Tech. degree from the Bharati Vidyapeeth University, Pune, Maharashtra, India, in 2013, and M.Tech. from MRIU, Haryana, India in 2015. His current research interests include low power VLSI design, analog IC design and computer architecture, Embedded Systems and Robotics.

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