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Design and Analysis of Clock Recovery Circuit in 45nm Technology

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Abstract: Clock Recovery circuits are used to detect the transition in the received data and generate a periodic recovered clock. These circuits are used in high speed asynchronous communication systems. This paper presents the design of clock recovery circuit using analog pll in 45nm technology. The proposed circuit is designed keeping in mind some basic design goals which are nothing but the expected enhancement in those parameters which reflects the performance and robustness of the circuit. Such as- To shift the frequency from 2Ghz to 3Ghz, increase rise time by 20%, increase the data rate by 25%, To overcome drawbacks of earlier models, to maintain robustness of circuit, reduce area, To build a power efficient circuit. The proposed circuit consist of TSPC-DFF based phase frequency detector/XOR frequency detector, single ended/differential wide swing charge pump, ring VCO, low pass filter, TSPC based frequency divider(DFF based) .

Keywords: Clock recovery circuit, PLL, Phase Frequency detector, VCO, Charge Pump, Frequency Divider.

I. INTRODUCTION

Conventional clock recovery circuit using PLL consist of the following functional blocks-

1.)Phase Comparator/detector
2.)Loop Filter
3.)Voltage Controlled Oscillator(VCO)
4.)Frequency Divider

Phase Locked loop is an electronic circuit with a voltage or current driven oscillator that is constantly adjusted to match in phase (and thus lock on) and frequency of an input signal. PLL can be used to generate a signal, modulate, demodulate a signal, reconstitute a signal with less noise or multiply/divide a frequency. It is used at the receiver to recover the clock from the data. It is a negative feedback system. PLL is basically a form of servo loop. Although a PLL perform its actions on RF signal all the basic criteria for loop stability and other parameters are the same.
Conventional PLL consist of three basic elements- Phase Comparator/detector, Loop filter and VCO as shown in fig 1.1

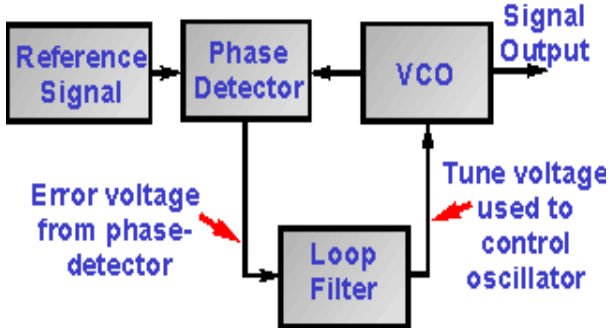

Fig1.1 **Phase locked loop basic diagram**

Phase detector compares the phase of two signals and generates a voltage according to the phase difference between the two signals. These are split into two categories- phase only sensitive and phase/frequency sensitive detectors.
Loop filter is used to filter the output from the phase comparator in the PLL. It is used to remove any high frequency components which might pass out of the phase detector and appear in the VCO tune line. They would then appear on the output of the VCO as spurious signals. The filter also affects the ability of the loop to change frequencies quickly. If the filter has a very low cut-off frequency then the changes in tune voltage will only take place slowly, and the VCO will not be able to change its frequency as fast. This is because a filter with a low cut-off frequency will only let low frequencies through and these correspond to slow changes in voltage level.

Conversely a filter with a higher cut-off frequency will enable the changes to happen faster. However when using filters with high cut-off frequencies, care must be taken to ensure that unwanted frequencies are not passed along the tune line with the result that spurious signals are generated. The loop filter also governs the stability of the loop. If the filter is not designed correctly then oscillations can build up around the loop, and large signals will appear on the tune line. This will result in the VCO being forced to sweep over wide bands of frequencies. The proper design of the filter will ensure that this cannot happen under any circumstances.
The voltage controlled oscillator is the circuit block that generates the output radio frequency signal. Its frequency can be controlled and swung over the operational frequency band for the loop. Within a phase locked loop, PLL, the performance of the voltage controlled oscillator,

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VCO is of paramount importance. This is because the VCO Voltage Controlled Oscillator performance determines many of the overall performance characteristics of the overall synthesizer. Basic design requirements of VCO are – VCO tuning range, VCO tuning gain, VCO voltage/frequency slope, phase noise performance.

II. PHASE LOCKED LOOP OPERATION

The reference signal and the signal from the voltage controlled oscillator are connected into the phase detector. The output from the phase detector is passed through the loop filter and then applied to the voltage controlled oscillator. The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.
The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency. The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

A. Limitations of Conventional PLL circuit
It includes the limitations of the individual functional components of the PLL circuit .
Limitations of Phase Detectors-
1.) Frequency Acquisition Can Be Slow
2.) Input Square Waves Required for Digital Phase Detectors => High Harmonics
3.) Divider Output Can Lock to Reference Harmonics Unless VCO Output Frequency Range is Limited
4.) Solution: Phase-Frequency Detection

Limitations of Loop Filters-
1.) High Frequency Noise
2.) High Power consumption
3.) Frequency limitation
4.) Poor Hold and Capture Range
5.) Poor switching speed of loop in lock

Limitations of Varactor LC VCO
1.) Large layout area → large area for inductor
2.) Narrow tuning frequency range
3.) Require a lot of characterization
4.) Poor integration and more complicated design

B. Proposed PLL circuit-
Keeping in mind the drawbacks and limitations of conventional PLL circuit we have redesigned the PLL circuit and simulated it in 45nm technology .The basic changes made in the circuit are –
1.) Replacement of Phase Detector with XOR Phase and Frequency Detector
2.) Single ended charge pump is used
3.) Varactor based LC VCO is replaced by Ring VCO
4.) TSPC based Frequency Divider is used in the feedback circuit(DFF based)

The following fig 1.2 shows the proposed circuit diagram of PLL

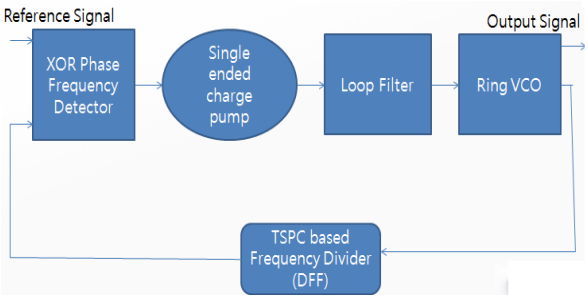

FIG 1.2 PROPOSED PLL CIRCUIT DIAGRAM

The following fig.1.3 shows the layout of complete phase locked loop (PLL) using Microwind3.1 VLSI backend software. The technology used is 45nm CMOS technology. This PLL is designed for 8.06 GHz. The total power consumption is 74.138 microwatt (uw) which can be seen in figure 1.4. The parametric analysis of voltage VDD with respect to frequency is shown graphically in fig 1.4. The data array for this graphical representation is shown in table 1.1. This table shows that frequency is remaining stable only up to 1.00 volt. As voltage rises above 1.00 volt, large change in freq observed. Means stability in frequency is obtained only up to the supply voltage of 1.0 volt

C. Layout and simulation results of Proposed PLL in 45nm Technology

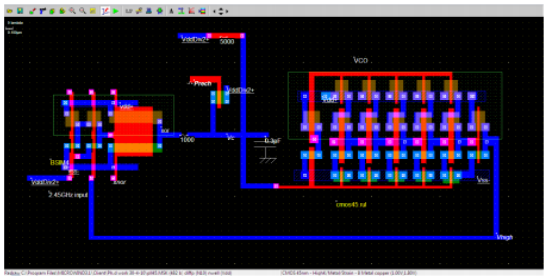

Fig 1.3 Layout of complete phase locked loop (PLL) using 45nm VLSI technology

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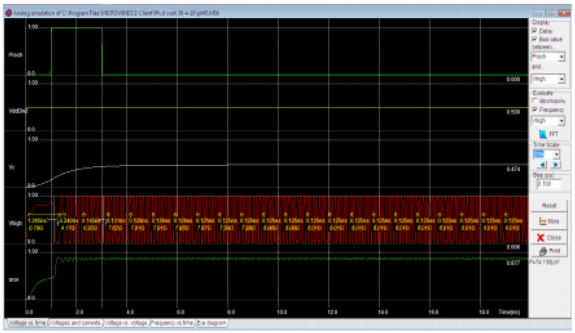

Fig1.4 Voltage verses time response of complete phase locked loop (PLL) using 45nm VLSI technology

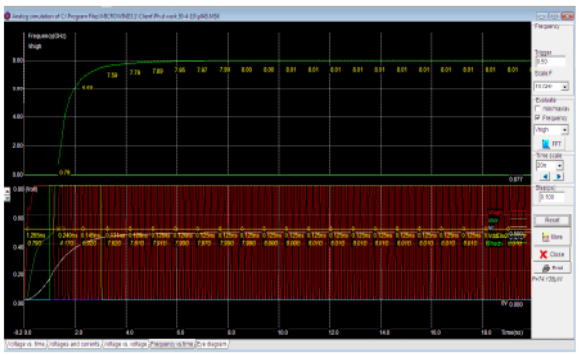

Fig 1.5 Voltage verses time response of complete phase locked loop (PLL) using 45nm VLSI technology

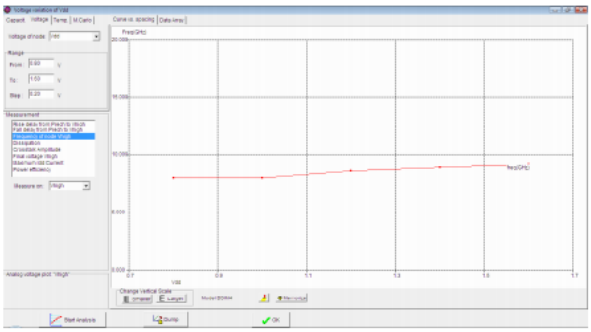

Fig 1.6 Voltage variation of VDD verses frequency of node Vhigh

Sr. No.	Vdd (volt)	Freq (GHz)
1	0.800	8.006
2	1.00	8.006
3	1.20	8.591
4	1.40	8.913

Table 1.1 parametric analysis of voltage VDD with respect to frequency

D. Layout and simulation results of Functional Blocks of Proposed PLL in 45nm Technology

In the proposed PLL Circuit Phase frequency Detector, Filter, Ring VCO, and TPSC based frequency divider is used.

1.) Layout and simulations of PFD in 45nm technology

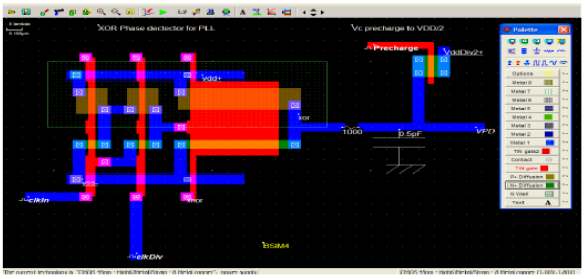

Fig 1.7 Layout of phase frequency detector with filter using 45nm VLSI technology

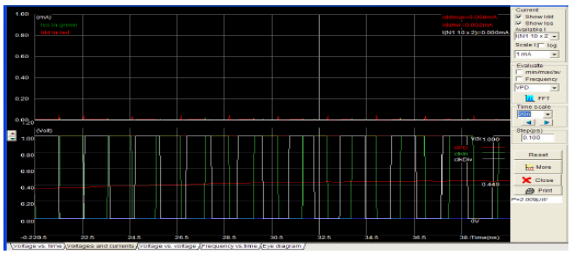

Fig 1.8 Frequency verses time response of phase frequency detector

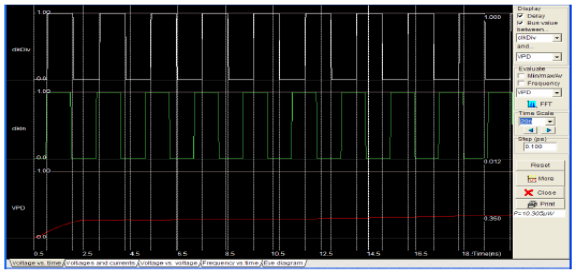

Fig 1.9 Voltage verses time response of phase frequency detector

Above fig 1.5 shows the layout of phase frequency detector with filter , designed by VLSI using 45nm CMOS technology. This layout uses a power supply of 1 volt DC with 8 metal copper connections. Fig 1.6 Shows frequency verses time response of phase frequency detector. The PFD output is found 0.449 volt. The total power consumption is 2.009 microwatt which is very low. Fig 5.8 gives the output of phase detector and filter in terms of voltage verses time diagram.

2.) Schematic, Layout and simulations of Ring VCO in 45nm technology

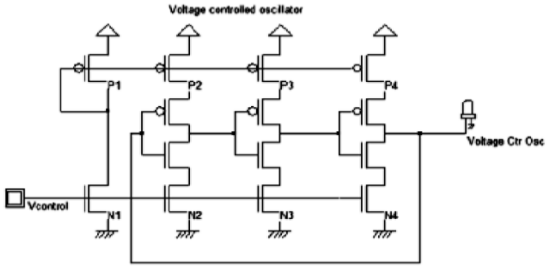

Fig 1.10 Schematic diagram of a voltage controlled oscillator

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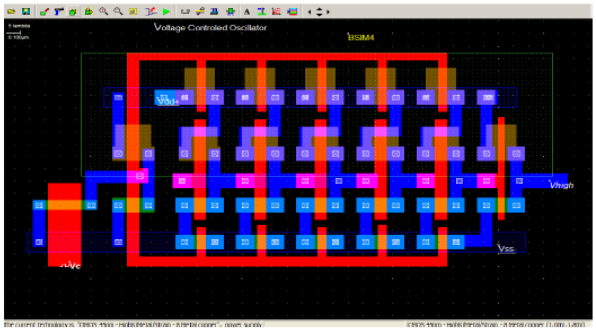

Fig 1.11 Layout of voltage controlled oscillator using 45nm VLSI technology

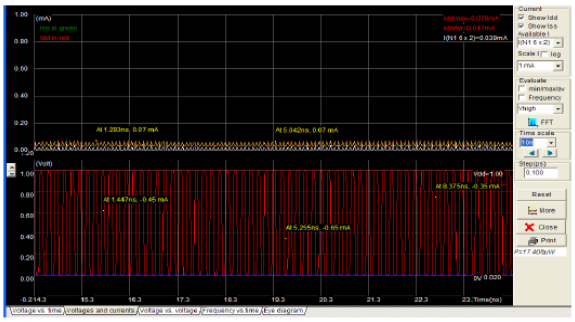

Fig 1.12 Voltage and currents of VCO with respect to time

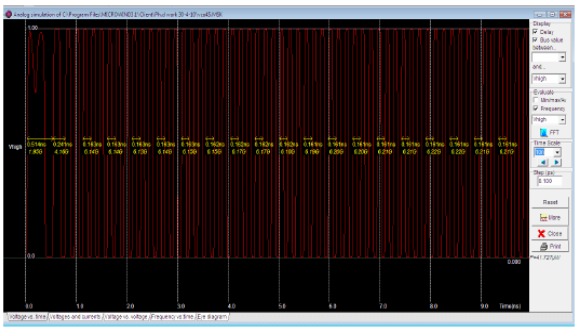

Fig 1.13 Output frequency of VCO verses time

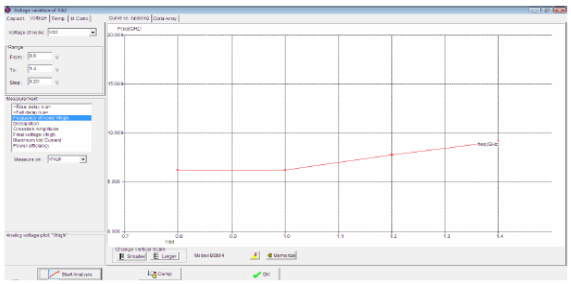

Fig 1.14 Voltage variation of VDD verses frequency of node Vhigh

Sr. No.	Vdd(V)	freq(GHz)
1	0.80	6.211
2	1.00	6.211
3	1.20	7.770
4	1.40	9.116

Table 1.2 Voltage variation of VDD verses frequency of node Vhigh

In the above VCO Circuit the supply VDD is chosen as 1.00 Volt DC supply. Vcontrol is the clock applied with low time (tl) = 0.225 ns, Rise time (tr) = 10 ns, High time (th) = 0.225 ns and full time (tf)= 10 ns. Vss is DC supply of 0.0V. NMOS transistor is having the width W = 0.120 µm and length L = 0.040 µm. The total power consumption of the circuit is P = 16.076 µw. The fig 1.9 shows layout for VCO, Fig 1.10 shows voltage and currents with respect to time. The output frequency Vhigh of VCO is shown in fig 1.11. From the data array shown in graph in fig 1.12 and as shown in table 1.2, it is found that frequency remain same i.e. 6.21 GHz upto 1.0 volt. As the supply voltage increases beyond 1.0 volt frequency get varied. Simulation of VCO layout is taken for frequency Vs time graph with timescale of 5nsec. The frequency obtained for VCO is 6.21 GHz. By increasing the no. of inverter and altering the size of the MOS current source, we may modify the oscillating frequency very easily.

3.)Layout and simulations of TSPC based frequency divider in 45nm technology

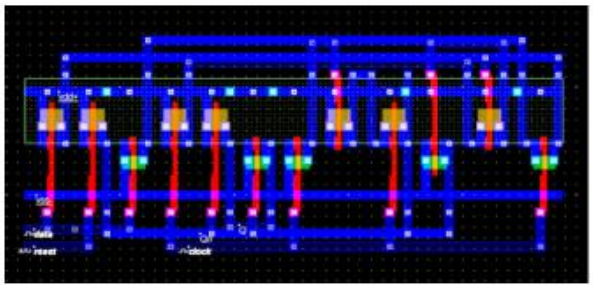

Fig 1.15 Layout of D-FF TSPC based frequency divider using 45nm technology

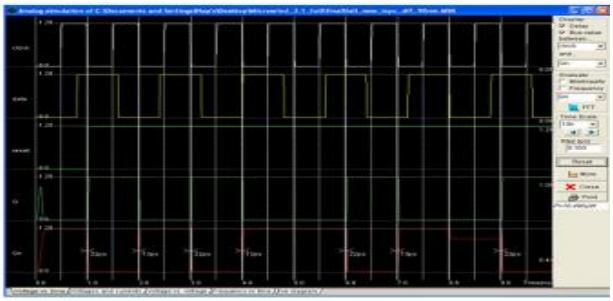

Fig 1.16 Simulation of D-FF TSPC based frequency divider using 45nm technology

4.)Schematic and simulation results of charge pump

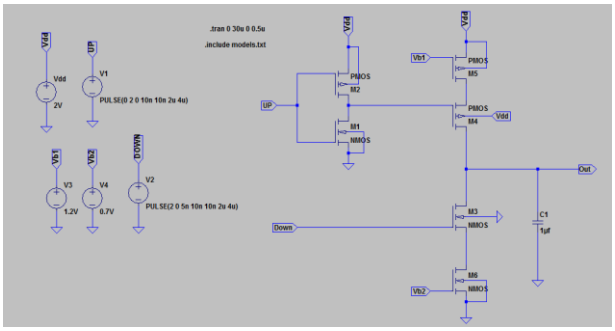

Fig 1.17 Schematic of single ended charge pump

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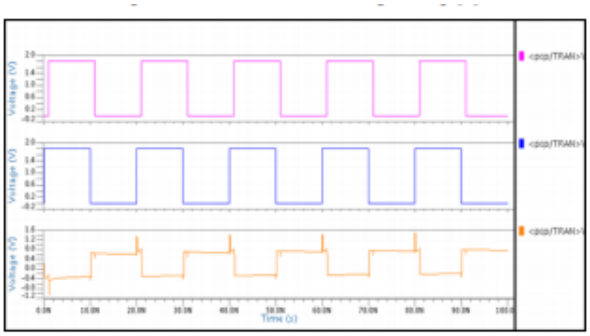

Fig 1.18 Waveform of Single ended Charge Pump

E. Advantages of current proposed PLL circuit in 45nm Technology

- Reduced noise and less jitter
- Reduced power consumption
- No offset voltage
- Very high frequency resolution (fclock/2N)
- Fast switching time
- Reduced layout area
- Wide Tuning Range

CONCLUSION

As shown above the proposed PLL based clock recovery circuit is able to overcome the limitations and drawbacks of the conventional PLL based clock recovery circuit.

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