IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 6, June 2016

Mapping of Turbo Encoded bits with 64-QAM modulator for spectral efficiency in LTE

Kajal Bambole[1], Rutuja Deshmukh[2], Neelam D. Deshmukh[3]

M.E. Dept. of E&TC, D. Y. Patil College of Engineering, Akurdi, Pune, India[1]

Assistant Professor, Dept. of E&TC, D. Y. Patil College of Engineering, Akurdi, Pune, India[2]

H.O.D Dept. of E&TC, Vice Principal, Priyadarshini Polytechnic College, Nagpur, India[3]

Abstract: In turbo-coded transmission systems, several ways of allocating the bits generated by the turbo encoder can be considered. Thus the bits generated by turbo encoder can occupy different positions in the modulator input symbol. In this paper, we have considered the performance of transmission systems, in terms of bit/frame error rate with respect to signal to noise ratio (BER/FER vs SNR) for both single binary turbo code of the LTE standard with coding rates 1/3 and 2/3 and also double binary turbo code of the DVB-RCS2 with coding rate 2/3. The simulation results show that different investigated allocation methods affect the performance of bit/frame error rate with respect to signal to noise ratio of the turbo coded system. The simulation result provides certain conclusions for the selection of best allocation methods, both in waterfall region and error floor region.

Keywords: turbo codes, modulation, QAM, LTE.

I. INTRODUCTION

Quadrature amplitude modulation (QAM) offers high spectral efficiency; hence it is frequently used in current communication systems. Variants of QAM are used in digital cable television or wireless and cellular technology applications. Most of the communications standards (LTE, DVB, deep-space communications, etc) use digital modulation together with the turbo-coding in order to assure error protection. It provides a good compromise between the bit/frame error rate (BER/FER) versus signal to noise ratio (SNR) performance and bandwidth efficiency [1]. For uncoded system 64-QAM gives a symbol error rate of $10^{-6}$for a SNR of about 19 dB. However, using a turbo code, a BER of 10^{-10} can be obtained at a SNR of 9 dB. 64-QAM technique with gray allocation can be used to minimize the BER[2].

In QAM modulations with gray allocation the bits of symbol modulator are not uniform protected. This non uniform protection is the characterization of square 64-QAM modulation. The important thing here is the mapping between the encoder and the modulator. Encoded symbol bits must be better protected by the QAM in order to obtain a better system performance. We have analysed the performances obtained using three mapping modes between encoding and modulation. The aim of the investigation was to evaluate the effect of different possible allocations on the performance of proposed transmission system. We also take into account the puncturing used in system, considering different coding rates. The structure of this work is organised as follows. In section II we have presented the turbo encoders used in this paper. Section III describes square 64-QAM and in section IV we proposed several ways of allocating turbo coded bits with modulator. Section V shows the simulation results and section VI concludes the paper.

II. THE TURBO ENCODER

The composition of the turbo coded block is determined by the structure of the turbo encoder and puncturing matrix. This section describes the SBTE specified in [3] and the DBTE specified in [4], as well as the puncturing matrices used to derive coding rate 2/3.

A. Single binary turbo encoder

The structure of SBTE is shown in fig. 1. Input sequence u is encoded directly by the convolutional encoder C1 and via interleaver (π) by the encoder C0. Depending upon the requirement, the outputs of the two convolutional encoders are punctured to obtain higher coding rate.

It follows redundant sequences x_0 and x_1, which, along with the original information sequence $u = x_2$ form SBTE's output. In the absence of puncturated, the (natural) encoding rate of SBTE's is 1/3. At this rate, the turbo coded block size is 3XN where N is the length of interleaving.

In other words, one turbo coded block consists of N symbols of the form $x_j = (x_2^j, x_1^j, x_0^j)$, with j from 0 to N_s-1. To obtain the coding rate 2/3 we have used the punctured matrix.

$$M_{ps} = \begin{bmatrix} 1 & 00 & 0 \\ 0 & 10 & 0 \end{bmatrix} \qquad (1)$$

which applies to sequences x_1 and x_0 . In this way the structure of turbo coded block is of the form:

$$\begin{array}{ccccccc} \ldots & x_2^j, & x_2^{j+1}, & x_2^{j+2}, & x_2^{j+3}, & \ldots \\ \ldots & x_1^j, & , & , & , & \ldots \\ \ldots & , & x_0^{j+1}, & , & , & \ldots \end{array}$$

with j from 0 to ($N_s/4 - 1$)

IJARCCE

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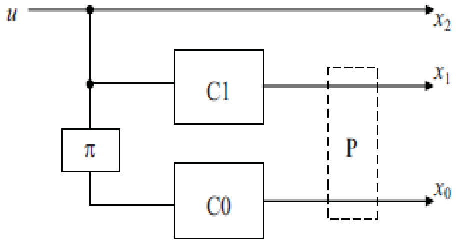

Fig. 1.The scheme of a SBTE.

B. Double binary turbo encoder

Fig. 2 shows the scheme of a DBTE. DBTE generates a four-bit symbolsx_j = (x_3^j , x_2^j , x_1^j , x_0^j) at its natural rate 1/2. In this case the size of a turbo coded block is $4XN_D$where $N_D$is the length of inter-symbol interleaving.

To obtain the same coding rate 2/3 for DBTE we have used the punctured matrix

$$M_{pd} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \qquad (2)$$

which also applies to sequences x_1 and x_0. The structure of a turbo coded block is of the form:

$$\begin{array}{l} \dots\ x_3^j,\ x_3^{j+1},\ \dots \\ \dots\ x_2^j,\ x_2^{j+1},\ \dots \\ \dots\ x_1^j,\ \dots \\ \dots,\ x_0^{j+1},\ \dots \end{array}$$

with j from 0 to (N_d/4 – 1)

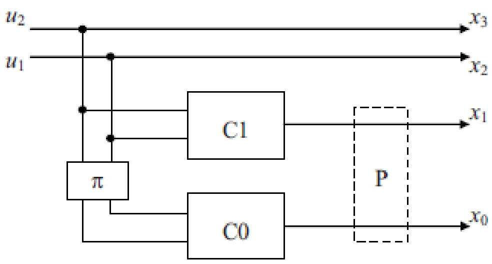

Fig2.The scheme of a DBTE.

III. THE SQUARED 64-QAM

The signals chart for 64-QAM square modulation is presented in Fig.3 and the signal modulated has the form:

$$s_j(t) = p_j \cdot \varphi_1(t) + q_j \cdot \varphi_2(t),\ j \in \{1,2,\dots,64\}, \qquad (3)$$

where $\varphi_1(t)$ and $\varphi_2(t)$ are in-phase and quadrature carriers of unitary energy. Due to the "squared" shape of the signals constellation in Fig. 3, the values of the coefficients pj and qj can be separately established, from the set {–7, –5, –3, –1, 1, 3, 5, 7}m0, depending on three of the six bits of the modulating symbol, mj, where:

$$mj = [aj,\ \alpha j,\ bj,\ \beta j,\ cj,\ \gamma j],\ \ j \in \{1,2,\dots,64\} \qquad (4)$$

So, the bits αj and aj determine the sign of the coefficients pj and qj, while the triplets (βj, γj) and (bj, cj) determine their module, with γj and cj playing the role of the most significant bit, and γj and cj playing the role of the least significant bit. Thus, the 64-QAM square modulation will protect differentiated the bits of mj. The most protected bits will be the sign bits, (βj, γj) then bits from the pairs (βj, cj) and (γj, cj).

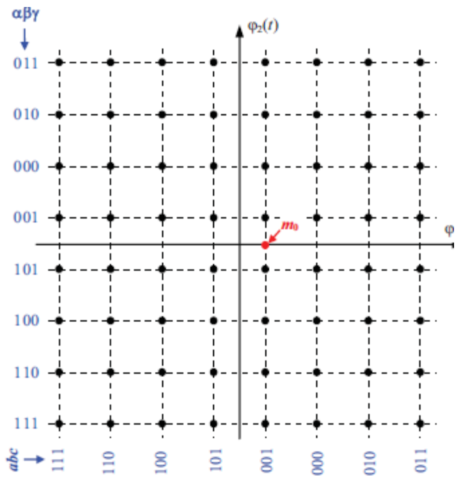

Fig3.Signal points constellation for square 64-QAM with Gray allocation.

IV. MAPPING BETWEEN TURBO ENCODER AND 64-QAM

This section describes interconnection ways (interfacing) between the turbo encoder and modulator. For each turbo code and coding rate we have chosen three allocation ways, indicated by acronyms q0, q1 and q2, respectively. On the complete labeling of variants we have noted the SBTC with s, the DBTC with d and the encoding rates 1/3 and 2/3 with 33 or 67, respectively.

A. CMBM variants for SBTC

Variants of coding to modulation bit mapping (CMBM) for SBTC with coding rate 1/3 are shown in Table I. Since the natural coding rate of SBTC is 1/3, in this case the bits allocation for in-phase component is identical to those of the quadrature component. What is different is only the position of the modulator symbol mjin which the information bit x2 will be placed. In the first case s33q0, x2 is the most protected bit (with role of ajor αj). In the second case s33q1, x2 is the middle bit (with role of bjor βj) and in s33q2 case, x2 is the least protected bit (with role of cjor γj). CMBM variants for SBTC with the coding rate 2/3 are shown in Table II. In order to obtain similar situations as in the case above (with two parity bits and one bit of information) for in-phase component, on the quadrature component we just placed information bits. Thus, the cases in Table II differ only in-phase component. These are similar to the case of the rate 1/3 SBTC.

B. CMBM variants for DBTC

Coding rate of 2/3 is only used for DBTC. CMBM variants in this case are shown in Table III. Because of the symmetry, we chose the symbol bits (generated by DBTE) with even index to be assigned to in-phase component and the symbol bits with odd index to beassigned to odd symbols. By doing so, we will have 2 information bits and

DOI 10.17148/IJARCCE.2016.56168

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

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Vol. 5, Issue 6, June 2016

only one parity bit for triplets (ajbjcj) and (αjβjγj). The cases chosen and presented in Table III differ by positioning the parity bit.

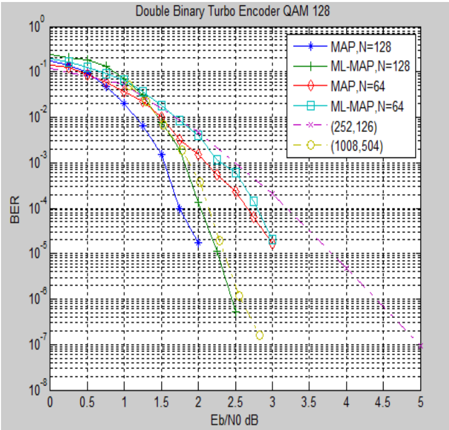

Fig. 4. The performances of memory 4 SBTC from [2] with the coding rate Rc= 1/3 and CMBM modes

TABLE I
CMBM VARIANTS FOR SBTC AND A CODING RATE OF 1/3

	a_i, α_i	b_i, β_i	c_i, γ_i	protects
$s33q0$	x_2	x_1	x_0	information
$s33q1$	x_1	x_2	x_0	hybrid
$s33q2$	x_1	x_0	x_2	parity

TABLE II
CMBM VARIANTS FOR SBTC AND A CODING RATE OF 2/3

	in-phase			quadrature		
	a_j	b_j	c_j	α_j	β_j	γ_j
$s67q0$	x_2^j	x_1^j	x_0^{j+1}	x_2^{j+1}	x_2^{j+2}	x_2^{j+3}
$s67q1$	x_1^j	x_2^j	x_0^{j+1}	x_2^{j+1}	x_2^{j+2}	x_2^{j+3}
$s67q2$	x_1^j	x_0^{j+1}	x_2^j	x_2^{j+1}	x_2^{j+2}	x_2^{j+3}

TABLE III
CMBM VARIANTS FOR DBTC AND A CODING RATE OF 2/3

	in-phase			quadrature		
	a_j	b_j	c_j	α_j	β_j	γ_j
$d67q0$	x_3^j	x_2^j	x_1^j	x_3^{j+1}	x_2^{j+1}	x_0^{j+1}
$d67q1$	x_3^j	x_1^j	x_2^j	x_3^{j+1}	x_0^{j+1}	x_2^{j+1}
$d67q2$	x_1^j	x_3^j	x_2^j	x_0^{j+1}	x_3^{j+1}	x_2^{j+1}

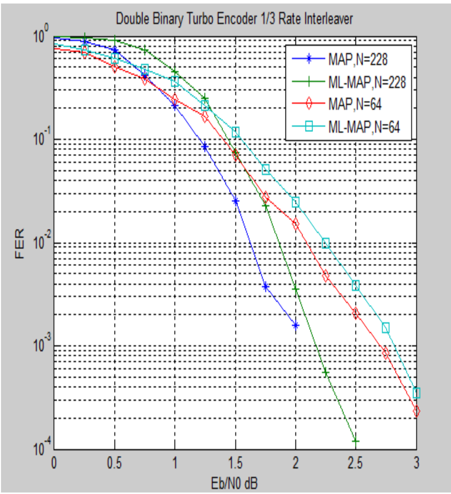

Fig. 5. The performances of memory 4 SBTC from [2] with the coding rate Rc= 2/3 and CMBM modes

V. SIMULATION RESULTS

The simulation results are shown in Fig. 4 and Fig.5 . For each point of curves shown in the diagrams of these figures, we have carried out simulations to obtain 500 erroneous blocks or to process a number of 10^9 data blocks. The CMBM investigated variants were those shown in Table II.The cause of this fact is the presence, in turbo coded block, of a much larger number of information bits in relation to the parity bits. Furthermore, in all CMBM variants of Table II we opted to send on carrier (the quadrature one) only information bits. The hierarchy previously set is kept both for waterfall and error floor regions in this case, too.

VI. CONCLUSION

The results presented in the previous section led us to several conclusions. First, note that by carefully choosing the CMBM variant we can influence with almost 1 dB the performance of TC. This effect depends on the coding rate: itis great for a coding rate equal to or close to the natural rate of TC and decreases while coding rate departs of the natural rate. A second conclusion drawn from the analysis of our results is that the best performance in waterfall region is obtained with maximum protection on information bits for the 64- QAM. However in the error floor region, we have the contrary result: better performance is achieved through a preferential protection for parity bits. In this case matters the number of iterations performed. In other words, to reduce the error floor phenomena (to achieve very small FERs) it is recommended to protect the parity bits, through 64-QAM, and to increase the number of iterations.

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BIOGRAPHIES

Kajal N. Bambole received his B.E. degree in the year 2013 from SSBT college of engineering and technology,Jalgaon, North Maharashtra University, in Electronics & Telecommunication. Currently he is pursuing his M.E. in Communication Networks from D. Y. Patil College of Engineering, Akurdi at SavitribaiPhule Pune University. His research interest includes Long Term Evolution.

Mrs. Rutuja A. Deshmukha Research Assistant in Electronics and Telecommunication Department, D. Y.Patil College of Engineering, Akurdi at SavitribaiPhule Pune University. She received her B.E. degree from Raisoni Engineering College in Electronics & Telecommunication and Master's degree from Priydarshani Engineering College at Nagpur University in VLSI. Her research interest is Signal Processing, VLSI.

Dr. Mrs. Neelam D. Deshmukh is Vice-Principal, HOD E&TC, at Priydarshani Polytechnic College, Nagpur. She received her Bachelor's Degree from VNIT, Nagpur.