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Addressing of Electromagnetic Interference Aspects in VLSI design

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Abstract: This paper presents the theoretical aspects of electromagnetic interference issues in very large scale integrated circuit development. Primarily, the development of integrated circuits, various noise causing factor and numerous associated technologies in VLSI towards electromagnetic compatibility achievement. Here we intend to illustrate trends in CMOS technology and its consequences on electromagnetic compatibility (EMC) and all possible issues.

Keywords: VLSI, electromagnetic, CMOS, electromagnetic compatibility (EMC)

I. INTRODUCTION

Over the past four decades , electromagnetic compatibility (EMC) concerns have raised in importance as low emission from and high immunity to interference have emerged as key differentiator in the overall IC performances. Progresses in process integration, higher switching speeds and more complex circuits tend to increase the amount of RF emission generated by ICs. Reduced supply voltage and increased number of interfaces tends to decrease the immunity to radio-frequency and impulse interference. EMC has become one of the major causes of IC redesign, mainly due to inadequate design methods and lack of expertise on noise reduction and immunity improvements. Specific workshops and dedicated sessions in major conferences have enhanced this dialogue and have initiated knowledge exchange within the IC-EMC community. With the IEC international standardization committee, applicable standards have emerged both for IC emission [1] and susceptibility characterization [2] as well as IC EMC modeling [3]. The idea of an EMC roadmap following progresses in IC manufacturing technology has emerged from several experts. In close relation with IC-related standardization committees over recent years, the EM environment of ICs has gone through a gradual process of expansion in terms of frequency bandwidth utilization, power used in wireless communications, and signal modulation complexity. The need for low-emission and highly immune ICs within the frequency band of GHz rapidly, putting IC support engineers and designers under extraordinary pressure.

The increasing demand for high speed and high performance integrated circuit (IC) systems has been a driving force for increasing the speed and performance of metal oxide semiconductor field effect transistors (MOSFET) devices which constitute the IC. The increase in the speed of the MOSFET devices has primarily been enabled due to reduction in their sizes. However, this reduction in the MOSFET device sizes has been accompanied by a proportional reduction in the cross sectional area of the metal interconnects used for communication on an IC dies as [1]. The increased system complexity, density and die size of a typical planar IC, coupled with the reduction in the cross-sectional area of metal interconnects, have increased the parasitic effects associated with interconnects. The global metal interconnect lines are now considered as a bottleneck to the increase in IC speed as the delay due to interconnects is higher than the delay due to the MOSFETs [4]. Certain conventional design approaches used by the semiconductor industry to mitigate this problem include increasing the interconnect width (i.e. reverse scaling of interconnects) and changing the inter layer dielectrics (ILD) on the die to low dielectric materials [3]. However, these design approaches only increase the life time of the global interconnect system by a few technology generations [4].

In contemporary design approaches, 3D integrated circuits (3DICs) are considered as a viable solution to alleviate the problems posed by the scaling of metal interconnects in planar integrated circuits (ICs). Depiction of semiconductor technology scaling length of the interconnects between two communication endpoints thereby increasing demand for high speed and high performance integrated circuit (IC) systems has been a driving force for increasing the speed and performance of metal oxide semiconductor field effect transistors (MOSFET) devices which constitute the IC. The increase in the speed of the MOSFET devices has primarily been enabled due to reduction in their sizes. However, this reduction in the MOSFET device sizes has been accompanied by a proportional reduction in the cross sectional area of the metal interconnects used for communication on an IC die as [4]. The increased system complexity, density and reducing the interconnect delay

[5]. Another possible alternative for a global communication network on a chip is to use radio frequency (RF) interconnects. There are two (2) types of RF IC interconnects of note: The micro-strip transmission line based interconnects operating in the RF range [6] and the wireless communication based intra-chip interconnects operating in the RF range [7]. This chapter focuses on the electromagnetic compatibility (EMC) of the on-chip antennas with the complementary metal oxide semiconductor (CMOS) digital circuits for a typical 9-metal layer 40 nm CMOS technology.

II. METHODOLOGY

The methodology presented in this work can also be used to investigate the electromagnetic compatibility of the on-chip antennas optimized for RF communication functionalities on radio frequency integrated circuits (RFICs) or system-on chips (SoCs).

A .The effect of the metal interconnects on the antenna characteristics [8,9],

B .The effect of the electromagnetic radiation from the on-chip antennas on the MOSFET devices [9],

C .The effect of the electromagnetic radiation from the on-chip antennas on the metal interconnects [9].

In [8], it has been tried to show that the presence of metal interconnects placed on the same metal layer as that of the antenna in parallel orientation to the antenna decreases the antenna gain in the lower frequency range and increases it in the mid-band and high frequency ranges. However, the change in the gain is not very large and does not have a major influence on the transmission gain. In other words, the presence of the metal interconnects shifts the response to a higher frequency range. However, the percentage metal utilization of the metal layers considered in [8] is very low and untypical of ICs. Researchers have also found it that transmission gains reduce substantially for higher percentage utilization [9].

The effects of the radiation from the antennas of the wireless interconnect system on the MOSFET devices has been discussed in [9]. It is shown in [7] that the effect of the radiation on the leakage current of the MOSFET devices is very low and can be neglected. However, the effect of the EM radiations on the MOSFET device alone and neglects the effects of the electromagnetic interaction with the metal inter connects. The functionality of the CMOS digital circuits can also be affected due to the signal coupling with the metal interconnects. It has been found that the majority of the wave propagation happens in the substrate and through surface waves. Since there are local metal interconnects present in the same metal layer as that of the antenna, substantial amount of power can be transmitted to these interconnects from the radiations [9]. Hence, it is critical to analyze the signal coupling between the antenna and the metal interconnects. Since the metal interconnects are essentially micro-strip elements, the signal coupling depends on the dimensions of interconnect. The signal coupling between the on-chip antennas and the metal interconnects can be characterized for varying width, length and placement of the metal interconnect [9]. It is also possible to have a good electromagnetic compatibility for the on-chip antennas. Though [9] investigates the signal coupling between the on chip antennas and the metal interconnects, it does not consider the effect of this signal coupling on the CMOS digital circuits. The criticality of the analysis of the antenna electromagnetic radiation effects on the CMOS digital circuits significantly increases for deep sub-micron technologies as VDD and noise margins for these technologies are scaled down significantly.

Electromagnetic interference (EMI) problems have been a great concern in high-speed digital systems and plenty of works have been done to handle the electromagnetic compatibility (EMC). Depending on different propagation approaches, they have conducted EMI noise, capacitive/inductive coupling EMI noise, and radiated electromagnetic (EM) wave noise. Conducted and coupling EMI problems have been studied most in the literature since fast operation and large integration scale started making the interconnect effect an important issue in high-speed systems two decades ago. , the behavior of integrated circuits in the presence of GHz-range interference was not extensively studied. In 2000, an updated version of the Integrated Circuit Electromagnetic Immunity Handbook published by NASA gave valuable information on the immunity levels of simple integrated circuits up to 10 GHz [10].

III. Electromagnetic aspects in IC's

The electromagnetic interference (EMI) on IC was initiated (1965) in defense[11], However, limited by their own state of the art technology, EMC problems in IC were not seriously considered until the 1980s where the EMC performance of IC's was Important. Thus, over past 30 years, IC's have become key elements of electronic devices where EMI/EMC issues are concerned. A typical high speed PCB contains numerous IC's. When operating, those IC's are considered as noise source and high susceptibility of an integrated circuit [12] are two essential performance requirements for IC EMI compliance.

Driven by high clock speed and circuitry complexity, parasitic emissions in ICs contribute the most of interference phenomena. Conduction emissions are generated by high transient currents, which leak from the digital core through silicon tracks, bonding wires and package lead frames. Unwanted radiation may propagate as a result. Electromagnetic fields, which radiate from internal interconnects or the package frame, are referred to as radiated emissions. The recent trend of portable, wireless electronic devices (i.e. mobile Phone, radar GPS Wireless network etc.) has resulted in ICs being non-responsive to radiated emissions in parasitic radio frequency sources which may aggress integrated circuits [12]. A high level of susceptibility is needed for the utilization of modern ICs. It has been stated that ICs are more susceptible to higher radio frequency interference [13] when the operation frequency increases. The decreasing supply voltage reduces the noise margin while

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the IC will be most easily affected by low amplitude RFI. Consequently, a researcher's goal is to develop high performance ICs with low emission and high susceptibility. Due to the complexity of an integrated circuit system, it is split into several parts for specific study. A hierarchical decomposition of a typical IC Is displayed. The effects of each component is widely studied in EMC scientific research. There are five elements of primary concern in the area of EMC problems in ICs. These include the die, package, I/Os, Heat sink and PCB. Among them, the parasitic effect is caused by internal connection crosstalk and simultaneously switching noise. The integrated circuits (IC) packaging technology is being rapidly developed as process technology improves other components related to intergraded circuits are consequently involved to the consideration of electromagnetic issues as well.

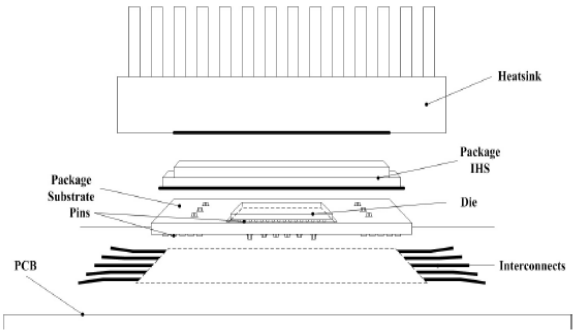

Figure 1 hierarchical decomposition view of electronic system.

As shown in Fig 1 and Fig 2 are elaborate the hierarchical de composition of electronic systems which will knowing the basic parameters effecting due to high frequency operation and so many parameters will effect which will leads to undesired and distorted characteristics like radiation emission and conduction emission etc .

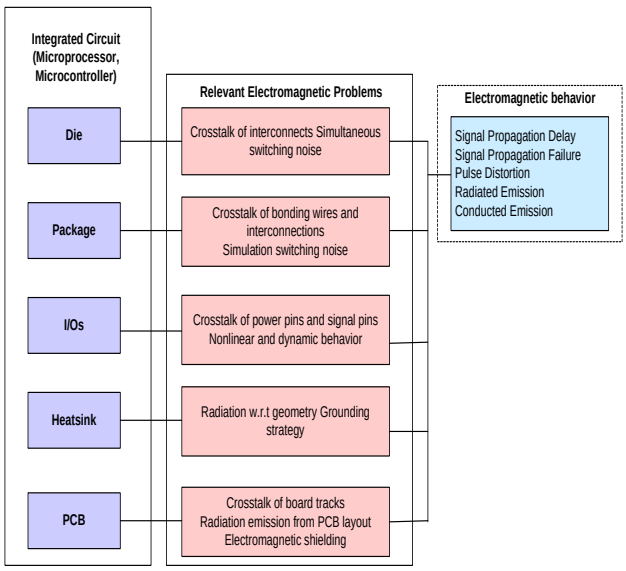

Figure 2 - electromagnetic problems existing in the electronic systems

A. Internal noise on DIE

The die is an internal semiconductor core, which performs all functions of the IC. Following the shrinking of semiconductor technology and clock speed improvement, crosstalk and simultaneous switching noise (SSN) are becoming more significant and are affecting signal integration. The Noise coupling provokes faulty in the integrated circuit, mostly in digital cores. A brief discussion on the predominant issues in IC design such as crosstalk and SSN is given in the following section:

B. Cross talk

Crosstalk has been a very common problem in IC design for half a century. It is referred to as an undesired interference created by a signal transmitted on one circuit causing faulty behavior on a nearly devise. All of these noises are spatial correlations between signals, which destroy the hierarchy of the IC. Crosstalk is usually expressed in dB as in Crosstalk in

$$dB=20 \log \frac{V_c}{V_s}$$

where V_s is signal voltage in source circuit V_c coupled voltage in victim circuit.

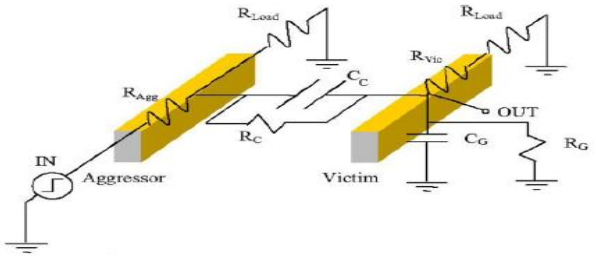

Figure 3 A simple crosstalk model for two aggressor and victim wires [17]

As the semiconductor process scale decreases and structural complexity increases, the reduction in distance between interconnections contributes to an increase in crosstalk noise. This consequently affects IC performance. A simple example of crosstalk between two connections is given in Figure 3, the coupled noise has been pointed out as a potential cause of failure in high speed electronic system since 1967 [14] IC provokes malfunction of the IC by affecting the propagation delay of the logic and analog cells. An evolution of parasitic capacitive coupling affects is modeled by [15] which show how crosstalk influences behavior of basic IC functions. Moreover, the coupling capacitance between adjacent lines is becoming a significant fraction of the capacitance to the substrate due to the aggressive scaling between adjacent interconnects that leads to an increase in coupling noise [16].With the implementation of sub-micron and deep-micron technologies, crosstalk prediction is becoming important of the design phase. To reduce and prevent crosstalk noises, consideration of hierarchy structures and nonlinear IC behaviors is needed, with additional physical and timing constraints in the specific model. In the early stage of design the optimization strategy of buffer planning is needed for better noise reduction during floor planning

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[18]. The simultaneous buffering and shielding insertion can also be employed in global outing [19]. With more detailed information of the physical layout given in the post design phase, various efficient crosstalk reduction techniques have been developed through studies of known circuit properties. By appropriate adjusting the driving gate size of the aggressor and victim net the gate sizing method for crosstalk reduction can be accomplished [20][21][22]. In addition wiring size and spacing could also contribute to a reduction of noise given in [23] and [24].

C. Simultaneous Switching Noise

Simultaneous Switching Noise (SSN), which is also referred to Δl noise or ground bonus, is another significant parasitic effect caused by the simultaneous switching of millions of internal transistors. It generates faster and stronger steep current at the digital core level and is related to the increasing integration and rising operating frequency. It is relatively recent topic introduced by the sudden increase in IC clock speed and transistor number.

$$V = L\frac{di}{dt}$$

The bonus voltage V is proportional to inductor L and rate of current change di/dt between device ground and system ground. This means the faster the current switches, the greater the drop in voltage. Using single CMOS inverter, for example which is the most common gate is ICs a small transient current is produced in the pull-up network or pull-down network each type the logic level switches from 1 to 0 or 0 to 1. Due to the increasing number of logic cells in an IC, especially a high performance IC, this transient switching current could be significant and fatal to the circuit. Figure 3.4 illustrates transient current generation in a single CMOS inverter cell.

The SSN influences the circuit performance in numerous manners. Some of the predominant approaches are given as follows:

1. Leading to glitches on the ground and in the lower network
2. Degrading gate driven strength
3. Reducing the margin of overall system noise.
4.

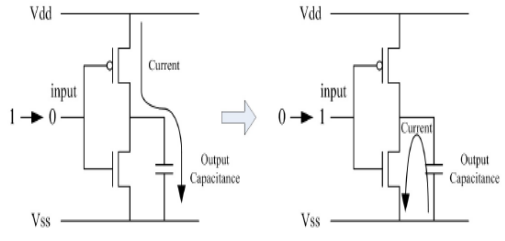

Figure 4 Switching current generation procedure

Due to rapid developments in process technologies, devices are becoming smaller and more sensitive to SSN. It has brought many new challenges to the internal interconnection network design with related SSN problems. Bus layout and coding efficiency have been carefully analyzed in [25] and [26] as the bus is taking a large percentage of distributed interconnections in the IC and is closely relevant to the SSN. Moreover, [27] and [28] have studied the design of power and ground distribution, taking into account the affects of wave propagation inductance and capacitance coupling by using an equivalent circuit model. The analytical expression characterizing the SSN voltage can be derived on the basis of a lumped, inductive-resistive-capacitive model in the design of internal power distribution networks of ICs [29], [30]. Furthermore, SSN at chip output drivers can be accomplished by using a simple metal oxide semiconductor field effect transistor [MOSFET] model. determining the SSN voltage on a ground rail based on the assumption of a fast ramp input signal [31].

Sample analytical expression of electromagnetic interference in sense of simultaneous switching noise, the following results of SSN is measured with reducing delay with varying the values of capacitances and inductances. The equivalent circuit therefore simplifies to the circuit shown in Fig. 4. and are the parasitic inductance, capacitance, and resistance of the ground rail, respectively. The input signal is for (1) After the input voltage reaches , the NMOS transistor turns ON and begins to operate in the saturation region. It is assumed that the NMOS transistor remains in the saturation region before the input signal transition is completed. The current through the NMOS transistor (2), the parasitic inductance ( ), and the SSN voltage ( ) are given, respectively, as

$$v_{in} = \frac{t}{\tau_T} v_{dd} \quad \text{for} \quad 0 \le t \le \tau_T \quad \text{----(1)}$$

$$I_N = B_n(V_{in}\text{-}V_{TN}\text{-}V_s)^n \text{---------- (2)}$$

$$V_s = R\,V_{ss}\,I_L + LV_{ss}(dI_L/dt) \text{----------(3)}$$

$$I_l = I_N\text{-}CV_{ss}(dV_s/dt) \text{ ---------- (4)}$$

Assuming that the magnitude of is small as compared to , can be approximated as

$$I_N \approx B_n(V_{in}\text{-}V_{TN})^n\text{-}(dI_N/dV_{gs})V_s \text{----------} \quad (5)$$

Rewriting (5)

$$F_1 = dI_N/dV_{GS} = nB_n(V_{in}\text{-}V_{TN}\text{-}V_s)^{n-1} \quad \text{..... (6)}$$

is a function of , i.e., for the case of an inverter. In order to simplify the derivation, is approximated using equal to 0.5 Combining (4) –(6)F_1 is a function of V_{GS}

$$L_{Vss}C_{Vss}(d^2V_s/dt^2)+(Rv_{ss}C_{Vss}+L_{Vss}f_1)(dV_s/dt)+(R_{Vss}f_1+1)V_s \cong R\,V_{ss}B_n(V_{in}\text{-}V_{TN})^n+L_{Vss}\,d/dt[B_n(V_{in}\text{-}V_{TN})^n] \text{----- (7)}$$

1st term of LHS in eq(7)

neglected and rest of two terms leads to

$$(Rv_{ss}\,C_{Vss}+L_{Vss}\,f_1)(dV_s/dt)+(R_{Vss}f_1+1)V_s \cong R\,V_{ss}B_nV^n{}_{dd}(t/T_r\text{-}V_n)^n+L\,V_{ss}B_nV^n{}_{dd}/T_r[(t/T_r\text{-}V_n)^{n-1} \text{---------(8)}$$

where .No closed form solution of this differential equation exists due to the non integer value of and In order to derive an analytical expression for the differential equation, and are approximated by a polynomial

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expansion to the fifth order, where the average error is less than 3%

$$\xi^{n} = a_0 + a_1\xi + a_2\xi^2 + a_3\xi^3 + a_4\xi^4 + a_5\xi^5$$

$$\xi^{n-1} = b_0 + b_1\xi + b_2\xi^2 + b_3\xi^3 + b_4\xi^4 + b_5\xi^5 \text{ -----(9)}$$

$$\xi = \frac{t}{Tr} - Vn \text{ , where } a_i, b_i \text{ are i=0,1,2,3,4 and 5}$$

Note that and for are independent of the input transition time . The solution of the SSN voltage is for

$$v_s = c_0(1 - e^{-(t-Tn)/\gamma\tau} +$$

$$c_2\xi^2 + c_3\xi^3 + c_4\xi^4 + c_5\xi^5 \text{ ----------(10)}$$

For $T_n \le t \le T_r$ where $\gamma = (Rv_{ss}\ C_{Vss}+L_{Vss}\ f_1)/(R_{Vss}f_1+1)T_r$----------(11)

$T_n=(V_{Tn}/V_{dd})T_r=V_nT_r$----------(12)

These coefficients are Coefficients are

$$c_0 = A_0\gamma - A_1\gamma^2 + 2A_2\gamma^3 - 6A_3\gamma^4 + 21A_4\gamma^5 - 120A_5\gamma^6$$

$$c_1 = A_1\gamma - 2A_2\gamma^2 + 6A_3\gamma^3 - 21A_4\gamma^4 - 120A_5\gamma^5$$

$$c_2 = A_2\gamma - 3A_3\gamma^2 + 12A_4\gamma^3 - 60A_5\gamma^4$$

$$c_3 = A_3\gamma - 4A_4\gamma^2 + 20A_5\gamma^3 \quad c_4 = A_4\gamma + 5A_5\gamma^2,$$

$$c_5 = A_5\gamma \text{ ----------(13)}$$

Here A_i for i=0,1----5 are Simultaneous switching noise results is

$$Ai = [(R\ V_{ss}B_nV^n_{dd}.)T_r/(Rv_{ss}\ C_{Vss}+L_{Vss}\ f_1)]a_i + [(L\ V_{ss}B_nV^n_{dd})/(Rv_{ss}\ C_{Vss}+L_{Vss}\ f_1)]\ b_i \text{--} \quad (14)$$

where and are defined in (9). The SSN voltage reaches a maximum when the input voltage completes the transition,

i.e.,$V_{s\ max}$

$$= v_s = c_0(1 - e^{-(Tr-Tn)/\gamma\tau} +$$

$$c_2\xi^2 + c_3\xi^3 + c_4\xi^4 + c_5\xi^5 \text{ ----------(15)}$$

Where, the SSN voltage on a ground rail as predicted by (10), This expression provides a method for evaluating SSN voltage at the system level. The analytically derived waveform characterizing the on-chip SSN voltageents the analytical prediction and the thin line represents the results from SPICE simulations.

D. Packaging Technology

Packaging technology has not kept pace with the development of semi conductor technology. Being an essential part of IC design, the package is fundamentally performing functions of isolation and protection between the device and the environment. Technically besides functions of heat dissipation and die protection, electrical and electromagnetic futures have been much concerned by different requirements in IC evolution.

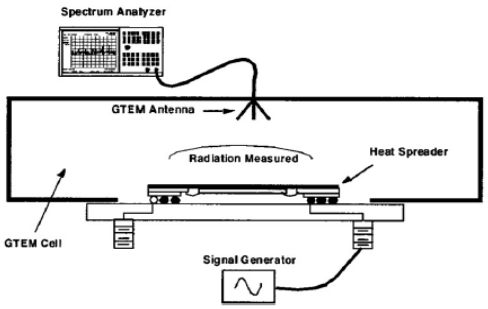

Figure 5- the test setup for measuring shielding effectiveness by GTEM cell [34]

As the package covers the internal die, it is the only media for delivering power and signals, as well as unexpected conducted interference. It is considered a major coupling part of radiated interference to the die when the size of the package is no longer large enough compared to the relative wavelength. For example, when the diagonal length of the package is larger than 25 nanometer, the corresponding radiation frequency that can be generated is around 3-10 GHz. In addition a large size lid is affected by magnetic field problems while the multiplication of metallization layers substrate is affected by electric field problems.

The effective packages design can significantly reduce the radiation emitted from them [31]. In [32], power/ground plane currents and crosstalk in the IC package can be simulated by the finite difference time domain (FDTD) method. The computational simulation [33], measurements cal also be employed to test the package shielding effectiveness with a GHz transverse electromagnetic [GTEM] cell [34]. The measurement setup has been illustrated in above mentioned figure (Figure 3.5) so as to perform suppression, the EMC performance of the package has been presented in [35]. Methods of crosstalk's reduction and radiation suppression are given by [36] on a microprocessor working above GHz. Ground patches are utilized for crosstalk reduction and switching visa is used for radiation suppression. The trend of high integration of analogue and digital circuits in one package, radioactive coupling too influences the mixed signals design in a package [37].

E. Heat sink

The heat sink mounts directly upon an IC chip for heat dissipation. However, when considering the electromagnetic noise coupling from the source (generally, IC) the heat sink can passively result in significant electromagnetic problems depending on the size, shape, material and grounding. Due to the increasing thermal requirement, the size of the heat sink is no longer electrically small compared to the corresponding operating wavelength .the sufficient electrical size will enable the heat sink to act as a potential antenna, which radiates the coupled noise radiation emitted from heat sink [38] using a simplified heat sink model and diole element as the source of electromagnetic noise. The EMC mitigation Another FDTD based method for modelling heat sink RF characteristics can be significant for EMC mitigation [39].

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A number of different standard heatsink geometries also plays significant role in alleviating radiation [40]. Furthermore, from an antenna perspective, radiation performance of a circular heat sink is well studied by using FEM as compared to a monopole [41]. Since a heatsink is a compulsory requirement in high-frequency micro-processers, the ability of the heatsink to radiate electromagnetic energy must be considered. The joint IEEE/EMC society technical committee (TC-9) and Applied Computational Electromagnetic society [ACES] [42] have placed a challenge model [2000-4] on traditional microprocessors with a heat sink for investigation of EMC problems.

With the problems of Heat sink radiation known, solutions to suppress radiation are also in development. Grounding of the Heat sink is one of the most effective ways to achieve this .Deferent grounding schemes have been proposed and implemented by Intel [43] with multiple grounding posts, where it has been found that eight grounding posts around the periphery of the heat sink could be effective in suppressing emission of up to 6 GHz while four grounding posts at four corners only affect up to 1.5 GHz. Some researches have found that the efficacy also depends on impedance of ground connections and distribution [44].

I/Os and PCB

In general, the nano liner dynamic behavior of individual input and output of a digital device is considered in EMC assessment since it directly affects the interconnects where EMI is generated (typically crosstalk, radiation etc.) and hence the research of I/O ports is primarily focused on behavioral modeling and simulation with the use of numerical methods [45] [46]. A common method of creating behavioral models is a simplified equaling circuit of IC ports, where I/O buffer information specification is mostly adopted. In addition, some other approaches are like parametric modeling and input/output system identification methods. A radial bases function (RBF) or piecewise RBF models can be employed as a model of presentations. Though simple, the parametric models approach performs quite accurately.

IV. FUTURE CHALLENGE OF EMC IN VLSI DESIGN

This is the matter of fact that the development in integrated circuits (ICs) is taking place with very vast pace. For instance, the current transistor count in ICs is still doubling every 18 months. On the other hand, microprocessors will entering into 50 Ghz and micro controllers which are supposed to employ 32 nm and 20 nm technique with 3GHz in the despite lagging five years behind technical developments in microprocessors with the constant increase in logic speed and working frequency, smaller elements are becoming more efficient radiators of EM. On the other hand, the technology development is also scaling down to nano scale technologies which are being employed with sub/deep nano scale technology.

The semiconductor technology is constantly developing which allows more ICs to be fabricated simultaneously. However it still requires U-H cost equipment to deal with wafer in atomic scale precision. That makes EMC prediction and its accuracy in design phase both critical and valuable. The systems are becoming more and more complex such a SOC and SIP system on chip and system in package. Thus, the level of emissions study would therefore move into a new frequency band and therefore the susceptibility in the new frequency band should be studied and the level of interferences should be assessed. To satisfy the requirement for the development of IC, a super high frequency measurement technology is inevitable. As the complexity of IC has been increasing swiftly, the correspondent parasitic effect is the jeopardizing the performance of IC EMC lower supply voltage also decreases the associated noise margins and increases the sensitivity to interference, in relation to IC emission levels and immunity levels. It is evident that IC performance without EMC optimization will not satisfy user needs and performance optimization. In the IC design industry a long design circuit and high fabrication costs are critical factors which are closely related to the market value of products. On the other hand, a manufacturer might have to face expensive re-design cost or product failure, in case a potential EMC problem is detected after chip fabrication. These all factors motivate researchers, industries and academicians to develop a robust and optimal approach for EMI/EMC assessment of the chips to ensure minimal discharge and irregularities in function.

V. CONCLUSION

This paper discussed and elaborates varied aspects of electromagnetic compatibility and allied electromagnetic interference factors in VLSI design process and chip design. The key factors such as integrated circuits and its development, significance of ICs and various problems associated with ICs such as, EMC and EMI have been discussed in this paper. The discussions in this paper suggested to developing a novel approach for EMC assessment of the IC devices and reduction in noise to ensure optimal functionality of the ICs in real time applications at higher frequency range. high frequency aspects in vlsi may consider in different parameters such as power dissipation during the activity of chip ,crosstalk due to ground bounce, delay due to rise time , inductance effects and scaling down of chip etc.

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