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Design of a Power Efficient Parallel Architecture for Linear Feedback Shift Registers

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Abstract: This brief presents a new parallel architecture for linear feedback shift registers. This is 8-bit parallel architecture, which can be used to achieve high-throughput. In linear feedback shift registers exclusive-or is commonly used as linear function. Linear feedback shift register is determined by the feedback polynomial. Cyclic Redundancy Check (CRC) & Bose - Chaudhuri –Hocquenghem (BCH) are encoders for storage and communication systems. CRC is a system that reduces complexity of its feedback loop. When compared to previous parallel architectures based on the transposed serial LFSR. In this the LFSR based upon the IIR topology. The previous 4-bit parallel architecture has more complexity; it occupies more area, time. The proposed 8-bit parallel architecture better achieves area-time product &reduces complexity.

Keywords: Bose–Chaudhuri–Hocquenghem (BCH) encoder, cyclic redundancy check (CRC) encoder, linear feedback shift register (LFSR), parallel architecture.

1. INTRODUCTION

LFSR is a shift register. An n-bit shift register pseudo-randomly scrolls between 2^n-1 values, but does it very quickly because there is minimal combinational logic involved. Once it reaches its final state, it will transverse the sequence exactly as before. LFSR produces equal number of 1s and 0s. LFSR implemented in different applications, using a parallel architecture.

Normal LFSR produces output of several clock cycles of a serial LFSR, due to this frequency reduces. It allows reduction in the power supply voltage. In LFSR n-bit counters exhibiting pseudo-random behavior, built from simple shift-registers with small number of XOR gates.

Cyclic redundancy check (CRC) is an error detecting code, commonly used in digital networks and storage device to detect accidental changes: it is based on the remainder of a polynomial division. To implement in binary hardware, code is easy to analyze mathematically.

Bose-Chaudhuri-Hocquenghem &Cyclic Redundancy Check (CRC) are implemented by a polynomial i.e., generator polynomial and remainder polynomial [1] and [2]. When high speed data is required in sequential LFSR circuit it cannot meet the speed requirement. Sometimes LFSRs used in built -in self-test (BIST) and design for test (DFT). Generally LFSR lead to an increase in the critical path. When critical path increases the speed of the circuit decreases [2]. The IIR topology for parallel architecture is based on both feed forward paths and feedback

LFSR parallel architecture can also face issues like fan out due to the number of non-zero coefficients especially in generator polynomial [3]. In linear feedback shift registers (LFSR) based on conventional architecture. In CRC the output signal is connected to a number of nodes, it is going to be linked to the nonzero coefficients to the generator polynomial [4]. It is suffering from the large fan out effects.

In LFSR when we unfold directly, Pipelining is not possible. There are no feed-forward cut sets. In communication systems and storage systems it is going to be widely used in forward error correction [4]. By using this forward error correction is to recover code words corrupted by noisy channels.

Multimode encoding architecture for lengthy Bose – Chaudhuri-Hocquenghem (BCH) codes has the more area efficiency [4]. Bose –Chaudhuri-Hocquenghem (BCH) eliminates completely the preprocessing and post processing multimode encoder’s. Generally normal linear feedback shift registers having a loop. The loop can be simplified by applying a linear transformation [5].

The parallel processing while increases the number of bits that can be processed in one clock cycle. It can also lead to a long critical path, thus it will decrease the speed of the circuit and increase the high through put rate, and this is achieved by parallel processing [5]. Another issue is occurred i.e., increase of hardware cost caused by parallel processing.

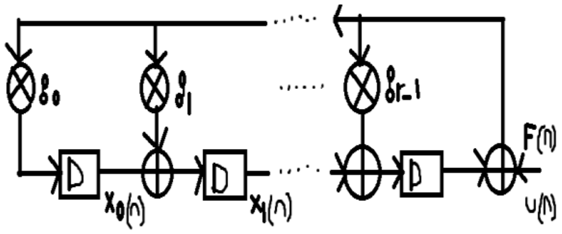

Fig.1: Serial LFSR Architecture.

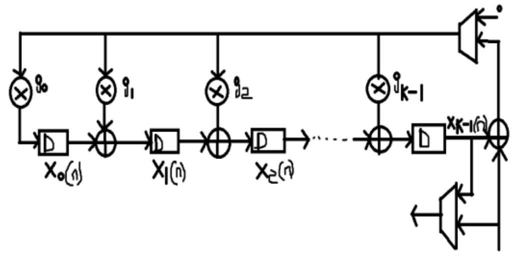

Fig.2: Basic LFSR Architecture.

Here in this above fig.1 the inputs are u(n) and the outputs are y(n) and then the feedback loop values is f(n).

The LFSR output is divided into two parts. If one part is depending an input and another part is depending an output [5]. By the transformed loop structure, it has no feedback loop in the dependent part of an input, and the pipelining part technique it can be adopted in between the output dependent part and the input dependent part [6].

In fig.1: Shows the f(n) values it is calculated as the input feedback values, end the p is represented as the parallel system. Then the x (mp) represented as the explicit input of y. By this way the complexity has been moved out of the feedback loop [6]. This type of structures is applicable to any linear feedback shift registers (LFSR).

The rest of this is organized as follows. Section2 summarizes the basic LFSR architecture with the polynomial equation and section 3 describes the parallel LFSR architecture based on the IIR topology and section4 describes the proposed architecture in detail. Simulation results & Experimental results are explained in section 5 & section 6 and conclusion are made in 7.

2. LFSR ARCHITECTURE

A general basic LFSR architecture for k^th order generating polynomial. Here the K denotes the length of the LFSR. Then the g0, g1, g2……gK is the number of delay elements it represents the characteristic polynomial of the coefficients. Then the characteristic polynomial equation is shown below.

$$g(x)=g_0+g_1x+g_2x^2+.....+g_Kx^k \text{ ....(1)}$$

Where $g_k=g_0=1$ for BCH and CRC generator polynomials. By using two input XOR gate is the sum of two elements are either short circuits or open circuits i.e., $g_i=1$. No connection exists on the other hand $g_i=0$ then the corresponding XOR gate can be replaced by a direct connection from input to output [7]. By modifying the system we can increase the throughput to process some number of bits in parallel. By reducing the complexity is proposed a state space transformation [8].

The basic of high speed parallel CRC implementation is to insert a number of delay elements [8]. The feedback loop is useful for eliminating large fanout. Here the feedback loop is to reduce the iteration bound [9].

The conventional parallel architecture is to reduce the critical path delay. In generally the LFSR parallel architecture based on the equation (1).

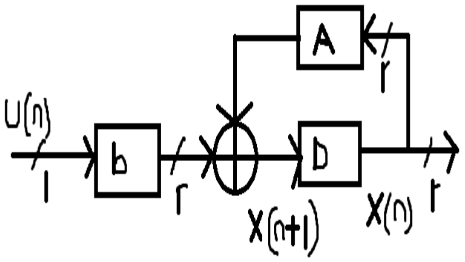

Fig.3: Serial LFSR Architecture.

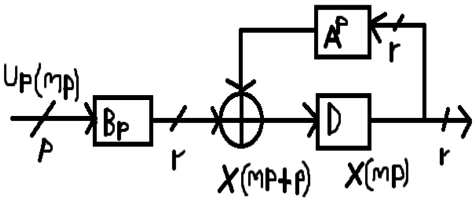

Fig.4: P-Parallel LFSR Architecture.

The basic LFSR architecture the critical path is proportional to $\log_2 k$, here k is the length of the BCH code and then the second step is proposed to realize the CRC computation in hardware [10]. In generator polynomials CRC and BCH encoders are based on division and multiplication. To speed up the LFSR but their hardware cost is high.

3. LFSR ARCHITECTURE BASED ON IIR FILTER TOPOLOGY

Here we can derive parallel architecture for linear feedback shift registers with IIR topology.

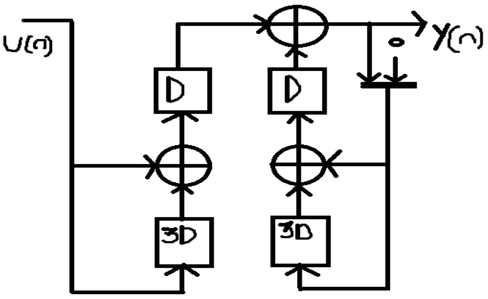

Fig.5:4-Bit Parallel LFSR Architecture Based On IIR Filter Topology for $g(x) =1+x^3+x^4$.

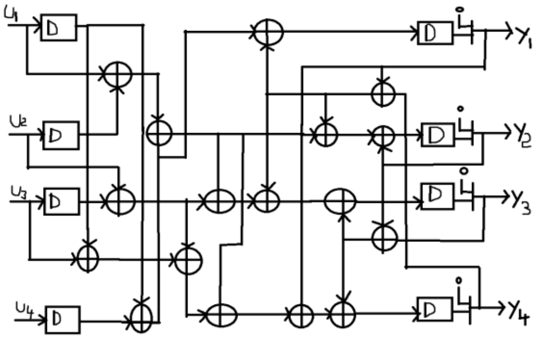

Fig.6: Conventional 4-Bit Parallel LFSR Architecture for $g(x) =1+x^3+x^4$.

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The basic LFSR architecture the critical path is proportional to $\log_2 k$, here k is the length of the BCH code and then the second step is proposed to realize the CRC computation in hardware [11]. In generator polynomials CRC and BCH encoders are based on division and multiplication. To speed up the LFSR but their hardware cost is high.

A new 4-bit parallel architecture based on the unaccustomed serial LFSR is to reduce both critical path delay and hardware complexity [12]. The conventional serial LFSR are used to store incomplete outputs instead of the feedback values. The 4-bit parallel architecture generates the outputs by using the past inputs and outputs stored [13].

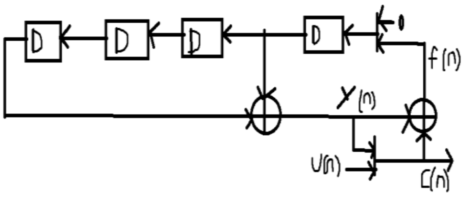

Fig.7: Transposed Serial Encoder For g(x).

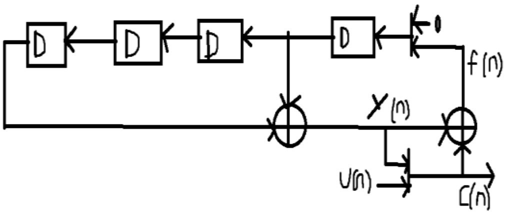

Fig.8:4-bit Encoder For g(x) = $1+x^3+x^4$.

Let p be the parallel factor, N be the code length.tne 4-bit parallel architecture takes N/p cycles in the case [14]. The below architecture, the past inputs are eliminated from the registers holding, and the calculations are depending on the inputs are distributed to two small combinational logics.

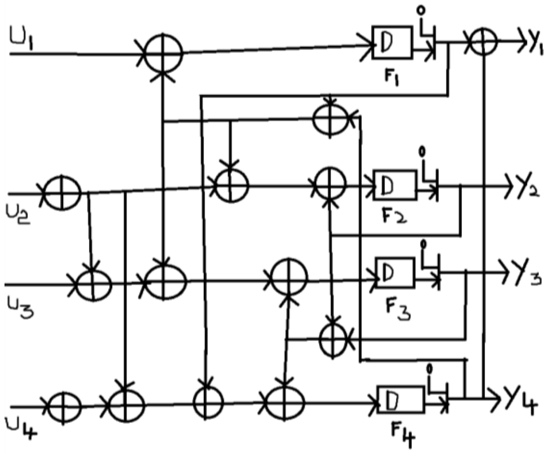

Fig.9: 4-Bit Parallel Architecture For g(x) $=1+x^3+x^4$.

The above 4-Bit Parallel Architecture has no feedback loop associated with the input values. Here we are applying the tree-structured computation in the circuit can be optimized. The input and feedback dependent part to connect an additional gate is added.

4. PROPOSED ARCHITECTURE

The proposed architecture is 8-bit parallel architecture. When compared to previous parallel architecture the circuit performance is good. It reduces the hardware cost when compared to the previous and also reduced the critical path by eliminating the calculation input.

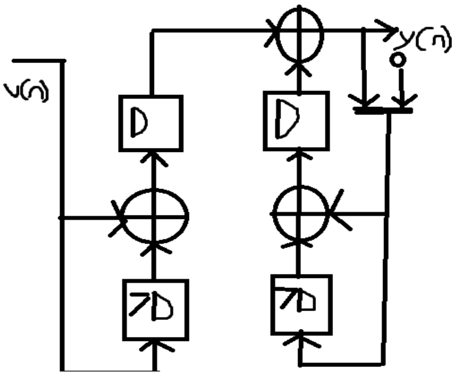

Fig.10: 8-Bit Parallel LFSR Architecture Based On IIR Filter Topology for g(x) $=1+x+x^7+x^8$

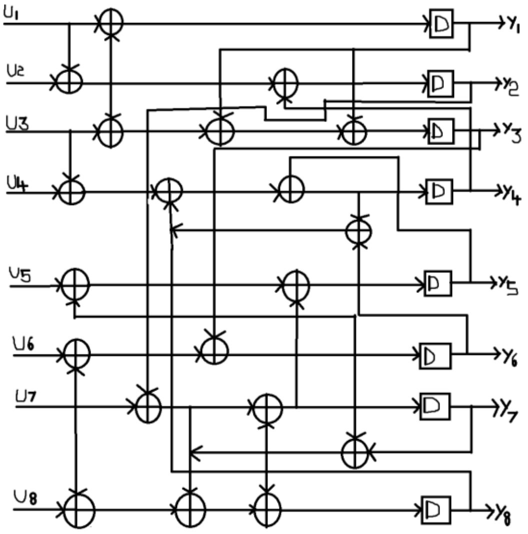

Fig.11: 8-Bit Parallel Architecture For g(x) $=1+x+x^7+x^8$.

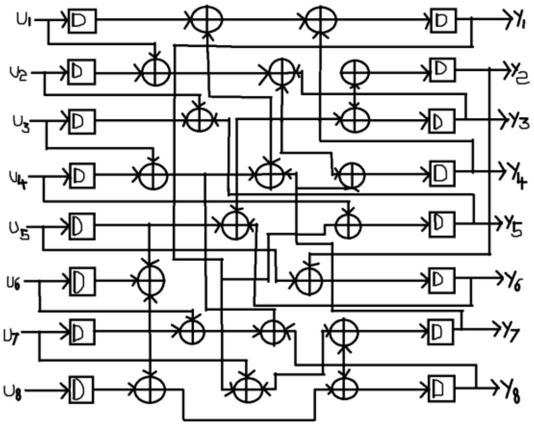

Fig.12: Conventional 8-Bit Parallel Architecture For g(x) $=1+x+x^7+x^8$.

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5. SIMULATION RESULTS

1) CMOS implementation of Conventional 4-bit parallel LFSR architecture:

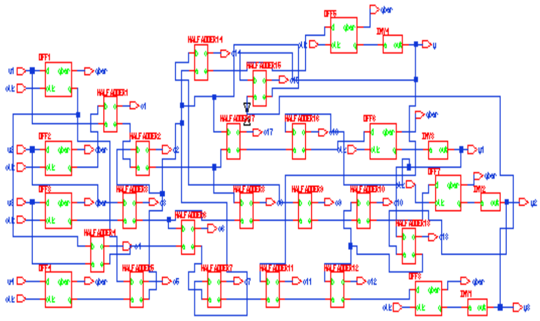

Fig.13: CMOS Implementation Of Conventional 4-Bit Parallel LFSR Architecture.

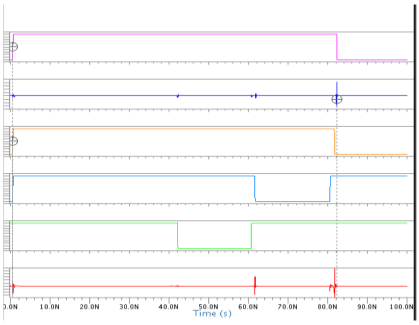

Fig: 14: Simulation waveform for CMOS Implementation Of Conventional 4-Bit Parallel LFSR Architecture.

In the above simulation results as shown CMOS implementation of conventional 4- bit LFSR architecture, simulation waveform.In this input side and output side are using D-flipflop and also the number of adder are used in the circuit. By using this type of conventional LFSR, speed of the circuit is decreased and also it occupies large area.when the number of components increases the speed of the circuit automatically desreases. Here the complexity of the circuit in high.

2) CMOS Implementation Of 4-Bit Parallel LFSR Architecture $G(X) = 1+X^3+X^4$:

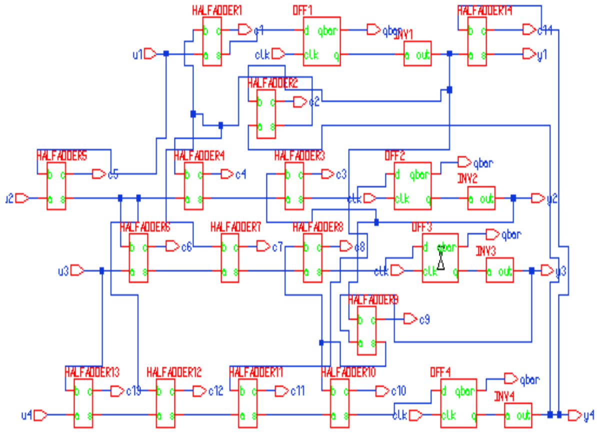

Fig.15: CMOS Implementation Of 4-Bit Parallel LFSR Architecture $g(x) = 1+x^3+x^4$.

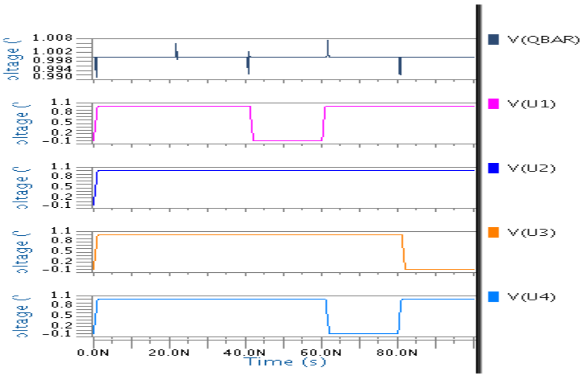

Fig.16: Simulation waveform for CMOS Implementation Of 4-Bit Parallel LFSR Architecture $g(x) = 1+x^3+x^4$.

In the above simulation results as shown CMOS implementation of a 4-bit parallel LFSR architecture $g(x) =1+x^3+x^4$, Simulation waveform. In this architecture it stores only the feedback value.It generates outputs by using the stored feedback values. It stores both the past inputs and past outputs,it achieving the high speed compared the conventional 4-bit parallel architecture.It has a block for CRC & BCH encoders with low complexity.

3) CMOS Implementation Of 8-Bit Parallel LFSR Architecture $G(X) = 1+X+X^7+X^8$:

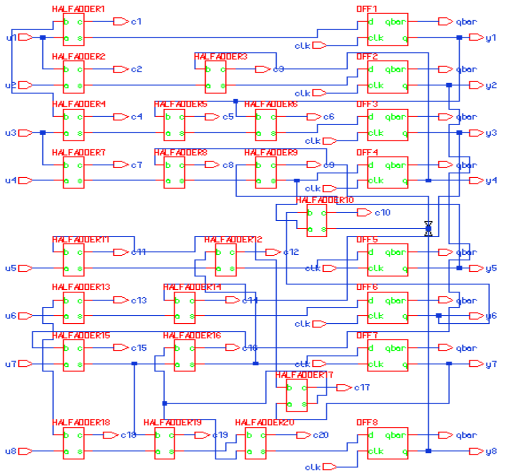

Fig.17: CMOS Implementation Of 8-Bit Parallel LFSR Architecture $g(x) = 1+x+x^7+x^8$.

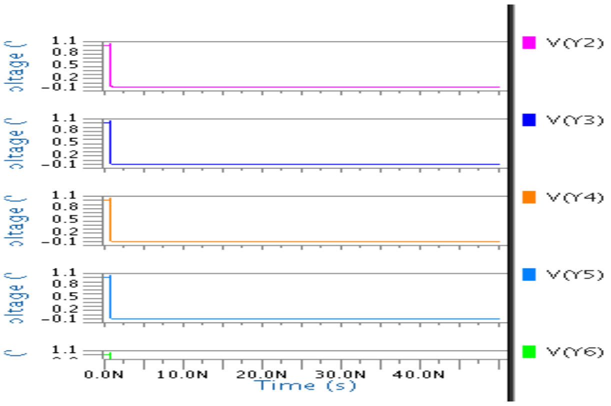

Fig.18: Simulation waveform for CMOS Implementation Of 8-Bit Parallel LFSR Architecture $g(x) = 1+x+x^7+x^8$.

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In the above simulation results as shown CMOS implementation of a 8-bit parallel LFSR architecture g(x) $=1+x+x^7+x^8$, Simulation waveform. It reduces critical path increasing the hardware cost at the same time, and also speed of the circuit performance increases is based on parallel IIR filter design.

4) CMOS implementation of Conventional 8-bit parallel LFSR architecture:

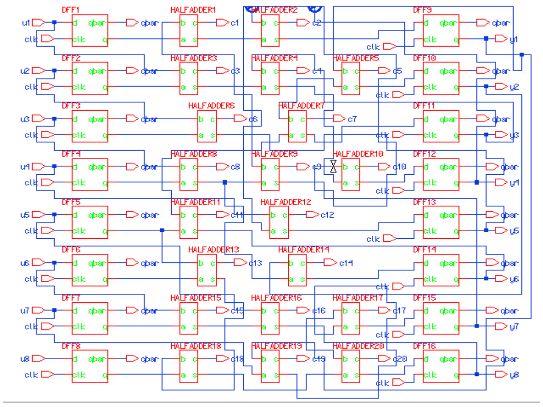

Fig.19: CMOS Implementation Of Conventional8-Bit Parallel LFSR Architecture.

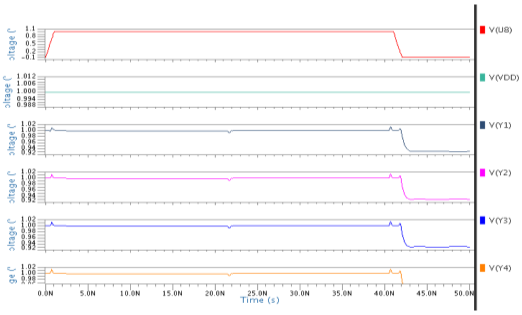

Fig.20: Simulation waveform for CMOS Implementation Of Conventional 8-Bit Parallel LFSR Architecture.

In the above simulation results as shown CMOS implementation of conventional 8- bit LFSR architecture, simulation waveform.In this input side and output side are using D-flipflop and also the number of adder are used in the circuit. When compared to conventional 4- bit LFSR architecture with conventional 8- bit LFSR architecture, in 8-bit power dissipation reduces, and also number of adders are reduced.

6. EXPERIMENTAL RESULTS

Comparison table of Parallel LFSR Architecture:

Si.No	Parameters	Conventional 4-bit LFSR architecture	4-bit LFSR architecture	8-bit LFSR architecture	Conventional 8-bit LFSR architecture
1	Power Dissipation	5.7476mw	4.8619mw	6.9959mw	7.3311mw
2	Delay	81.758Ns	20.704Ns	20.785Ns	20.614Ns
3	Slew Rate	432.89mEG	4.0921mEG	6.0022mEG	95.120mEG

7. CONCLUSION

This brief has presented new parallel linear feedback shift register architecture. In the proposed 8-Bit Parallel LFSR Architecture which without increasing the hardware cost at the same time, and also speed of the circuit performance increases is based on parallel IIR filter design. The proposed Parallel LFSR Architecture Can reduces the critical path. As a result the proposed parallel linear feedback shift register architecture is effective in achieving a high speed for parallel Cyclic Redundancy Check (CRC) & Bose Chaudhuri Hocquenghem (BCH). This type of design is applicable to any type of LFSR architecture. Further work will be directed towards reducing complexity, critical path in the feedback part of the design using IIR filtering. The performance of long CRC & BCH codes will be evaluated in the future work.

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