IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 7, July 2016

Design and Simulation of 4T-Cascode Amplifier at 45 Nanometer Technology Node

Arshad Jamal[1], Dr O.P.Malik[2]

M. Tech, Student, AFU, Faridabad, India[1]

Professor, AFU, Faridabad, India[2]

Abstract: In this research paper, design and simulation of of 4T-Cascode Amplifier at 45 Nanometer Technology Node has been performed using 45nm technology. DC voltage gain, average power, bandwidth and output resistance have been computed using HSPICE Software. Further, the low voltage Cascode Op Amp has better DC Gain, output resistance and less power dissipation. Thus the simulation studies have revealed that the performance of the low voltage folded cascode Op Amp can be improved optimized at different voltage. DC voltage gain is 35.6 dB, average power is 7.81 uW, bandwidth is 4.08 MHz, Phase Margin 88.3^0 and Output Resistance 25.16 K-Ohms have been computed using HSPICE Software at 0.9V. DC voltage gain is 13.7 dB, average power is 0.23uW, bandwidth is 110.7 MHz, Phase Margin 95.30 and Output Resistance 9.5 K-Ohms have been computed using HSPICE Software at 1.5V.

Keywords: 4T-Cascode amplifier, DC Gain, Output Resistance, Band width, Average Power.

I. INTRODUCTION

The cascode topology has the advantage of higher gain performance at lower frequency. As the operation frequency increases, cascode transistors have a larger parasitic capacitance which reduces the inter-stage impedance and gain. Cascode topology and the gain-boost cascode topology in millimeter-wave ranges, three topologies as shown in Fig. 1 are fabricated using 65-nm CMOS technology. The transistor M1 in the three topologies is the same one, which uses the asymmetric-layout technique in. The transistor M2 uses the common layout provided by foundry [1]. One drawback of the cascode configuration, however, is the reduced voltage swing at the output compared to the simple common-source amplifier with current source load. Advantages of the cascode amplifier configuration include high gain (due to high output resistance) and improved bandwidth due to reduced Miller Capacitance associated with the input time constant. Invented in 1979 and subsequently refined in 1990, the CMOS active-cascode gain-enhancement technique1 finds wide applications in analog integrated circuits, such as Nyquist-rate and oversampling data converters, sample-and-hold amplifiers, switched-capacitor filters, band-gap reference circuits, and voltage regulators. By boosting the low-frequency transconductance of the cascode device, the technique increases the output resistance of CMOS cascode operational amplifier (op amp), and hence the voltage gain without degrading its high-frequency performance. As a result, it is ideally suitable for on-chip applications, where a large gain-bandwidth product is desirable while driving capacitive loads. In addition, as the technique derives extra gain laterally using an auxiliary amplifier (booster) without stacking multiple cascode transistors, it retains the high-swing feature simple cascode stage, and thus, becomes widely popular in scaled CMOS technologies with low supply voltages [2-5]. This has an advantage in the attainable bandwidth amplifier when driving a capacitive load, which itself acts as compensation capacitor [6-10].

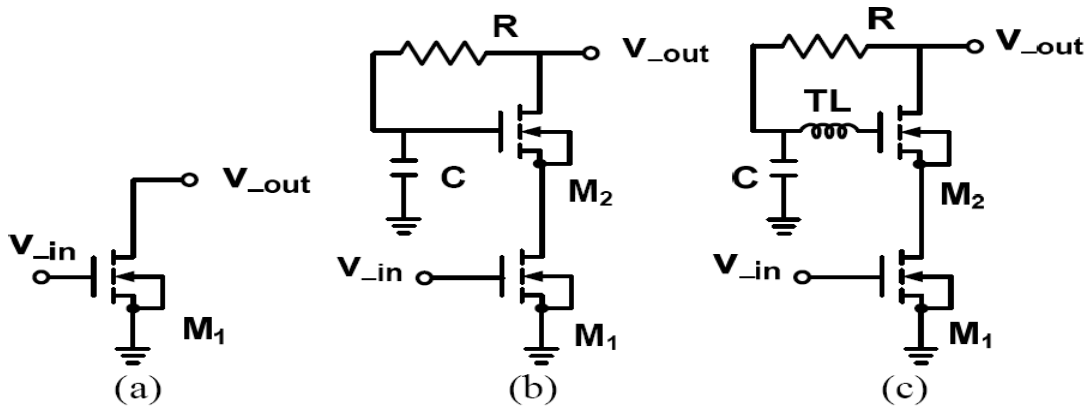

Fig 1 (a) Common Source Topology (b) Cascode topology (c) Gain boosting cascode topology

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 7, July 2016

This paper begins with an overview of Cascode Amplifier in section 2, Simulations of proposed 4T-Cascode Amplifier in section 3, & Section 4 gives result and conclusion.

II. PROPOSED 4T- CASCODE AMPLIFIER

Common Source amplifier with current source load is implemented using the short-channel CMOS Technology of 45nm. The gain of the general Amplifier is low. To boost the gain of the single-stage amplifier and to eliminate, or more correctly to reduce, the Miller effect, consider the cascode amplifier seen in Fig 2.

The gain of the cascode amplifier is the resistance in the drain divided by the resistance in the source of the amplifying device (Ml).Input ac signal is applied at the gate of M1 to amplify.

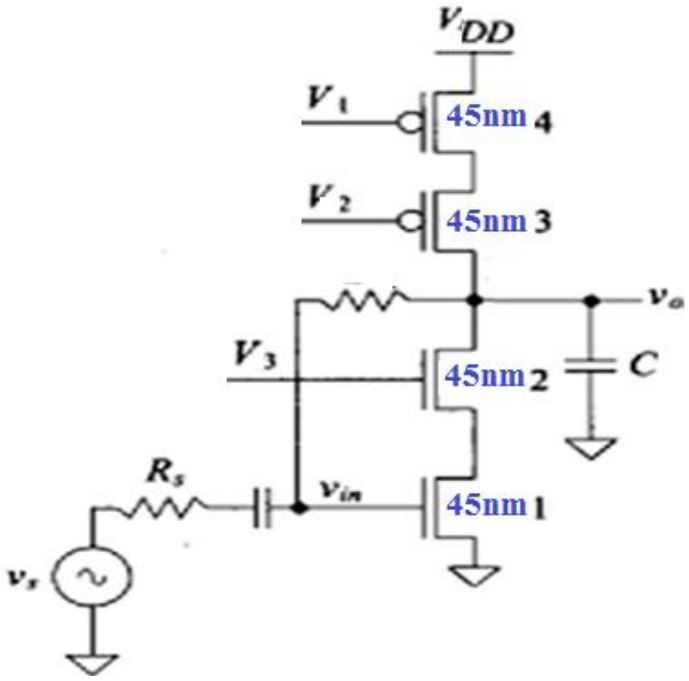

Fig 2: Conventional CMOS Cascode amplifier

III. SIMULATIONS OF PROPOSED 4T-CASCODE AMPLIFIER

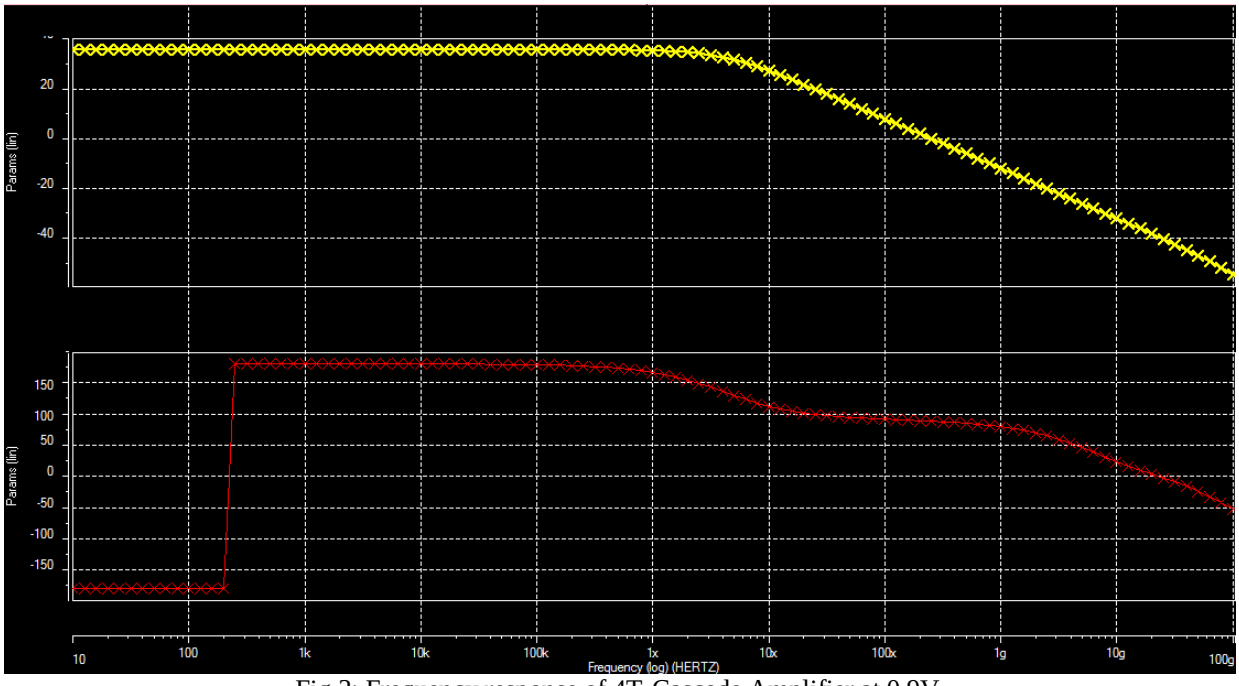

Fig 3: Frequency response of 4T-Cascode Amplifier at 0.9V

DOI 10.17148/IJARCCE.2016.5716

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 7, July 2016

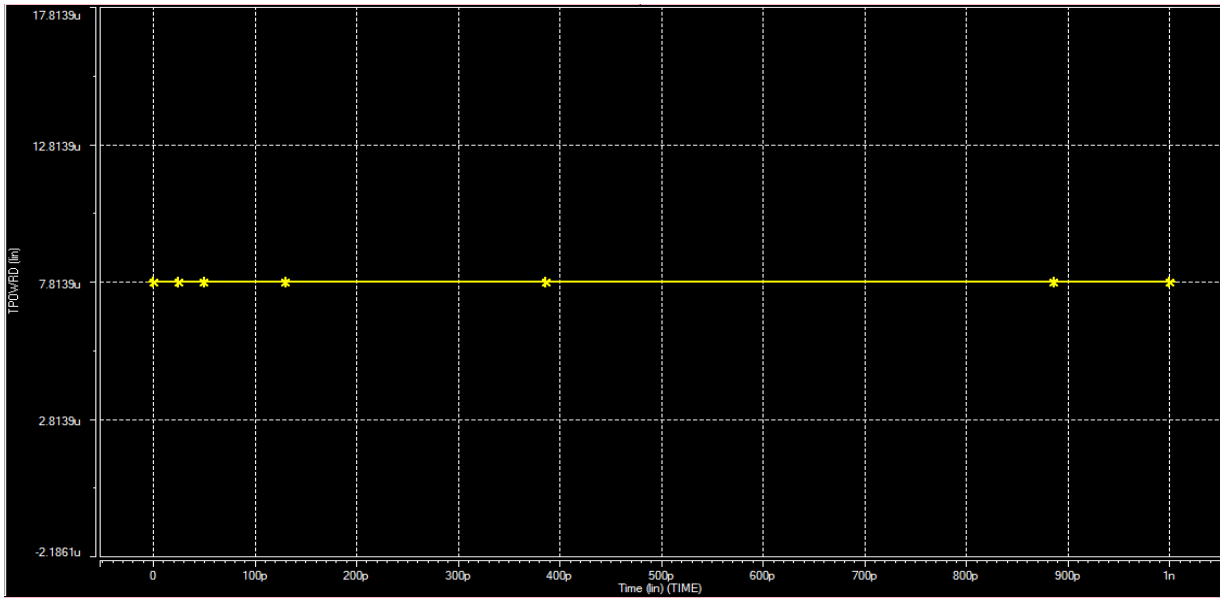

Fig 4 : Average Power of 4T-Cascode Amplifier at 0.9V

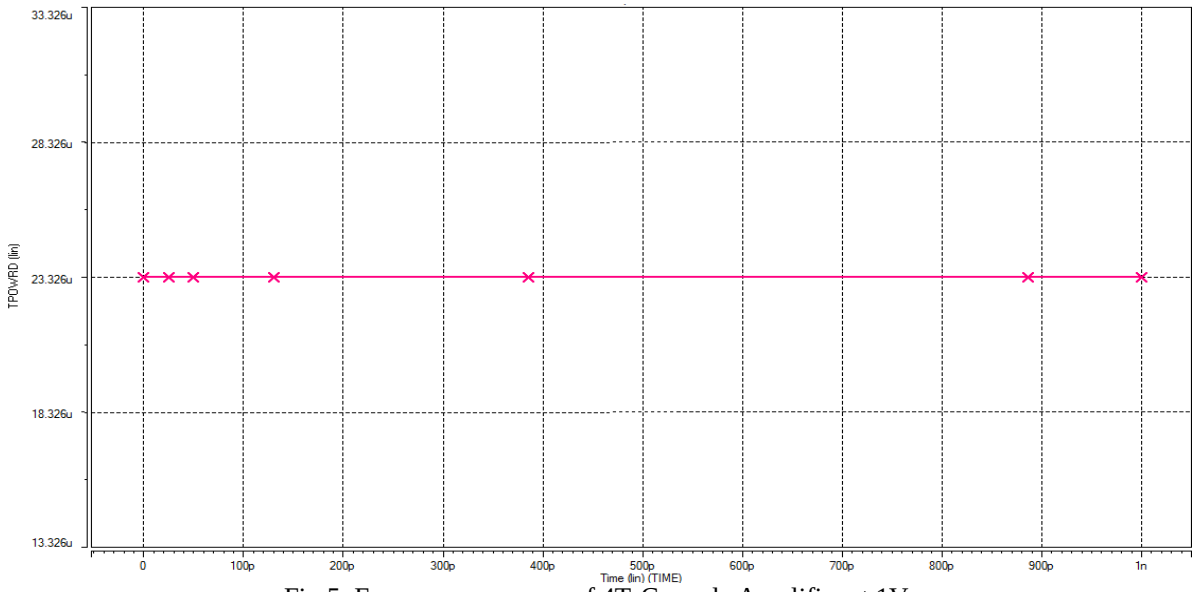

Fig 5: Frequency response of 4T-Cascode Amplifier at 1V

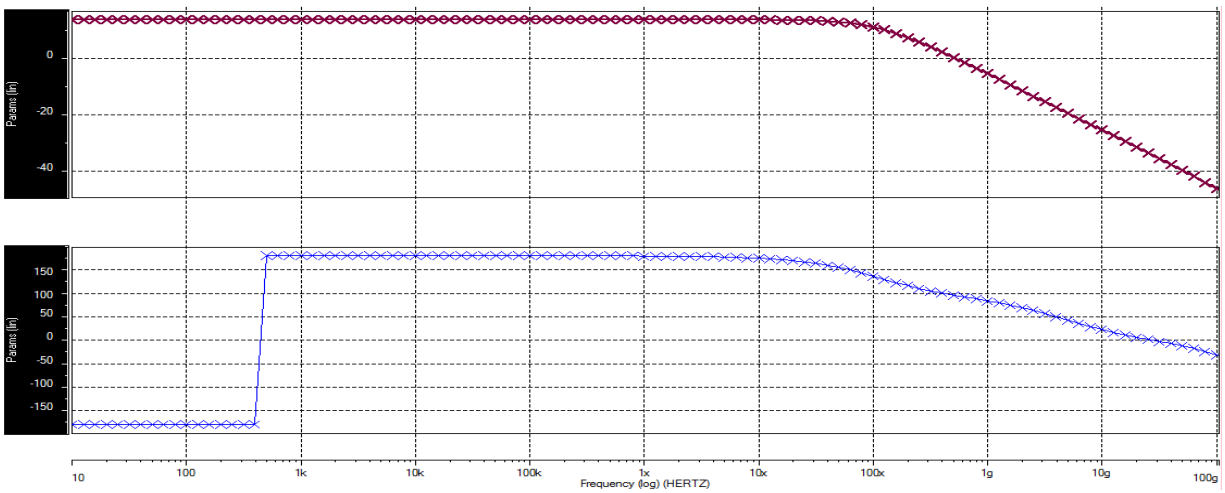

Fig 6: Average Power of 4T-Cascode Amplifier at 1V

DOI 10.17148/IJARCCE.2016.5716

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 7, July 2016

IV. RESULT AND CONCLUSION

This paper has successfully designed and simulated 4T- cascode amplifier based on at 45nm. DC voltage gain is 35.6 dB, average power is 7.81 uW, bandwidth is 4.08 MHz , Phase Margin 88.30 and Output Resistance 25.16 K-Ohms have been computed using HSPICE Software at 0.9V. DC voltage gain is 13.7 dB, average power is 0.23uW, bandwidth is 110.7 MHz, Phase Margin 95.30 and Output Resistance 9.5 K-Ohms have been computed using HSPICE Software at 1.5V. The overall design and indicates that the four transistor based cascode amplifier has excellent performance in terms of DC gain, output resistance, Band width and average power.

Table 1: Comparative analysis of Simulation of 4T-Cascode Amplifier at 45 Nanometer Technology Node at different V_{DD}

S. No.	Parameters	4T-Cascode Amplifier at 1 V	4T-Cascode Amplifier at 1.2V
1	DC Gain	35.6dB	13.7 dB
2	Bandwidth	4.08MHz	110.5 MHz
3	Output Resistance	25.16 K-Ohms	9.5K-Ohms
4	Average Power	7.81uW	0.23uW
5	Phase Margin	88.3^0	95.3^0

Table 2: Parameters used in the proposed 4T-Cascode Amplifier

S. No.	Parameters	Value
1	Channel Length	45nm
2	Channel Width	763nm
3	Supply Voltages	0.5V and 1.5V
4	nMOS Transistors	2
5	pMOS Transistors	2
6	Technology File	PTM45v203

REFERENCES

1. Qinghong Bu, Ning Li, Kenichi Okada and Akira Matsuzawa A Comparison between Common-source and Cascode Topologies for 60GHz Amplifier Design in 65nm CMOS Department of Physical Electronics, Tokyo Institute of Technolog, Tokyo, 152-8552, Japan.
2. B. J. Hosticka, "Improvement of the gain of MOS amplifiers," IEEE Journal of Solid-State Circuits, vol. 14, pp. 1111-1114, Jun. 1979.
3. K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," IEEE Journal of Solid-State Circuits, vol. 25, pp. 1379-1384, Dec. 1990.
4. E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," IEEE Journal of Solid-State Circuits, vol. 25, pp. 289-298, Feb. 1990.
5. H. C. Yang and D. J. Allstot, "An active-feedback cascode current source," IEEE Transactions on Circuits and Systems, vol. 37, pp. 644-646, May 1990.
6. P. R. Gray and R. G. Meyer, "MOS operational amplifier design-a tutorial overview," IEEE Journal of Solid-State Circuits, vol. 17, pp. 969-982, Dec. 1982.
7. A. A. Abidi, "On the operation of cascode gain stages," IEEE Journal of Solid-State Circuits, vol. 23, pp. 1434-1437, Dec. 1988.
8. Behnam Ghavami, Mohsen Raji, Hossein Pedram, and Massoud Pedram," Statistical Functional Yield Estimation and Enhancement of CNFET-Based VLSI Circuits", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 21, No. 5, May 2013.
9. Bipul C Paultt, Shinobu Fujitat, Masaki Okajimat, and Thomas Leet," Modeling and Analysis of Circuit Performance of Ballistic CNFET", DAC 2006, July 24-28, 2006, San Francisco, California, USA.
10. J. Deng, H.S.P.Wong, Modeling and analysis of planar gate capacitance for 1-d FET with multiple cylindrical conducting channels, IEEE Transactions Electron Devices 54(2007)2377–2385.