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Comparison Study of Induction Motor Drives using Microcontroller and FPGA

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Abstract: Variable speed induction motors are one of the most researched topics in the industry today. As the digital control of the motors took over the analog control, the search for an efficient speed control scheme for ac induction motors has started. Along with the speed control mechanism the selection of the controller is also of utmost importance. As there are different controllers available like microcontroller, FPGA, dsp, Choosing the most efficient controller for the given application is crucial. This project is a comparison study of speed control of induction motor using a microcontroller and FPGA. The induction motor is driven using both FPGA and microcontroller and the results are studied. The system is tested and experimental results are recorded for various speed for both controllers.

Keywords: Induction Motor; Microcontroller; Pulse Width Modulation Inverter; Speed Control; FPGA.

I. INTRODUCTION

Induction motors are widely used in any section of the society including domestic section, industrial areas, educational areas and many more human areas. Induction motors are robust, cheap, efficient, reliable and simple in construction. They have low maintenance cost and high starting torque. Speed control means intentional change in drive speed to a value required to perform a specific work. Controlling the speed of induction motor can be classified into two type scalar control and vector control. Scalar control involves controlling the magnitude of voltage or frequency of the motor.

To keep the torque of the motor close to the rated torque at any frequency the average stator flux must be constant. If the supply frequency is decreased without changing the supply stator voltage, the air gap flux increases which increases the magnetizing current, distorts the line current and voltage, increase the core and copper loss and the system become noisy. Air gap voltage is given by

$E_{avg}=K.\ \phi_{avg}.f$

Where E_{avg} is the air gap voltage, f is the operating frequency and ϕ_{avg} is the average flux. The input voltage is directly proportional to the product of supply frequency(f) and average flux (ϕ_{avg}).Input supply voltage

$V_s \approx k.\ \phi_{avg}.f$

and, $\phi_{avg} \approx v/f$

Thus by varying both voltage and freequency at the same time to keep t their ratio as constant stator magnetic field and hence torque can be kept constant.Hence v/f method is considered for this project.

The popularity of variable speed induction motor powered by switching power converters are increasing , because it is easy to control power converters.PWM signal is used to control power converter to deliver energy to motor.Microcontroller ,microprocessor ,DSP and FPGA can be used to facilitate the digital implementation of the control system.FPGA can generate required PWM more easily and economically because of its flexibility, parallalism and also FPGA operate faster than microprocessor.On the other hand microcontrollers have powerful computational abilities and inbuilt modules which makes them the widely used control equipment in induction motor drives. In this paper a comparison study of induction motr drive systems using a FPGA and microcontroller is presented. The aim of this study is to findout which control system is more efficient in driving the induction motor.

II. PROPOSED SYSTEM

The Proposed systems block diagram is shown in figure 1. A three phase pwm inverter is used to drive the motor. The inverter changes the dc input voltage to ac output voltage of desired frequency and voltage to drive induction motor. The control signals required for this dc to ac conversion is provided by FPGA/Microcontroller. The gate driver circuit provide isolation between high voltage power circuit and control circuit.

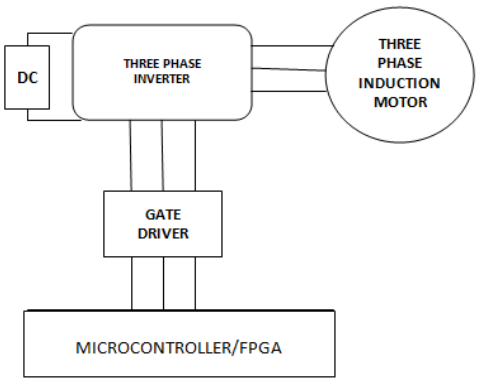

Fig. 1 Block diagram of the proposed system

Fig 3.2 shows the 3 phase inverter circuit .it consists of six switches which are controlled by six PWM signals

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generated by FPGA/Microcontroller. This PWM signals vary the gain of the inverter and hence the output voltage. The gating signals for these switches are generated by comparing a sinusoidal signal with a triangular reference signal. The frequency of the sine wave determines the frequency of the inverter output and its amplitude control the amplitude of the output voltage.

Frequency of the PWM signal will be same as that of frequency of the triangular wave. Three of these six PWM signals are generated by comparing equally shifted (120^0) reference signal with triangular signal and the rest are obtained by inverting these three signals.

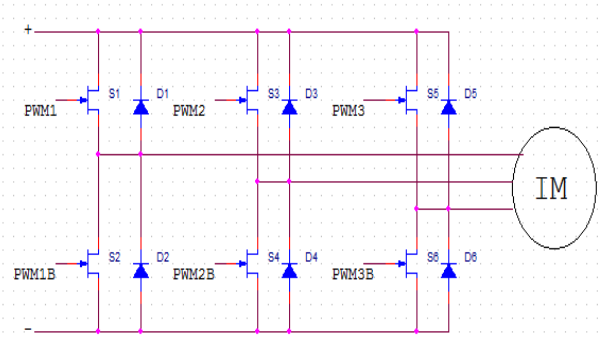

Fig 2 Three phase inverter

When a switch is turned on current flows into the induction motor and this energy is stored in it due to its inductive property. This stored energy is discharged through the diode connected across the switch when switch is turned off. In normal operation two IGBT switches in one phase leg will turned on one after another. If both switches are turned on at the same time it will result in rise of current between power supply rails which is limited by only dc link inductance. This bridge shoot through results additional losses it also cause thermal runway which result in failure of IGBT and inverter. PWM signal is given to upper switch and its inverted signal is given to the lower switch of the same limb. Hence there is no chance for turning on two switches at the same time .But since IGBT switches are not ideal their turn on and off time are different. Hence it is recommended to add dead time in to control scheme. Which ensures that one switch is turned off first only after dead time the second turns on .hence bridge shoot through can be eliminated.

III.FIRMWARE IMPLEMENTATION

A. Using Microcontroller

We use the LPC1769 ARM as the microcontroller to implement the firmware. The LPC1769 is a Cortex-M3 microcontroller for embedded applications featuring a high level of integration and low power consumption .Being a powerful microcontroller LPC1769 has inbuilt modules to create the pwm waves. Even though the basic pwm module is available because of its versatility and efficiency we use the Motor Control Pwm module of the microcontroller. The pwm waves required for all the three phases and their inverted forms are made using this module. The microcontroller is programmed in such a way that it can control the speed by varying the frequency of output waveform while keeping the V/f ratio constant.

The Motor control pwm module is a powerful module present in LPC1769 which is dedicated to AC and DC motor control applications. The module contains inbuilt registers for varying the pwm duty cycle, time period and also to insert dead time. The module also provides different interrupts.

The module is initialized and set up to create interrupts on every match with the sine table value. The user program is written in the ISR to avoid timing issues. Writing the program in the ISR will ensure that all the sample values are passed to the MCPWM register in exact same time intervals. Three sine modulated pwm waves, each 120^0 phase shifted from each other are created using the module. The MCPWM module will automatically create the inverted versions of the waves which is necessary for driving the inverter. The created waves are shifted and positioned in such a way that over modulation is completely avoided in the pwm outputs. The user commands are taken through two buttons corresponding to increasing and decreasing the speed. According to the command the amplitude and frequency of the pwm waves are varied keeping the V/f ratio constant. The microcontroller is set up to change the frequency of output wave from 10 Hz to 50Hz

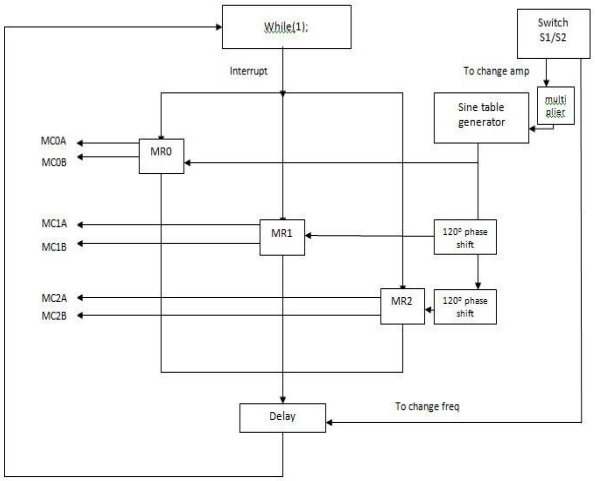

Fig 3 Firmware implementation using microcontroller

B. Using FPGA

The firmware code in FPGA is developed on spartan3 development board of frequency 30MHz. Programming is done using Verilog code ,to write the code Xilinx ISE design suit is used.PWM signal is generated by comparing sine and triangular wave .Triangular wave is implemented as an up down counter, that count from 0 to maximum value M ,then to zero. The frequency of triangular wave which is same as the frequency of required PWM signal is given by

$$f_t=f_{FPGA}/2M$$

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Where ft is the frequency of triangle wave, fFPGA is the frequency of FPGA board and M is the maximum count value of triangle.

Sine is generated using lookup table method. A ramp signal generated by an upcounter that count from 0 to n is used to take samples of sine data from lookup table. The address ramp signal increment each time when the clock signal reaches the count which is given by

$$\text{Count} = f_{FPGA}/(\text{no. of samples (n)} * \text{frequency of sine required})$$

The firmware is implemented to vary the frequency of sine wave from 10Hz to 50 Hz. Value of count for these extreme frequencies are calculated and depending upon the switch condition S1 and S2 this count value is varied to vary the frequency. The generated sine wave is multiplied by a variable that depends upon the count value to change amplitude such that V/f remains constant. After multiplication starting value of sine is shifted to the middle of the triangle to keep the average value of the demodulated PWM remains constant. Also the sine wave must remain within triangle wave to avoid over-modulation. Phase shifted sine waves are generated by setting starting point of address ramp at 0, n/3 and 2n/3 of different instances of look up table.

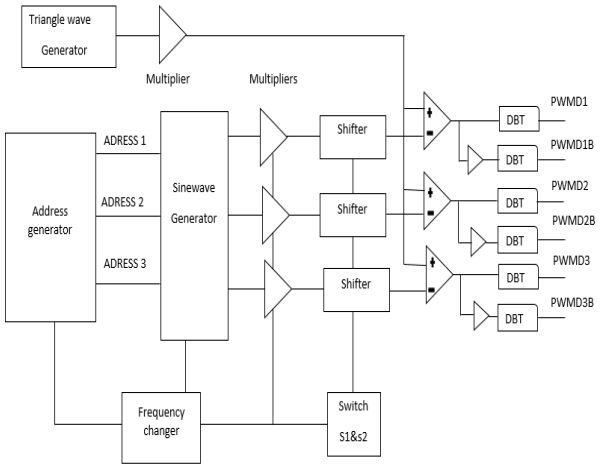

Fig 4 Firmware implementation using FPGA

IV. HARDWARE DESIGN

The hardware section consists of power circuit, controller, gate driver and induction motor. The Spartan-3 FPGA/ARM board is used as controller. Voltage source inverters are used to generate regulated AC voltage at the output. The operating voltage of the circuit is set to be 400V hence to avoid the risk having the MOSFET rating close to the operation point of the inverter at 400 V .The power circuit is designed using 12A,500V n channel power MOSFET-IRF 450. MOSFET are voltage controlled devices hence to drive a MOSFET the gate capacitance should be charged to operating voltage which is 9 to 10 volt range. But high voltage on drain of MOSFET upon interaction with gate-drain capacitance can cause problem known as miller effect. MOSFET drivers are used to avoid this issue. Here IR 2110 IC is used to dive both upper and lower MOSFET in one limb of inverter.IR 2110C has floating circuit to handle this bootstrap operation. Output pin of IR2110C can provide peak currents up to 2 ampere .it can provide fast switching speed .they can operate in switching frequency from few Hz to several hundred KHz.

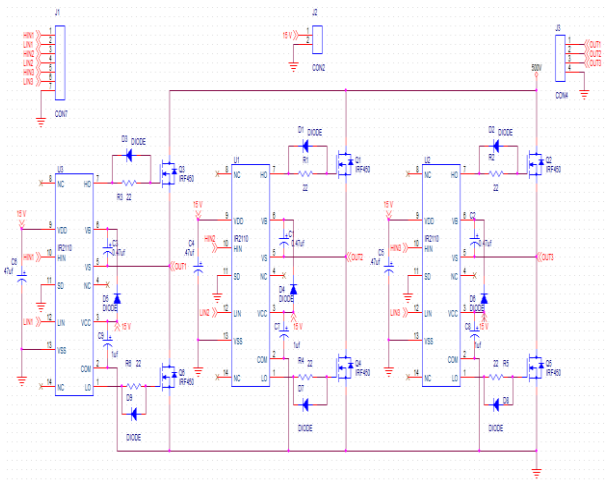

Fig 5 Inverter schematic

The drive circuit for the MOSFETs is made to work both with low voltage logic. The ports HIN and LIN of the driver are connected to control system. The port SD is for shutting down the IR2110 IC when given 5V. Bootstrap capacitor is used to push the MOSFET gate voltage to its operating voltage. Power dissipation of the gate driver circuit should not be comparable to overall power dissipation.

V. RESULTS

The complete hardware system has been developed and tested. After programming the pwm waveform is observed directly and observed after demodulating using a low pass RC filter on CRO. The frequency is varied then V/f is calculated at different frequencies.

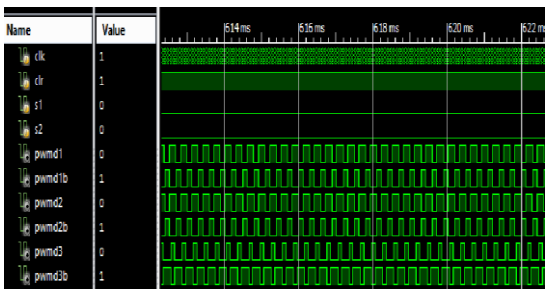

Fig 6 Simulated output for FPGA

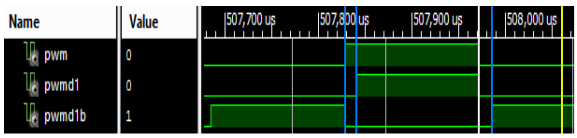

Fig 7 Simulated output showing dead time addition

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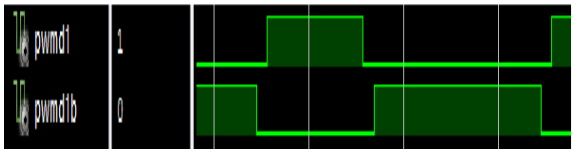

Fig 8 Simulated output showing pwm1d and pwmd1b

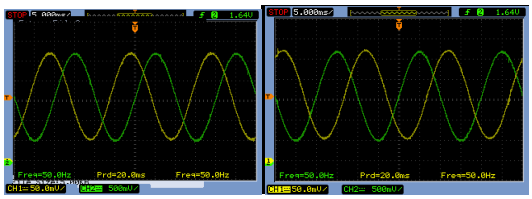
Fig 9 Filtered output waveforms from FPGA and ARM

TABLE 1 V/F TABLE FOR ARM

Sl. no	Stator voltage (V)	Gate pulse		
		(V)	(Hz)	v/f
1	76	0.48	10	0.048
2	154	0.96	20	0.048
3	230	1.44	30	0.048
4	304	1.92	40	0.048
5	379	2.40	50	0.048

TABLE 2 V/F TABLE FOR FPGA

Sl. no	Stator voltage (V)	Gate pulse		
		(V)	(Hz)	v/f
1	87	0.54	10	0.054
2	168	1.08	20	0.054
3	254	1.62	30	0.054
4	330	2.16	40	0.054
5	383	2.70	50	0.054

These PWM signals are fed into gate driver circuit and the output of the 3 phase inverter are observed by varying frequency It is clear that both amplitude and frequency of output waves changes depending upon switch condition. A table is formed using these values and the result is tabulated for both Microcontroller and FPGA outputs. From these results it is evident that we are getting constant V/f ratio.

VI. CONCLUSION

This paper presents a comparison study of induction motor drives using a Microcontroller and FPGA. The main aim of the study was to create a driver circuit and drive the motor using both Microcontroller and FPGA separately and study the results.

From the results its clear that the induction motor can be successfully driven using both FPGA and Microcontroller. The motor was driven using Microcontroller with a constant V/f ratio of 0.048 and using a FPGA with a constant V/f ratio of 0.054.From the results we can conclude that depends on the application you can choose either Microcontroller or FPGA to drive the induction motor. FPGA will give more complex and lengthy code but is flexible. User will have full control in setting dead time but controlling over modulation is difficult. Whereas when using microcontroller, coding will be easier but the user have to be within the limits of the PWM module. By careful coding over modulation can be completely avoided in Microcontroller. The designed system was successfully fabricated and tested using both controllers in the laboratory.

ACKNOWLEDGMENT

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