

International Journal of Advanced Research in Computer and Communication Engineering ISO 3297:2007 Certified Vol. 5, Issue 9, September 2016

Modelling and Performance Analysis of Zinc Oxide based Thin Film Transistor

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Abstract: In this paper, thin film of Zinc oxide is considered to be the active layer for the TFT. There are many advantages of using ZnO material as in large band gap of 3.37eV and photo transparency due to which it is extensively used in optoelectronics. The technology of macroelectronics has been the trend over the past few years and many research works mainly have been directed towards this macroelectronic domain. In this work the wurtzite crystal structure is assumed and a bottom aluminium gate TFT is designed having a glass substrate on which a layer of silicon nitrate dielectric layer is deposited, followed by the uniform deposition of ZnO active thin layer. The fabrication process is simulated on Athena framework of Silvaco TCAD and the IV characteristics of the TFT is extracted using the atlas framework. Finally the TFT is modelled into simple circuit to check the feasibility of ZnO based TFT in integrated circuits.

Keywords: TFT, ZnO, RF Magnetron sputtering, Silvaco.

I. INTRODUCTION

TFT devices with polysilicon or amorphous silicon thin ZnO can be converted into insulator, semi-conductor and a films implemented as the active layers are used in metal just by controlling the doping level, keeping the switching circuits. These materials though successful do not exhibit excellent electrical properties. Poly-Si fabrication is expensive and is literally impossible for large area deposition, if deposited it may crack under the tensile pressure of the flexible substrate. Secondly the implementation of a-Si:H TFT proves to exhibit low mobility values and lower on-off ratios [1]. The above shortcomings motivate many researchers to look for other materials, which would successfully replace these conventional ploy-Si and a-Si:H materials in TFTs. One such promising material with high carrier mobility and good on-off ratios is a metal oxide named Zinc Oxide (ZnO). This material is being researched extensively upon and it proves to be a material with the right properties and high potential. ZnO being a high bandgap material is found to be transparent, letting all the wavelengths of the stable only when grown on cubic substrates, therefore visible spectrum to pass through it. Due to these properties it finds application in displays, replacing poly-Si and a-Si:H devices. The fabrication process of this material is also straight forward and cost effective. Mostly RF magnetron sputtering technique is employed in its fabrication [2].

II. ZINC OXIDE

Zinc oxide is the most sort after material for its optoelectric properties. ZnO is also said to be available in high quality crystals, in addition the crystal growing technique is also quite simple and straight forward, therefore leading to lower fabrication cost. Several experiments conducted on ZnO confirm that it is suitable in space application due to its high resistivity property to high energy radiations.[4]

transparent property all the while hence best suited in flat panel displays and solar cell applications. Naturally ZnO is N-type conductivity configuration but if P-type like conductivity were achieved with repeatability, then ZnO would establish itself as the most preferred material in opto-electronic industry. Some properties of ZnO are discussed in brief.

A. Crystal Structure of Zinc Oxide

ZnO belongs to group II - VI, it crystallizes in hexagonal wurtzite or cubic Zinc blend structure. This structure consists of sp³ covalent bonding. The crystal structure shared by ZnO can be named as rocksalt (B1), Zinc Blend (B3) and wurtzite (B4). The rocksalt structure is obtained at high pressures, the Zinc blend structure is known to be wurtzite is the only structure which is thermodynamically stable at ambient conditions. Figure 1 shows the different forms of crystal orientation in ZnO material. In this work the wurtzite structure was considered.

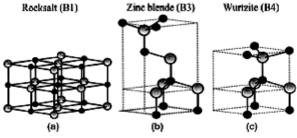


Fig. 1: 3D representation of different ZnO structures



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Β. Electrical properties of undoped ZnO

Due to its large band gap ZnO has various advantages over other material some of them include, higher breakdown voltages, capability to operate under high temperature and pressure, ability to withstand large electric fields and low noise generation etc. The electron transport in semiconductors can be considered for two conditions namely low electric field and high electric field. When low electric field is applied the field being less than the the N-type conductivity of ZnO is due to the presence of thermal energy of electrons has no effect on energy distribution of electrons as a result the material agrees well processes and it tends to diffuse quite easily into the ZnO with the Ohm's law and its electron mobility will be independent of the applied electric potential.

Now considering the case where electric field applied is increased to a point where the thermal energy of electrons is very much negligible when compared to the energy gained by the electrons. The electron distribution will not ii. P-type doping: be constant as in the case explained above and will result P-type doping in ZnO is quite difficult to achieve due to in generation of hot electrons.

C. ZnO growth

One of the many advantages of ZnO material is the ease at which superior and stable orientation of the crystalline or polycrystalline form can be deposited on various substrates like diamond glass, and sapphire. Polycrystalline type deposition was recorded using manufacturing techniques like magnetron sputtering and chemical vapour deposition. When ZnO is considered for bulk growth it is usually gown on sapphire due to the dislocation density of the pair resulting due to lattice mismatch between the sapphire orientation and ZnO's crystal orientation. In this work it is assumed that ZnO is fabricated with RF magnetron sputtering technique as presented in [3]. The RF magnetron sputtering technique has low operating temperature, is simple and cost effective when compared to the sol gel process and chemical vapour deposition (CVD) processes. This process involves certain process enhancing gases like oxygen (O₂) and argon (Ar), here the role of oxygen gas is to enhance the process by acting as the reactive gas and argon acts as sputtering enhancing gas. The RF power applied is varied in order to control the sputter yield rate from the target which is a ZnO crystal. In specific when ZnO was deposited on Si substrate of orientation (100) by reactive sputtering process n-type conductivity was achieved under low O₂/Ar concentration ratios and p-type conductivity was obtained when the O_2/Ar concentration were quite high [3][4].

Therefore both types of conductivity are achievable from this technique of RF magnetron sputtering just by varying the fabrication parameters like temperature and process enhancing gas concentration ratios.

D. N and P type doping

Like majority of large band gap materials, doping to achieve bi polar carriers is difficult whereas unipolar Ntype doping is quite possible, in fact naturally ZnO is Ntype doped. P-type doping is bit difficult to achieve when closer to the gate is moderately doped while the region compared to the ease at which N-type conductivity is closer to the source and drain contacts are quite heavily achieved in ZnO material.

i. N-type doping:

ZnO with wurtzite structure is naturally N-typed doped due to the presence of O_2 vacancies (O) and Zn interstitials. Though N-type conductivity is achieved the exact reason behind this donor formation is not clearly known, donors might be contributed either by O vacancies or Zn interstitials. Experiments conducted by various groups have given conclusive evidence and reported that hydrogen gas which will be present in all manufacturing material. Doping with aluminium (Al), gallium (Ga) and indium (In) has been attempted in many research groups resulting in better performing ZnO material in quality and conductivity alike [4].

one of the following reasons i. low solubility of dopant in ZnO material, ii. Deep impurity levels. Via extensive research and trials it is been believed that group V elements like nitrogen (N), phosphorous (P), arsenic (As) are most promising dopants to induce a P-type conductivity in ZnO material [4]. The group V elements replace the Zn interstitials and occupy its positions in the crystal lattice.

In this work Al and P are used to dope ZnO into N-type and P-type conductivity respectively. But phosphorous has larger bond length hence may induce lattice strain, in turn creating antisites. These antisites are again donor in nature and cancel out acceptor concentration, therefore practically nitrogen is preferred over phosphorous. But in this case due to unavailability of nitrogen as dopant option the next better option phosphorous was considered. In order to compensate for the acceptor loss due to the donor formation ZnO layer was slightly heavily doped with phosphorous.

III. TFT DESIGN AND IMPLEMENTATION

Since macro electronics deals with devices on flexible substrates, plastic substrates or fabrication on insulators; in this work we have considered Silicon dioxide as the substrate, which is similar to glass substrate and acts as an insulator. An aluminium gate is used in bottom gate staggered configuration. Aluminium is preferred due to its good work function and the bottom gate staggered configuration is simple to fabricate and widely used in industries. The dielectric layer employed is Silicon nitride, it was preferred over silicon dioxide due to its high k dielectric nature than silicon dioxide. Following the silicon nitride layer a thin layer of ZnO active material is deposited. As discussed earlier the undoped or un intentionally doped layer of ZnO exhibits N-type conductivity due to O vacancies and Zn interstitials. To enhance the donor concentration the part of the thin layer doped with aluminium.

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The source and drain contacts are again aluminium. The exposed part of the ZnO layer after deposition of source and drain contacts is etched. As in the case of other materials ZnO does not require a passivation layer to protect it from sunlight and external atmosphere. This is mainly due to ZnO's optical transparency property. Therefore in this design no passivation layer is provided leading to one less fabrication step, an added advantage. The fabrication of this device is simulated with the Athena framework of Silvaco TCAD tool [6] and the fabrication flow graph. The transfer characteristics are obtained after the device is evaluated by the Atlas framework of Silvaco TCAD tool [7]. For the evaluation to be successful the electrical characteristics of the ZnO material have to be clearly defined. Various parameters like band gap, electron and hole concentration and the defect densities were clearly defined [5][7]. After favourable transfer characteristics are obtained the TFT design is modelled into device and a simple inverter circuit is designed. The results obtained are clearly explained in the results and discussion chapter.

IV. RESULTS AND DISCUSSION

Following the simulation of the fabrication process the Atlas framework analyse each grid applying predefined models and based on the electrical properties like bandgap and density of states plots the transfer characteristics like drain current vs gate voltage / drain voltage graphs. The plots numbered as figure 2 and 3 are the transfer characteristics. The plot 5 represents the drain current (Id) vs drain to source voltage and the plot 6 represent Id vs gate to source voltage.

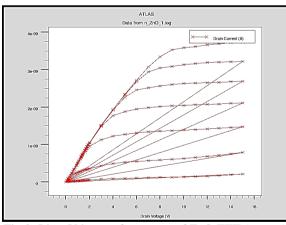


Fig 2: Id vs Vds transfer curves of ZnO TFT (n-type)

In the Id vs Vds plot the gate voltage is ramped up starting from 1V up to 13V in steps of two volts. Same is reflected in the plot, the curve nearer to the x-axis and top most curves correspond to 1V and 13V respectively. A saturation current of 3.60nA was achieved for a gate bias of 13V. Similarly the Id vs Vgs represent the curves for different drain voltages. The curves nearest and farthest from the x-axis correspond to drain voltage of 2V and 10V respectively, increasing in steps of 2V.

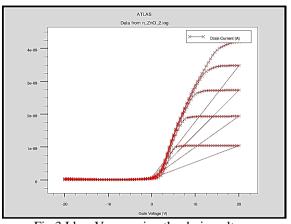


Fig 3 Id vs Vgs varying the drain voltage (n-type ZnO TFT)

The Threshold voltage of the device recorded for the channel length of 10um and an drain voltage of 1V was about 1.69V. Various other varied parameters are given in the table 1. In which Vt values and on-off ratios are tabulated for different channel lengths.

The DC voltage to the inverter is ramped from 0V to 20V with VDD of 15V. For the transient response the initial voltage is set to 0V and the final voltage is set to 5V. The delay time set to 0s and rise and fall time set to 10us each. The pulse width and time period set to 150us and 300us respectively. Both the DC plot and the transient analysis plot is given in figure 4 and 5 respectively.

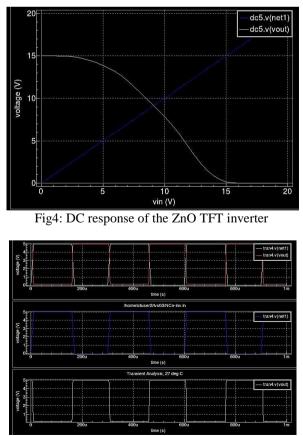


Fig5: Transient response of the ZnO TFT inverter

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V. CONCLUSION

Based on the results obtained, we conclude that integration of ZnO TFT in integrated circuits is feasible and if p-type ZnO TFT fabrication is made possible on regular basis, ZnO would be the better option to replace crystalline silicon on flexible substrates and large area fabrication. Further work should be done to implement ZnO TFT in various other circuits like amplifiers and Op-amps. Digital logic implementation using CMOS like (n-type and ptype) ZnO TFTs can also be considered for future work. The stress and strain test of ZnO would completely solidify its role in replacing crystalline Si in

macroelectronics. As discussed earlier the fabrication of ptype conducting ZnO thin films are proving to be quite difficult, but if this made achievable with descent repeatability then ZnO thin film based integrated circuits would capture the macroelectronics industry and market.

REFERENCES

- [1] Kuo Yue, Thin Film Transisitor technology- Past, Present, and future, The Electrochemical Society Interface, Springer 2013.
- [2] R. L. Hoffman, B. J. Norris and J. F. Wager, "ZnO-based transparent thin-film transistors", Appl. Phys. Lett., Vol. 82, No. 5, 3 February 2003
- [3] Christian Brox-Nilsen, Jidong Jin, Yi Luo, Peng Bao, and Aimin M. Song, "Sputtered ZnO Thin-Film Transistors With Carrier Mobility Over 50 cm2/Vs", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 10, OCTOBER 2013.
- [4] Ü. Özgür, Ya. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, "A comprehensive review of ZnO materials and devices", journal of applied physics, AIP, pg 98, 2005.
- [5] Faruque M. Hossain, J. Nishii, S. Takagi, A. Ohtomo, T. Fukumura, "Modeling and simulation of polycrystalline ZnO thin-film transistors", Tohoku University, Aoba-ku, Sendai; The University of Tokyo, Bunkyo-ku, Tokyo; Tohoku University, Sendai; Tokyo Institute of Technology, Yokohama; Japan
- [6] Athena user manual, www.silvaco.com.
- [7] Atlas user manual, www.silvaco.com
- [8] Utmost4 user manual, www.silvaco.com
- [9] Gateway user manual, www.silvaco.com