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Design and Analysis of Fundamental Gates and Adder using Adiabatic Array Logic

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Abstract: Adiabatic logic uses the principle of reversible logic in order to minimize the power consumption. The reduction of power dissipation in adiabatic is achieved through the use of power clock instead of DC voltage. Adiabatic switching is mostly used to minimize the power consumption during charging and discharging. The main purpose is to design a low power circuit using adiabatic array logic which consumes less power. In this paper we have designed fundamental gates adders using adiabatic array logic and compare their power dissipation, delay and area with CMOS logic

Keywords: Adiabatic Array Logic, Complementary metal oxide semiconductor (CMOS), Quasi adiabatic logic, Carry Select Adder (CSLA) , fundamental gates.

I. INTRODUCTION

In today VLSI design methodologies, power consumption is the major factor. Power reducing is one of the important concerns in today's life. It has two important factors, first is long time batteries operation and desirability of portable devices and second one is due to increases large number of transistors on a single chip causes high power dissipation and it also effects the IC packaging. As the demand of portable devices increasing day by day then require for low power circuit is become the major issue in high performance digital circuits like as digital signal processing, microprocessors and many other applications. In these applications, power has become an important concern. As end users need small devices with longer time battery life. Reducing power dissipation of the digital circuit systems because more important, especially in these portable and operated systems. Adiabatic switching is recently a new technique to reduce power dissipation in digital circuits. In adiabatic switching, the process of charging and discharging is done in a way that a less amount of power is dissipated. Adiabatic switching circuit requires invariable, non standard power supply with ramp voltage. This power supply is called pulsed power supplies. Several adiabatic logic families are developed in recent years. These are classified as fully adiabatic logic and quasi -adiabatic logic. But the quasi adiabatic logic is further divided into two groups. Ist is rank-1 quasi adiabatic logic and second is rank-2 adiabatic logic

II. BASIC OF ADIABATIC LOGIC

The term 'adiabatic' refers to the thermodynamic processes in which no heat exchange from the environment. It does not release energy from system to environment and therefore no dissipation energy loss. In adiabatic total energy in the system remains constant[1]. Adiabatic also allows the recycling of energy. It means we will transfer the energy back after some computational done to back to the power source. Therefore the heat from the power source to the circuit and transfer back to the power source. So the power supply is designed in this way that it regain the energy back to it. Adiabatic circuits use reversible logic to reduce the power dissipation.. Reversible logic is defined as the number of inputs equal to the number of outputs. Reversible logic circuits have one to one mapping[2].

Adiabatic circuits can operate only in the MHz range, it does not operate in the GHz range. Adiabatic loss is proportional to the frequency. So Adiabatic loss increases when the frequency of operation increases. They are much smaller into their standards, there are so many applications in which we use adiabatic circuits for example pacemaker whom need not really operate at a very high frequency, no need of operation need not be very high, but saving of energy is very important, because we cannot change the battery everyday and battery placement is dangerous. Adiabatic Logic is classified into two groups, one is asymptotically adiabatic logic and second is quasi adiabatic of partial energy circuits.

III. THE CHARGING PROCESS IN ADIABATIC LOGIC COMPARED TO STATIC CMOS

First we consider the energy dissipated in the static CMOS logic. In CMOS circuits sources of power dissipation are dynamic, short circuit and leakage power dissipation. The dynamic power dissipation is when the load capacitance charging and discharging. Equivalent circuit to CMOS logic for charging and discharging as shown in figure 1.1.

When charging through a resistor initially current is maximum because the voltage across the capacitor is zero. So enter voltage is developed across the resistor. Current of Vdd/R will flow initially. Current decreases with time and will become zero. The total power dissipation in CMOS logic is given by:-

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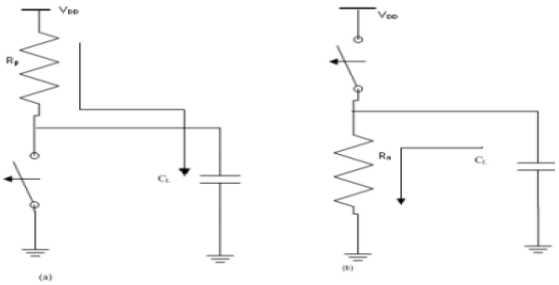
Ec = (1/2).C.Vdd^2



Fi Figure No: 1.1 Conventional CMOS a) Charging b) Discharging

Adiabatic circuits the energy dissipated during switching process. In fig 1.2 R represents the on resistance of the PMOS network. Load capacitance is not having any charge at time zero[3, 4, 5]. The capacitance voltage Vc is zero initially. In adiabatic switching a current source I(t) is used for charge the capacitance C, which is being applied across a resistor R. The voltage across the capacitance as a function of time Vc(t) is given as:-

$$Vc(t)=(1/C).I(t)t$$

$$I(t)=C.Vc(t)/t$$

The energy dissipated is given by:-

$$Ediss = R.I^2(T).T$$

$$Ediss = (RC/T).C.V^2(T)----------(1)$$

From the equation (1), the energy dissipation is opposite to the transition time T. This shows that less energy will dissipate when capacitor charge slowly. The energy dissipation is not only control by the transition time T, but also the resistance R which is absent in CMOS.

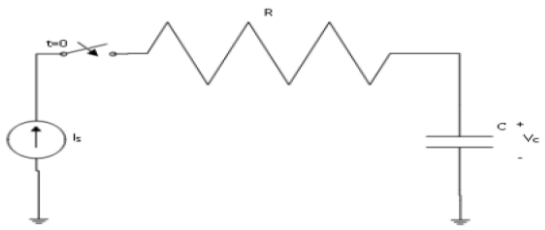


Figure No. 1.2- Adiabatic switching

For minimize the dissipated energy:-

$$Eal < Estatic$$
$$(RC/T)C.Vdd^2 < (1/2).C.Vdd^2$$
$$T > 2.R.C$$

So to reduce the power consumption, increase the value of T and second is instead of voltage quickly we can applied another voltage which rise more slowly and so we can make T>2.R.C. And another approach is to reduce the value of R so that it to make the less than (1/2) C.Vdd^2.

IV. ADIABATIC ARRAY LOGIC

Adiabatic array logic is type of Rank-2 quasi adiabatic logic. The Rank-2 is composed of state 0 or 1 is state and some of the input information is destroy in this. Adiabatic array logic shown in figure 1.3.

The circuit which drives the sinusoidal power supply is based on array logic. The logic consists of an array which is consists of transmission gates. These transmission gates made by AND plane and the desired output from this plane are drawn by some wired connections called the wired OR plane[6.7].

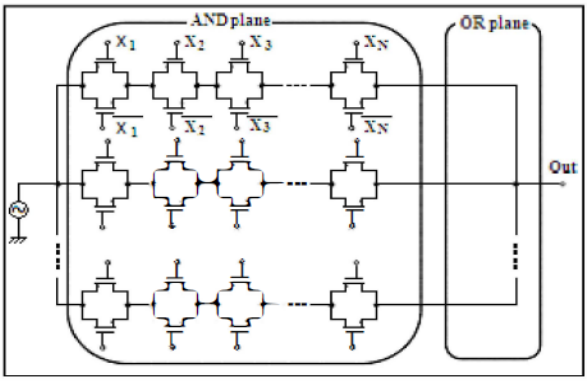


Figure No.1.3- Adiabatic array logic

In adiabatic array logic instead of DC voltage power clock is given so the the voltage rise more slowly. If the voltage increases very slowly then the time period is increases and the time is greater than the value of resistance and capacitor.
And energy dissipation of the circuit is inversly proportional to the time period. If the time period is increases than the energy dissipation is decreases.

Capacitance C is calculated in the triode region for both transistors is given as:

$$Cgs = (W*L*Cox)/2+W*Cov$$

Where, W and L are the width and length of the transistor, Cox is the oxide thickness capacitance, Cov is the parasitic overlap capacitance.

V. FUNDAMENTAL GATES AND ADDERS USING ADIABATIC ARRAY LOGIC

Design and analysis of fundamental gates and adder circuits at cadence virtuoso tool and to implement fundamental gates and adder circuit using adiabatic array logic and CMOS logic at 45nm technology.

a NOT Gate

In Adiabatic inverter there is one PMOS transistor and one NMOS transistor. Both are connected to the power clock. If the input is false then output is true.

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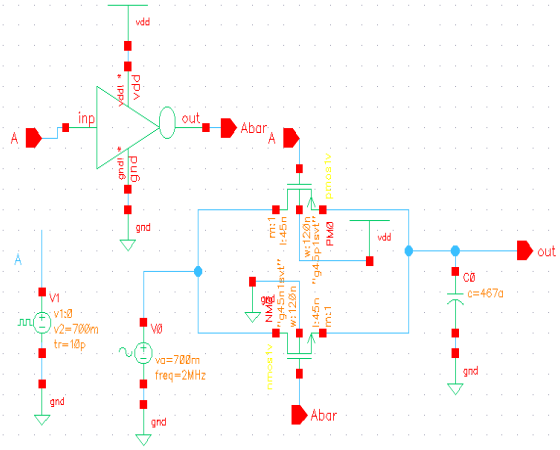
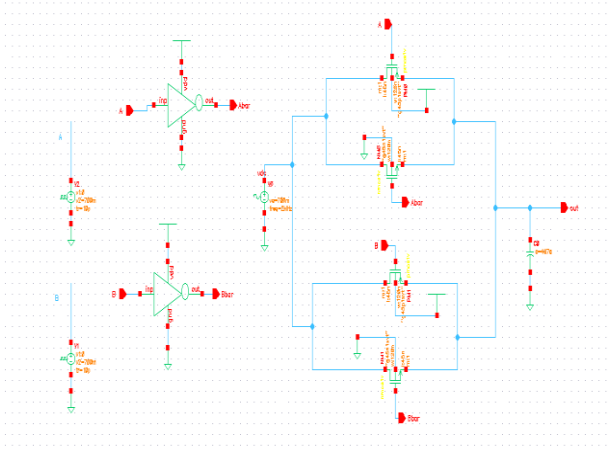


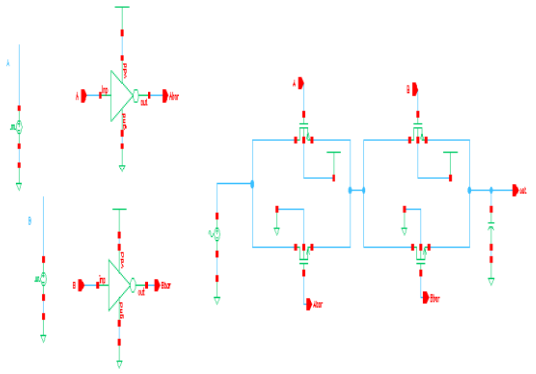
b NAND Gate

In adiabatic NAND gate there is two PMOS transistors and two NMOS transistor. In NAND gate there is two inputs and one output.



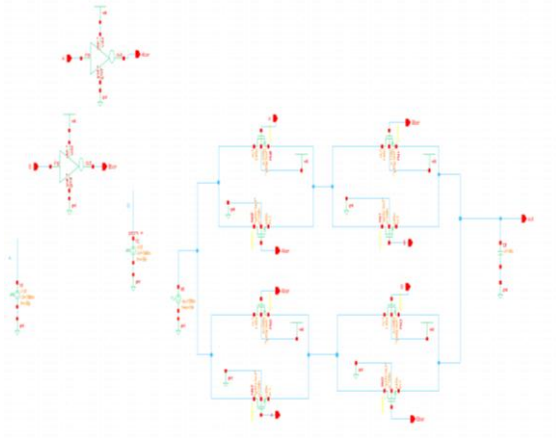
c NOR Gate

In adiabatic NOR gate there is two PMOS transistors and two NOR transistor. In NOR gate there is two inputs and one output.



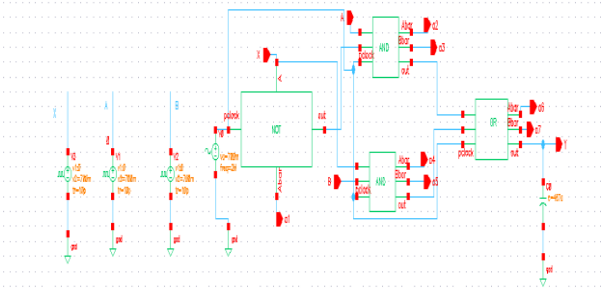
d XOR Gate

In adiabatic XOR gate there is four PMOS transistors and four NMOS transistor. In XOR gate there is two inputs and one output.



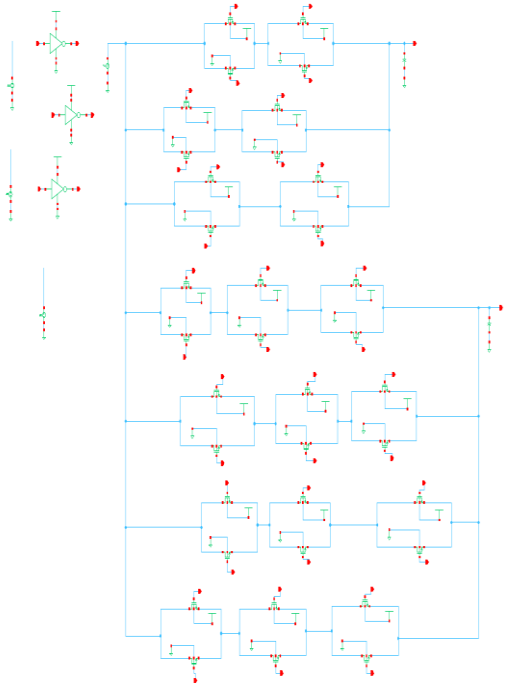
e 2:1 MUX

Adiabatic 2:1 multiplexer has 2 inputs , 1 select line and 1 output. Multiplexer combine the many signals into one signal. Multiplexer consists of one not gate, two and gate and one or gate.



f FULL ADDER CIRCUIT

Adiabatic Full adder consists of 36 transistors. The circuit produces two bit output and outputs are sum and carry.



g RIPPLE CARRY ADDER CIRCUIT

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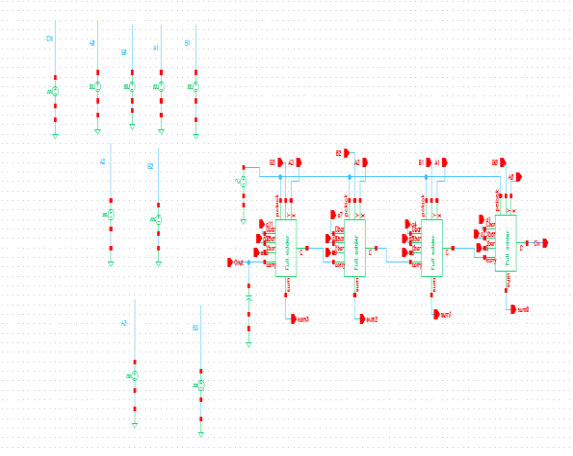
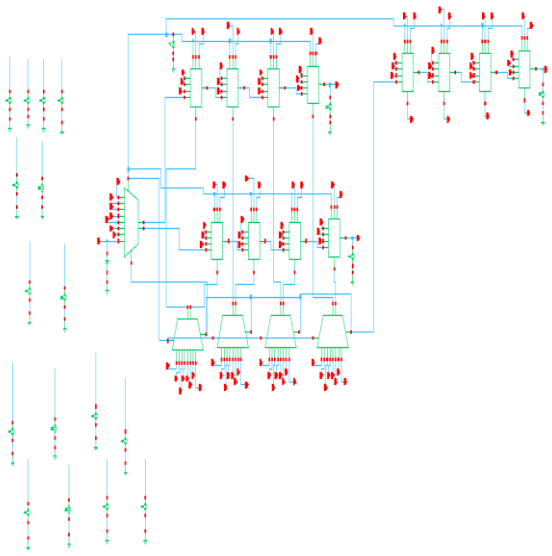
Ripple carry adder consists of 4 full adder circuits. In ripple carry adder carry output of each full adder circuit is carry in of the succeeding to next full adder circuit. In ripple carry each carry bit is rippled into the next stage.



h CARRY SELECT ADDER CIRCUIT

Carry select adder is fast adder which is used in many arithmetic functions. Carry select adder consists of ripple carry adder and 2:1 multiplexer. In CSA one ripple carry adder has carry zero and another ripple has carry one.



VI. PERFORMACE ANALYSIS

A. Comparison of Power dissipation

circuits	CMOS	Adiabatic
Inverter	22.76 n	18.03 n
NAND	44.9 n	34.11 n
NOR	38.76 n	25.51 n
XOR	81.16 n	50.77 n
MUX	86.94 n	64.94 n
FULLADDER	342.3 n	101.1 n
RCA	2.031 u	1.325 u
CSA	7.391 u	4.23u

B Comparison of area per chip
Area per chip is calculated by W*L*Transistor count

Circuits	CMOS	Adiabatic
Inverter	10.800u	10.800u
NAND	21.600u	21.600u
NOR	21.600u	21.600u
XOR	43.200u	43.200u
MUX	75.600u	75.600u
FULLADDER	216.000u	194.400u
RCA	864.000u	777.600u
CSA	2970.00u	2710.800u

C Comparison of propagation Delay

circuits	CMOS	Adiabatic
Inverter	1.225 u	1.53 u
NAND	728.2 u	1.419 u
NOR	1.732 n	323.6 n
XOR	731.7 n	250.5 n
MUX	103.4 n	205. 69 n
FULLADDER	207.4 n	250.5 n
RCA	98.01 n	104.65 n
CSA	57.24 n	85.91 n

D Comparison of Power Delay Product

circuits	CMOS	Adiabatic
Inverter	27.881f	27.586 f
NAND	32696.18 f	48.4021 f
NOR	67.132 a	8255.04 a
XOR	59384.772 a	12717.88 a
MUX	8989.596 a	13357.509 a
FULLADDER	70993.02 a	20776.05 a
RCA	199.058 f	138.661 f
CSA	423.06 f	363.399 f

VII. CONCLUSION

Adiabatic logic circuits provide a method of decreasing the energy dissipation when compared with CMOS logic. We have presented adiabatic circuits using array logic. In cadence virtuoso tool we design basic fundamental gates and full adder circuit, ripple carry adder and carry select adder using adiabatic array logic and CMOS logic at 45nm.

The power dissipation, Area per chip, Propagation delay and Power delay product of circuits are calculated. From simulation results, it is clear that the power dissipation of proposed array adiabatic logic is lower than the CMOS logic.

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