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Implementation of Low Power and Area Efficient Shift Register by Register Reusing

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Abstract: As the Word length of the shift register increases, the area and power consumption also increases. This paper proposes a low power and area efficient shift register by register reusing. In this system the multiple non-overlap delayed pulsed clock signals is used which timing problem between pulsed latches. The small number of pulsed clock signals used by grouping the latches to several subshift registers. Moreover, the similar functional operation of Register Reusing has been explained by using the Twisted Ring counter.

Keywords: Pulsed latches, pulsed Generator, Twisted Ring counter (TRC), Sub Shift Registers.

I. INTRODUCTION

Since 1970's VLSI plays a major role in communication and semiconductor devices. VLSI (Very Large Scale Integration) comprises thousands of transistors on a single IC Chips. VLSI is majorly linked with Low power, Area and Speed. Mainly CPU, ROM and glue logic all these functions are performed on a single VLSI Chip. The Power Consumption is important phenomenon in many applications. VLSI design builts its structures as such as design analysis, design implementation, computer-aided design, simution, testing. In VLSI modular technology it majorly deals with reducing interconnecting fabricating microchip Area. It is the one where rectangular blocks are constructed by repitive structures and they are connected by using wiring. For instance, the layout has been partioned into equal bit slices.

In digital circuits shift registers is used to construct many applications and it is the basic building block. It is constructed by connecting flipflops for data transmission and it is majorly used for shifting the data .flip-flops deals with the timing problem. So inorder to avoid timing problem we used Pulsed latches instead of flipflops. Thee pulsed latches also deal with timing problem but compared pulsed latches, flipflops produces larger timing problem.
Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock, and all are set or reset simultaneously

A register that allows each of the flip-flops to pass the stored information to its adjacent neighbour. The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity. A computer or microprocessor-based system commonly requires incoming data to be in parallel format. But frequently, these systems must communicate with external devices that send or receive serial data. So, serial-to-parallel conversion is required. Generally to produce dealy in the circuits The serial in -serial out shift register can be used as a time delay device. The amount of delay can be controlled by: 1. the number of stages in the register 2. the clock frequency .

This paper proposes a N-bit shift Register by using register reusing concept. The pulsed latch has been used to reduce the time delay in the circuits. SSASPL (static sense differential amplifier shared Pulsed Latch) which is the smallest latch with less number of transistors. The same similar operation of latch and flipflop is explained by using twisted ring counter or simply called as Johnson counter.

II. ARCHITECTURE

A. SHIFT REGISTER: The Existing method comprises of the design of the shift register by using pulsed latches. Moreover the Architecture of the shift register consists of pulsed clock generator which is used for generating clock pulses to the latches. Then, it also consists of sub-shift registers blocks and it also contains temporary storage latch to produce some time delay.

B. Ssaspl latch
As shown in the figure(1)static differential sense amp shared pulse latch).It consists of 7 transistors. The latch consists of one cross coupled inverters and it also consists of 3 NMOS transistors (M1-M3). The lowest clock power has been achieved because the pulsed clock signal is shared with one single transistor M1.Thecomplementary data ouput has been obtained based on the data input D and Db. The three NMOS transistors has been designed as

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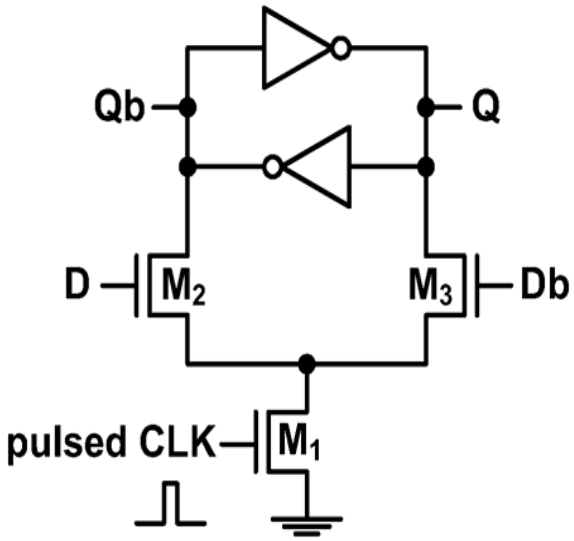
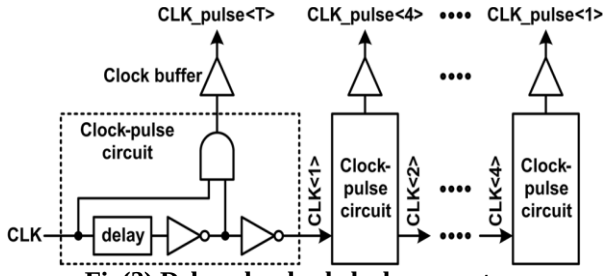
such transistors has been used to hold the data with four transistors (cross-coupled-inverters). It also needs differential data inputs and pulsed clock signal. If the pulsed clock signal input is high so it updates the data. The node q or qb is pulled down to ground according to the complementary data inputs. The output signals of the first latch (Q1 and Q1b) change correctly, because the input signal of the first latch (IN) is constant during the clock pulse width . On the other hand, the output signals of the second latch (Q2 and Q2b) do not change, because the input signals of the second latch, which are connected to the output signals of the second latch (Q2 and Q2b), change during the clock pulse width. The SSASPL flip the states of the cross-coupled inverters (Q and Qb) by pulling current down through either or during the clock pulse width. The clock pulse width is selected as the minimum time to flip the output signals of the latch (Q and Qb) when its input signals (D and Db) are constant. If the input signals change during the clock pulse width, the time pulling current down through either or becomes shorter than the clock pulse width, so that the latch has not enough clock pulse time to flip the output signals after the input signals change.



Fig(1) Schematic of the SSASPL

C. DELAYED PULSE CLOCK GENERATOR



Fig(2) Delayed pulsed clock generator.

The pulsed clock generator consists of delay circuit AND gate. The delayed pulsed clock generator is useful for generating small pulsed clock signals. The AND gate and delayed pulsed clock signals are used to generating sharp pulsed clock signals so that summation of rising and falling edge is shorter. The number of latches and clock pulse circuits changes according to word length of the subshift registers.

D.SUB-SHIFT REGISTERS

The M number of stages of sub-shift registers has been used to shift the data through the latches (q1-q5).the temporary storage latch named as T1-TM . It does not produce the same data to the next sub-shift registers it changes according to the input of the bit transferred to the latches. Fig (3)show the block diagram of existing shift registers and fig(4)show the schematic waveform for existing shift register.

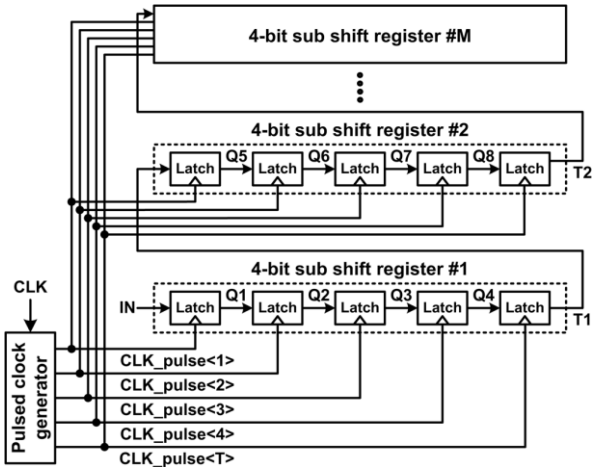
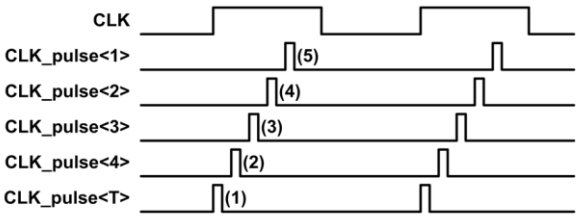
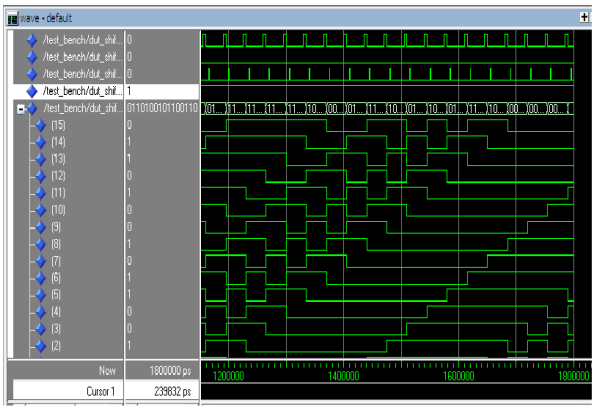


Fig (3) Existing Shift Register



Fig(4) Schematic Of Existing Shift Register

E. OUTPUT WAVEFORMS



Fig(5) Waveform of shift register

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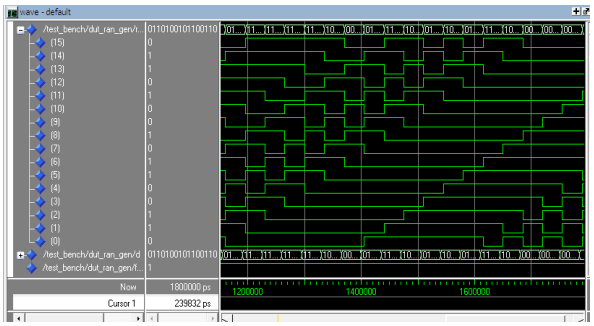
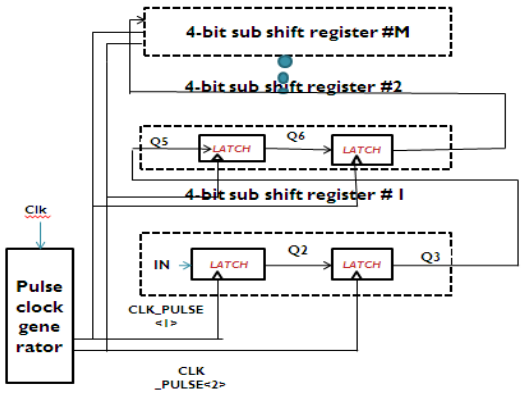


Fig(6)Waveform of random pulse generator

III. PROPOSED ARCHITECTURE

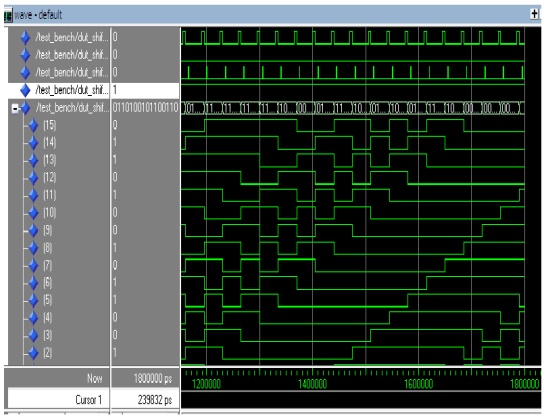
A. REGISTER REUSING

The Register Reusing is the concept introduced in the proposed shift register as shown in fig.7.The number of latches has been reduced .The structure consists of two latches .the shifting of data happens without delay. The structure consists of m-bit sub shift registers. The pulse generator which continuously provides clocks pulses to the latches. The operation of the existing shift register is same as performed by the proposed shift register. The same set of registers has reused to shift the data bits. Due to Register Reusing the area time and delay has been reduced greatly in proposed shift regiser.



Fig(7)proposed shift register

B.OUTPUT WAVEFORMS



Fig(8)waveform of Register Reusing

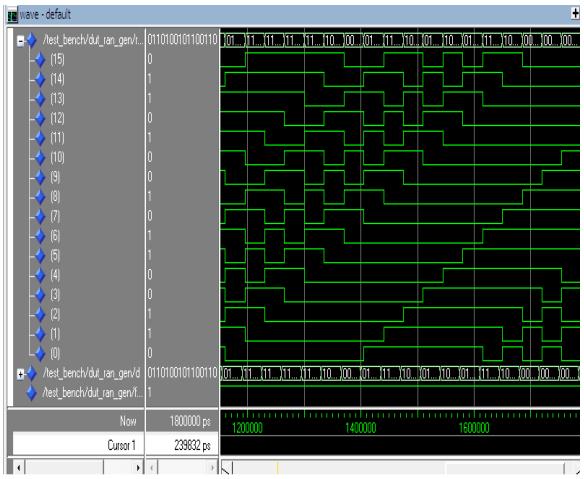


Fig (9) waveform of random generator

The similar phenomenon of Register Reusing concept has been explained in testing methodologies. The methodology has been explained by using twisted ring counter. If data volume increases simultaneously it need to change Automatic Test Equipment (ATE).and it requires Additional Test Application Time (TAT).To rectify the above problems we choose built in self test (BIST) and test data compression. The code based scheme compresses test data in the form of code words.

C. TWISTED RING COUNTER

As shown in the fig (8) the Twisted Ring Counter (TRC) Consists of decompressor and multiplexer and scan chains. The TRC consists of flip-flops it is used to store the test data. The R-TRC block has been used to improving reuseable data. (i.e) the feedback and twist characteristics of R-TRC for reusing previously test data. The values used here are the tri-state values. The multiplexer needs feedback and twist mode. The Twistmode data can be selected based on C_in data. The save and change of test data is based on the operation of multiplexer. The decompressor is used to continuously generate the data at a fixed length. scan chain receives the data signals. R-TRC is the general memory block to store the data inputs.

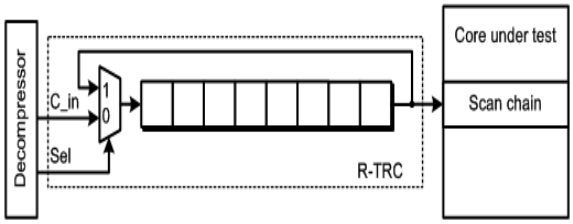


Fig (10) A simple test architecture using the 10-bit R-TRC.

D. ARCHITECTURE

The method consists of Automatic Test Equipment (ATE), Tristate detector, Decompressor, R-TRC, scan chain.ATE is responsible for generating Test Data Inputs (TDI).The range information has been increased and ATE used does not require additional ports.

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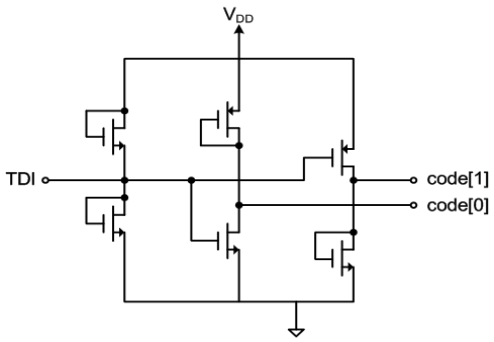
The tristate detector is that the TDI inputs has been is converted into 2-bit binary value .this conversion is responsible for decompressor and registers to analyse the Hi-Z value. The tristate detector consists of only 6 transistors and it produces two ouputs in the form of codes as shown in the fig (10).



Fig(10)Tristate Detector

d. CONTROL AND GENERATOR UNIT

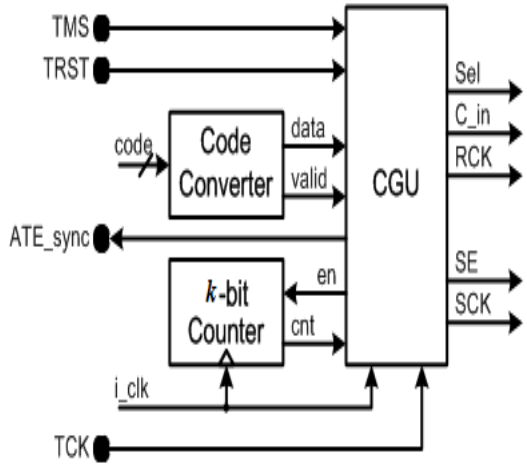
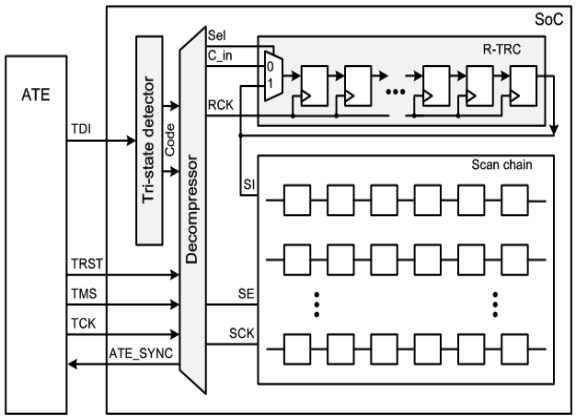


Fig (11) Decompressor for TSC

The code converter has simple combinational logic in order to identify the code data that are outputs of the tri-state detector. It has two input and two output ports and its truth table is shown in Table VI.



Fig(12)Proposed Architecture

The *kk*-bit counter helps to control the CGU to enable the shifting operation from the R-TRC to the scan chain, where *kk* is $\lceil \log2(llSSSS+1) \rceil$. The CGU is responsible for controlling the R-TRC and the scan chain, delivering the decompressed test data to the scan chain, adjusting the suitable clocks among the ATE clock and the internal clock and synchronizing the clocks between the ATE and the internal circuit.

F. OUTPT WAVEFORMS

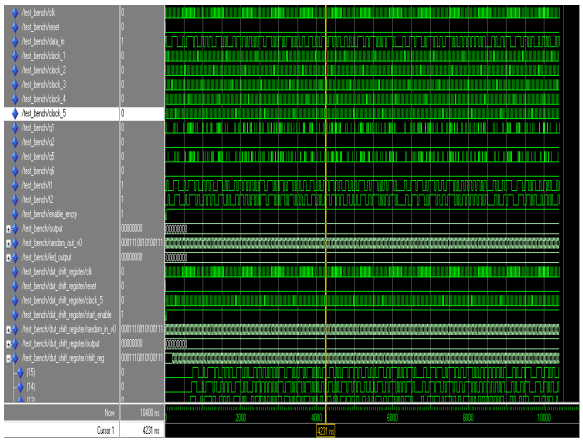


FIG (13) waveform of twisted ring counter

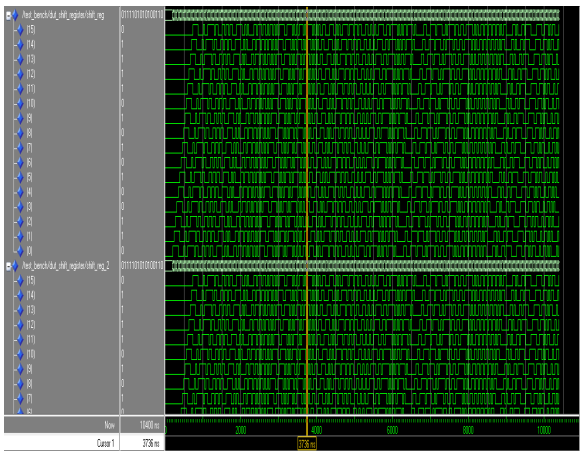


FIG (14) Waveform of Decompressor

IV. CONCLUSION

The proposed system uses the less number of latches compared to the existing system. The same shifting operation has been done in the Register Reusing concept. Moreover the Twisted Ring Counter explains the similar functional operation of Register Reusing in testing scenario. Thus area time, area and delay consumption has been reduced.

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