ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE
International Journal of Advanced Research in Computer and Communication Engineering

NCRICT-2017
Ahalia School of Engineering and Technology

Vol. 6, Special Issue 4, March 2017

Chip Morphing by Efuse

Harikrishnan A I[1], Lashmi K[2]

Assistant Professor, Department of ECE, NSS College of Engineering, Palakkad, India[1]

Student, Department of ECE, NSS College of Engineering, Palakkad, India[2]

Abstract: Chip morphing enables a new class of semiconductor products that can monitor and adjust their functions to improve their quality, performance and power consumption without human intervention. Chip Morphing Technology deals with eFUSE. eFUSE is part of a built-in self-repair system that constantly monitors a chip's functionality.It combines unique software algorithms and microscopic electrical fuses to produce chips that can regulate and adapt their own actions in response to changing conditions and system demands.

Keywords: Chip morphing, EFuse, Programming, Sensing.

I. INTRODUCTION

Chip morphingis a technology invented byIBMwhich allows for the dynamic real-time reprogramming of computer chips. Computer logic is generally "etched" or "hard-coded" onto a chip and cannot be changed after the chip has finished being manufactured. By utilizing a set of eFUSEs, a chip manufacturer can allow for the circuits on a chip to change while it is in operation. The primary application of this technology is to provide in-chip performance tuning. If certain sub-systems fail, or are taking too long to respond, or are consuming too much power, the chip can instantly change its behavior by "blowing" an eFUSE. IBM System z9 is the first z-Series product to use electronic fuses (eFUSEs) on July 30, 2004. The blowing of the fuse does not involve a physical rupture of the fuse element, but rather causes electro-migration of the silicide layer, substantially increasing the resistance. The fuse is 'blown' with the application of a higher than nominal voltage. eFUSEs provide several advantages over the laser fuses they have replaced.The physical and logical implementation of eFUSEs has resulted in improved yield at wafer, module, and final assembly test levels, and has provided additional flexibility in logic function and in system use. In this paper we discuss circuit design, fuse programming, and test considerations.

II. EFUSE EVOLUTION

First generation of electrical fuse was implemented using a tungsten silicide (WSi) polysilicon process. At that time metal laser fuse was the preferred method of manufacture, and the eFUSE basically mimicked the operation of laser fuse, with high resistance achieved by breaking the fuse link, but this produced significant collateral damage. The second generation of electrical fuse development began with the 0.18pm logic technology using cobalt silicide (CoSi2) polysilicon. The basic building block of the fuse remained the same with optimization of the fuse structure to improve the programming window. This fuse link introduced programming via electromigration, with no collateral damage. A programming Current (I=12mA) and anode voltage (Fsource-5V.) range were established to produce the desired electromigration phenomena. The fuse achieved typical programmed resistance in excess of 100KΩ with all fuses over 10KΩ.

The third generation included the eFUSE kit with a self-repair eFUSE controller circuit and built-in-self test (BIST). The fourth generation of electrical fuse development began with a low-voltage (IPROG=7mA typ. and VFSOURCE=1 .5V typ.) fuse in 65nm and 45nm logic technology. The NixSix fuse element was scaled to accommodate a lower fuse programming voltage requirement with standard gate oxide FETs, and the density was improved.

III. EFUSE CIRCUIT DESIGN

The silicidedpolysilicon in efuse is the element that is blown or programmed through an electro-migration event. Upon programming, eFUSE's show a large increase in resistance that enable easy sensing that is, the structure is typically programmed using a standard NFET in conjunction with appropriate select circuitry. eFUSE programmed under two opposing current directions show depleted regions near the cathode with corresponding accumulations in the anode. This signature is reversed when the current direction is reversed. When the gate pulse is raised above 1.5 V, the entire structure is ruptured and the location of the rupture is typically in the middle of the link, independent of polarity.The final resistance is hence significantly higher than the resistance expected.

The programming circuitry consists of two large-series n-FET transistors designed to draw a large amount of current (10–15 mA). The sense circuitry is the structure that reads the state of the polysilicon fuse.

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE

International Journal of Advanced Research in Computer and Communication Engineering

NCRICT-2017

Ahalia School of Engineering and Technology

Vol. 6, Special Issue 4, March 2017

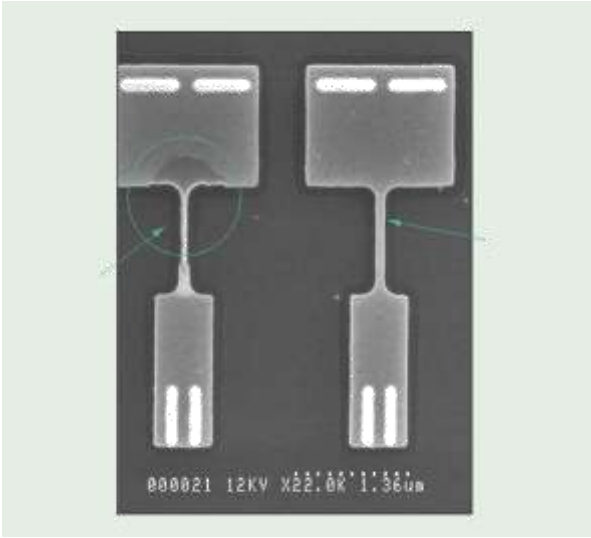

Fig 1 shows a scanning electron microscope image of blown and unblown eFUSEs

The control logic controls the fuse program and fuse read. operations. An external voltage source, called Fsource, is used to program fuse elements (at .3.3 V) and read them.

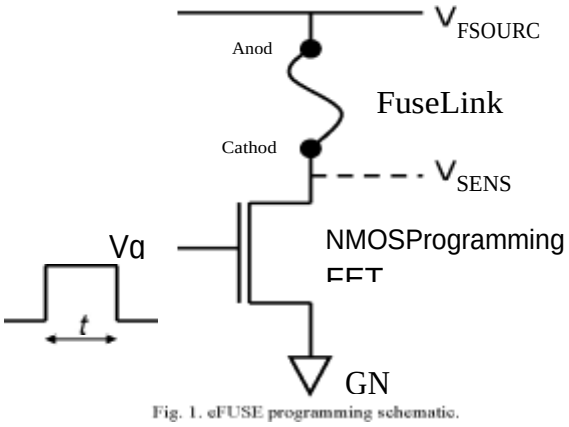

Fig. 1. eFUSE programming schematic.

Fig 2 shows eFuse programming circuitary

The initial design requirements for the sense circuit was to interpret any polysilicon fuse of less resistance than 500Ω as ‘‘unprogrammed’’ and any fuse of greater resistance than 5 kΩ as ‘‘programmed.’’A further requirement for the sense circuitry was that it must not draw more than 500 µA of current through the fuse to prevent reverse electro-migration from occurring. The first state is the steady state for the sense circuit, in which it holds the current state in the half-latch structure created by FETs P1, N14, and N15, and inverter I28. The second state is the precharge state, in which the latch feedback loop is broken by turning off n-FET N15 and the node sense node is precharged via p-FET P8. The third state is the fuse sense state, where n-FET N1 is turned on and the voltage divider is set up between p-FETs P8/P1 and the polysilicon fuse through n-FETs N1 and N4.

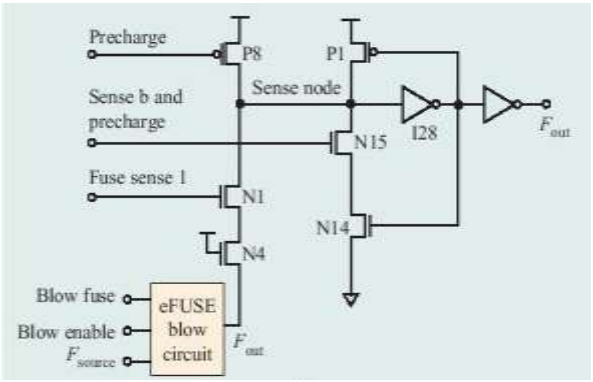

Fig 3 shows eFuse sense circuitary

TABLE 1 STATE-MACHINE SEQUENCE TO SENSE EFUSE

Time	Precharge	Sense b and precharge	Fuse sense 1	Fuse sense 2
0	1	1	0	0
1	0	0	0	0
2	0	0	1	1
3	1	0	1	1
4	1	1	0	0

The inverter I28 and p-FET P1 are then used to sense the state of the fuse. lFUSEs can be programmed only at wafer test. eFUSEs can be programmed much later in the manufacturing flow (but not in the field). ‘‘Soft fuses’’ are implemented by programmable and scannable latches, can be programmed even in the field, and are used to override hard fuses and they are used to control the programming of the eFUSEs.

A. Programming

Fuses are blown one at a time in order to limit IR drop on the Fsource line.

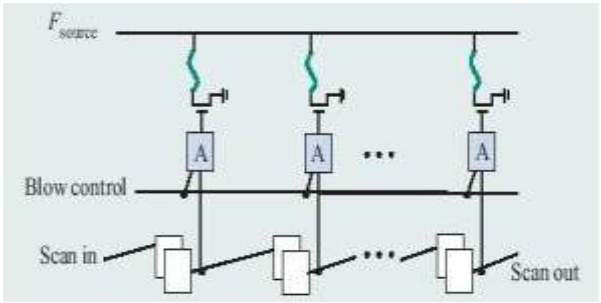

Fig 4 shows eFUSE programming logic

1. Flush zeros into the soft-fuse scan chain.
2. Scan a single ‘‘1’’ into the nth position in the soft-fuse chain, corresponding to the first fuse to be blown.
3. Set blow control high to blow fuse.
4. Set blow control low, flush chain with zero.
5. Scan in a single ‘‘1’’ to the mth position, corresponding to the second fuse to be blown.

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE

International Journal of Advanced Research in Computer and Communication Engineering

NCRICT-2017

Ahalia School of Engineering and Technology

Vol. 6, Special Issue 4, March 2017

6. Repeat Steps 3 and 4 to blow the next fuse.
7. Repeat Steps 5 and 6, modifying m until all required fuses are blown.An alternative, more efficient method isto follow Steps 1–3 above but then continue the scan to the next fuse blow position:
4a. Set blow control low but do not flush chain.
5a. Apply m–n clocks to scan the single '1' to the mth position, corresponding to the second fuse to be blown.
After that fuse is blown, the scan is continued to the next position. That fuse is blown. This continues until all fuses are blown. In this way, all fuses are blown with a single scan of the fuse chain.

B. Reading

Reading is accomplished by generating an initialization signal to read the eFUSE value into its sense latch. The steps are as follows:
1. Initializing test controls and state machine.
2. Set eFUSE select to use either test controls or state machine for precharge/sense eFUSE read sequence.
3. Run precharge/sense sequence to initialize eFUSEs and set eFUSE sense latches.
4. Set fuse select and fuse control inputs to 0 to capture eFUSE values in soft-fuse latches.
5. Scan out soft-fuse latches to verify eFUSE values.

IV. APPLICATIONS

The major applications are electronic chip ID (EID), array redundancy, recording chip parametric data, implementing fault tolerance on specific arrays, recording MCM specific data, array repair at the MCM level, and recording the total blown-fuse count.

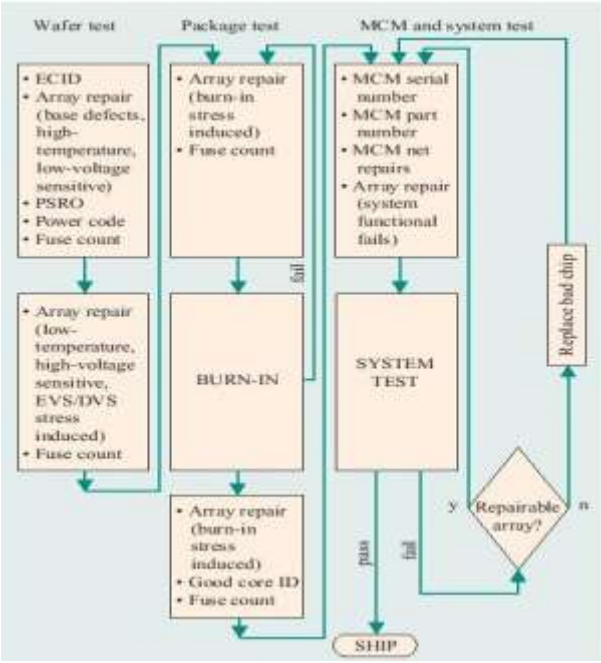

Fig 5 shows eFUSE applications at various test steps

V. CONCLUSION

EFUSEs are easily programmed, easily read, and reliable. Burn-in yield recovery, multichip module (MCM) electronic ID, MCM substrate repair, and MCM array repair without chip replacement are now possible. Since eFUSEs are significantly smaller than laser fuses and scale with the technology, more redundancy is available for less area. It is extremely convenient and elegant when pertinent test and redundancy data resides on the chip or MCM itself, with no external lookup required. The main challenges to eFUSE technology are from database lookup methods or electrically erasable programmable read-only memory (EEPROM) implementations, in which redundancy information is no longer stored on the chip as it is needed. This is driven by a predicted steep increase in required redundancy based on more dense arrays, process variation, projected defect levels at volume ramp time, and so on. Cost is also a factor. Now a days compression schemes have been proposed to reduce the number of fuses and the associated area required. There is an attractive simplicity in the ''plug-and-play'' aspect of eFUSE technology, with no external referencing required, especially for critical elements such as array redundancy.

ACKNOWLEDGMENT

We would like to express our heartfelt gratitude to all those who complemented our efforts, whose stimulating suggestions and constant encouragement helped us to successfully complete this work. Further we acknowledge the authors of the reference documents from which we sourced the materials and resources needed to conduct the present study.

REFERENCES

[1] J. S. Huang, H. K. Liou, and K. N. Tu, "Polarity effect of electromigration in Ni Si contacts on Si," Phys. Rev. Lett., vol. 76, no. 13, pp. 2346–2349, 1996.
[2] O. Torreiter, U. Baur, G. Geocke, and K. Melocco, ''Testing the Enterprise IBM System/390* Multi Processor,'' Proceedings of the IEEE International Test Conference, 1997, pp. 115–123.
[3] T. Foote, D. Hoffman, W. Huott, T. Koprowski, B. Robbins, and M. Kusko, ''Testing the 400MHz IBM Generation-4 CMOS Chip,'' Proceedings of the IEEE International Test Conference, 1997, pp. 106–114.
[4] C. Kothandaraman, S. K. Iyer, and S. S. Iyer, ''Electrically Programmable Fuse (eFUSE) Using Electromigration in Silicides,'' IEEE Electron Device Lett. 23, No. 9, 523–525 (2002).
[5] IBM System z9 eFUSE applications and methodology R. F. Rizzolo, T. G. Foote, J. M. Crafts, D. A. Grosch, T. O. Leung, D. J. Lund, B. L. Mechtly, B. J. Robbins, T. J. Slegel, M. J. Tremblay, G. A. Wiedemeier (2004).
[6] Electrically Programmable Fuse (eFUSE):From Memory Redundancy toAutonomic ChipsNorm Robson; John Safran; Chandra sekharanKothandaraman; Alberto Cestero; XiangChen; Raj Rajeeva kumar; Alan Leslie; Dan Moy; Toshiaki Kirihata; Subramanian Iyer2007 IEEE Custom Integrated Circuits ConferenceYear: 2007 Pages: 799 804, DOI: 10.1109/ CICC. 2007.4405850
[7] A Tag based solution for efficient utilization of efuse for memory repair HarsharajEllur and Kalpesh Shah Texas Instruments, Inc. Bangalore, India, (2014).