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An Efficient Way of Fruition Analysis on Content Addressable Memory

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Abstract: Content Addressable Memory (CAM) is a memory device that is addressed to the content (or data) rather than the memory address. It is widely used in many applications that require fast table lookup and the prequel estimation aspect. It is used to boost up RAM performance and used to fast searching purpose. Basically CAM can be classified into two types NAND-CAM and NOR-CAM. Another type of CAM is neither a Hybrid CAM which intent to neither associates the fruition of target of NOR type CAM with the energy efficient NAND type CAM.

Keywords: Content Addressable Memory (CAM), Hybrid CAM architecture, Fast searching administration, High performance.

INTRODUCTION

In a modern era, the purpose of memory storage gets increased and speed of the memory device is gets higher/ slower according to the amount of data feeded into the processor. Speed of the processor will varies according to the size of the memory device. In order to boost up the performance of a storage device a special set up is placed beneath of RAM. Content Addressable Memory which is placed before the RAM to improve search operation of processor .The size of the device is smaller when compared to the RAM. So area wise it will not affect the RAM operation and performance. It is suitable for various applications. As it performs the contrary function of search operation, it will fetch the address/data from the memory in a single clock cycle. If it take address as input then the outperforms the data. So we can fetch the binary out data when multiple character inputs are given. Existence of several types of CAM cell architecture that gives various valuable results like low power, high speed, high performance and so on. NAND TYPE cam cell, NOR type CAM cell, and Hybrid CAM cell. The first two architectures are the basic cells. The third design of Hybrid CAM cell is the weaving manner design of CAM cells which are specially proposed for a geared up performance. The power consumption of the cells are splitted according to their operating and precharge voltages.

I. CONVENTIONAL CAM

A. Types of CAM

Conventional CAM architecture traditionally consist of NAND and NOR type CAM cells. NAND type CAM cell provides low power consumption. But in the performance area speed is drastically poor due to the sequential data search. So latency increased. Moreover NAND type CAM cells are suffered from charge sharing problem. Charge sharing in the sense the amount of charge stored at the output node in the charging phase could be shared with the junction capacitance of transistors which are in evaluation phase. Here the gain of low power is fail to meet its courtesy. Prequel operation of NOR type CAM cells will creates the wide usage of this. So for a speedy function designer neither are mostly preferred NOR type CAM cells.

B. NAND and NOR CAM

The feature is, NOR type CAM will provide a geared up attainment compared with NAND type cell. Match line schemes are distributed in both types of CAM cells through which the data words are processed. NAND type match line is not suitable for high performance CAM with long word nevertheless the large delay and charge sharing problem. An example table of CAM with various 4 –bit data word entry,

TABLE1.

DATA ENTRY NO.	ADDRESS (BINARY INPUT)	OUT PORT
1.	1 0 1 X X	OUTPORT A
2.	0 1 1 0 X	OUPUT PORT B
3.	0 1 1 X X	OUTPUT PORT C
4.	1 0 0 1 1	OUTPUT PORT C

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Traditional CAM cell that performs reverse operation is shown in figure,

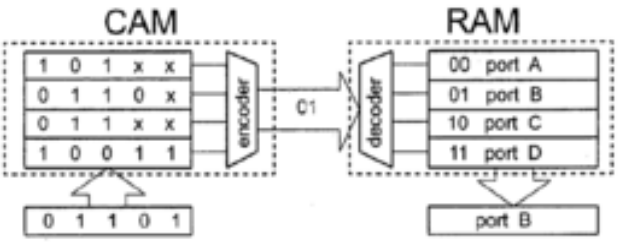


Fig 1.Classical CAM array implementation with data entry.

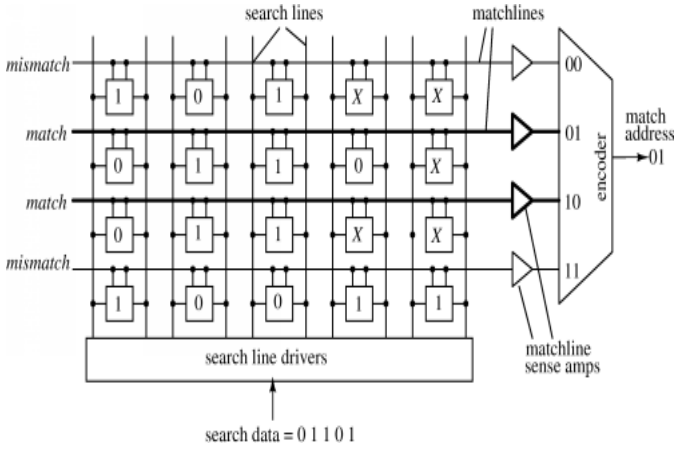
As we early said, CAM will the data as input and give the address output of the given input. From the above figure, data words are feeded into the device. If control bits and data bits are matched the output will be the high logic as '1'. If it is not matched the output will be '0'. Like that from the figure words are matched at the level of 01'. So CAM will fetch the corresponding address which is stored at the RAM. Through this operation the searching speed of the memory gets increased by CAM circuit.

II. MATCH LINE SCHEMS

several match line schemes are availablein CAM cell design. NML (NAND type match line), NOML (NOR type match line) and HML (Hybrid match line), NCC (NAND type CAM cell) NOCC (NOR type CAM cell). Operating and precharege valtages has some difference corresponds to their operation. An operating voltage has to be given to a particular circuit the only the system starts counducting. but a contant amount of potential energy which is given to the match line to drive the logic level form 0-1 transition. After getting the energy the match line will look the nwxt wors if it is match or mismatch. This is the importance of match lines.

A. NAND type match line

NAND type match lines are performs sequential search operation in low power and low speed. The following picture will explain the function of NCC.



Figs 2.Design of NAND type match line.

NAND type CAM cells are commonly preferred by the designers because of its low power consummation. Match lines are initially activated to high logic and they are defaultly programmed if logic '1' occurs the bit will match or else '0' occurs the bit will mismatch. The input data word is loaded into the search data drivers. These search line drivers are distribute the search word onto the distinctive search lines. Each and every CAM core cell compares its data bit which is stored in it against the bit on the corresponding search lines. Finally matched words are disperse at the output side and the word consist of at least one missing bit will be discharged to ground.

B. NOR type match line

NOCCs are performed in payroll functions in order to give high speed and high performance.

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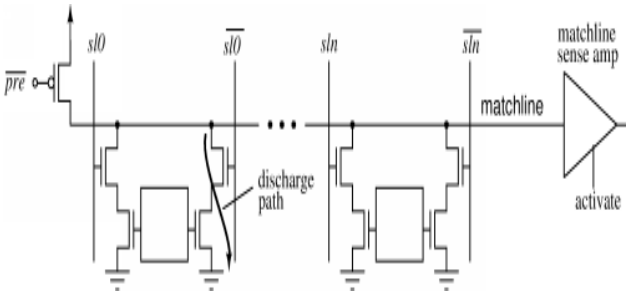

Fig 3. NOR type CAM cell

From the design itself we can see the transistor cells are arranged in prelate manner to provide high speed operation. Initially precharge voltage is given to every match line to drive the word data. Initially Control bit is set to zero. Match lines are compared with the control bit if '1' occurs the source of the transistor is connected to VSS so the output will be '1'. Otherwise it will drained to GND. As it is like a pipelined method, when a single bit completed its processed then the next bit from the second word will entered into the cell and it will be processed. These processes are continued concurrently until all the bits are transmitted. . There are some techniques proposed by developed authors shown below.

C. hybrid CAM

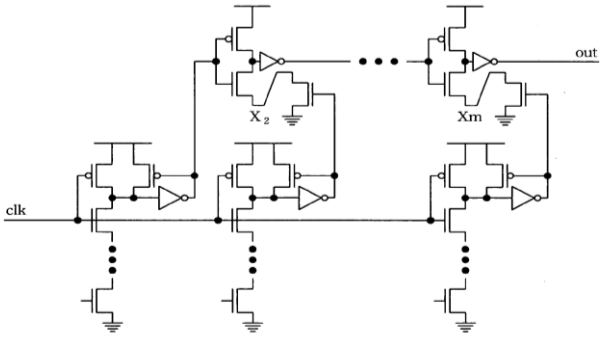

Fig 4. Design of hybrid CAM

Initially all the inverters are made to high. The designers made default program to the transistor such that for match for high logic and mismatch for low logic. An external input is entered into the circuit the search line will compares the data if it is matched with the match line bit. This process will continue for all the data bit. Drain terminal of all the inverters are made to zero. If the data bit matches the supply will connected, if GND will connected then there mismatch occurs. CAM serves the purpose of data search operation fast in a manner that functioned on both depressed energy and speedy act. The hybrid architecture of CAM cells are the concoction model of both NCC and NOCC. Exceptional to area considerations this arrangement of CAM cells will display an eminent attainment and colossal acceleration. From this hybrid procedure variety of techniques introduced to improve the CAM performance in ala the areas.

D. speed vs power analysis

From previous and existing CAM design methodology various factor are rising and falling due to the power, speed, and area measurements. The following representation will display the fruition analysis of various CAM cells

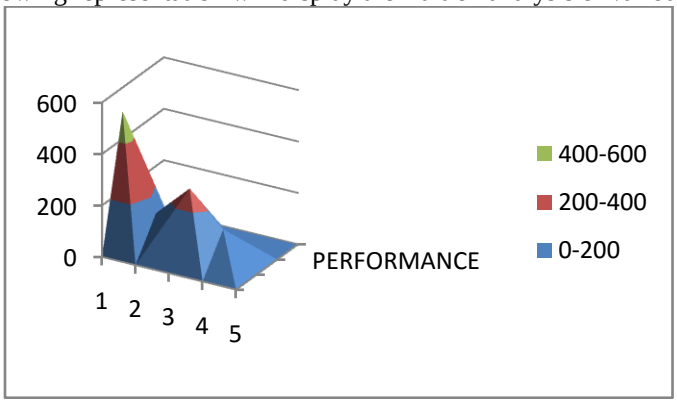

Fig 5. Graphical representation of power and speed.

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Analysis of Speed and power consumption for various CAM architectures are shown below,

TABLE 2. Speed vs. power

CAM TYPES	SPEED	POWER CONSUMPTION
CONVENTIONAL CAM	2.47 s	508 µw
NAND TYPE CAM	1.65 s	144 µw
NOR TYPR CAM	1.04 s	271 µw
PRE-CHARGE FREE CAM	1.42 s	144 µw

E. Equations

- In CAM cells search time[9] is defined as the time needed to provide default voltage contrast between the Match line and the source voltage.

$$Tsearch\ (\Delta\ min) = 0.1\ *vdd$$ with respect to the reference source.

Where, Tsearch is the search time and vdd is the power supply.

- Search power consumption plays a major role in CAM cell power management. Search line power consumption mainly depends on wire capacitance and gate capacitance of initial transistor of each row. The dynamic energy consumption of CAM circuit is,

$$PSL = 2n \times \frac{1}{2} C_{SL} V^2 DD\ f$$
$$= nC_S v^2\ DD\ f$$

- Where denotes, Psl is the total power consumption of search line, Csl is the single search line capacitance,,2n notifies the number search lines and vdd is the souce energy.
- Search power consumption of NOCC is fixed around of 3.40µw. but due to the implementation of some special technique the search power consumption is reduced to some amount that could also be considerable.
- Several techniques are proposed in last few years in CAM to improve number of factors like low power, high performance, delay reduction, voltage swing reduction, speed improvement, neglect capacitance and so on. Those are shown below

F. Performance comparision table

S.NO	TECHNIQUE PROPOSED	ADVANTAGES OF THE PROPOSED TECHNIQUE	DRAWBACKS
1.	combine the master slave architecture with charger refill technique [1]	Reduction of, switching power, refill swing ,parasitic capacitance	MSML takes high power, all performance- worst case, nor type cam used.
2.	Short circuit current in NOR-TYPE (ML) match line. [2]	Separate power supply for each ML. Possible sc current.	ML capacitance has to be precharged. Speed is limited. NOR experiences sc.
3.	hybrid type CAM[3]	Fast search operation, Reduces nor type search performance.	High power consumption.
4.	Early prediction MLs	Reduces the voltage swing of the MML. Performance improved. Differential match line.	NOR-TYPE cam cells are used.
5.	Self disabled sensing technique[5]	No W/R circuit. Sense Amplifier sense the. Voltage change.	NAND type CAM. Large searching time. Very slow performance.
6.	Hybrid CAM implemented using 30nm SOI technology. Utilizing the BSIM model[6].	Sc power is reduced. Search power consumption is roughly reduced.	Extra potential to charge and precharge. Not reliable for large word length.
7.	HP-SRAM based TCAM.[7]	Hybrid architecture so steep performance. Eliminates the drawbacks of traditional TCAM.	Large area required. Classical TCAM cannot be implemented on FPGA.

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CONCLUSION

Content addressable memory is also be known as an associative memory, associative array and associative storage. The survey on content addressable memory was proposed and various techniques that provides high performance in low power area was invented. While the usage of NOCC the amount of power consumption is less. For performance consideration hybrid content addressable memory can preferred. The comparison table will flow the easy view to get abrupt idea of various techniques in associative array.

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